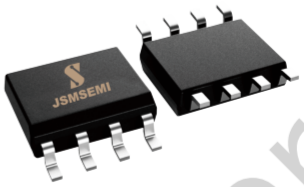
1 DESCRIPTION

The 65HVD233,65HVD234,65HVD235 are used to applications that utilize the ISO 11898-compliant Controller Area Network (CANserial communication physical layer. As a CAN transceiver, each device is used in the differential CAN bus and the CAN controller, each device provides transmit and receive functionality at signaling speeds up to 5Mbps.

Designed for operation in particularly harsh environments, these devices have cross-wire protection, over voltage protection up to ±40V, ground-failure protection,and thermal shutdown protection.These devices can operate over a wide common mode range of -7V to 12V. These transceivers are the interface between the host CAN controller on the microprocessor and the differential CAN bus used in industrial, building automation,transportation, and automotive applications that use differential CAN buses as the applications.It can workin the temperature range of -40°C to 125°C .

2 FEATURES

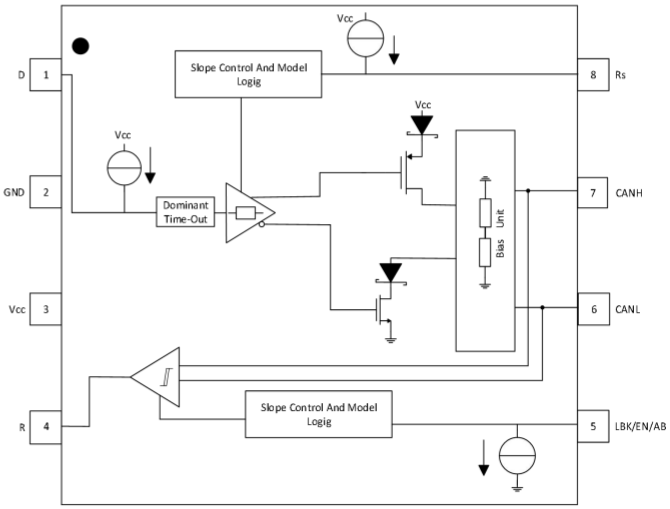
- 3.3V single supply voltage
- Bus pin fault protection greater than ±40V
- Bus pin ESD protection greater than ±16KV HBM
- Data rates up to 5Mbps
- Extended common-mode range: -7V to 12V
- High input impedance supports 120 nodes
- LVTTL I/O withstands up to 5V
- Adjustable driver transition time improves radiated performance
- Unpowered nodes do not interfere with the bus
- Low current standby mode, 400μA (typical)
- 65HVD233: Loopback Mode
- 65HVD234: Ultra-low current sleep mode
- 65HVD235: Automatic Baud Loopback Mode
- Thermal Shutdown Protection
- No interference on bus inputs and outputs during power-up and power-down



3 APPLICATIONS

- Industrial Automation, Controls, Sensors and Drive Systems
- Motor and Robot Control
- Building and temperature control (HVAC)
- Backplane communications and control
- CAN open, Device Net, CAN Kingdom, NMEA 2000, SAE J1939 and other CAN bus standard

Block Diagram



DESCRIPTION(continued)

Modes: The RS pin (pin 8) of the 65HVD233,65HVD234 and 65HVD235 provides three modes of operation: high speed, slope control, and low power standby modes. Directly grounding pin 8 selects the high-speed mode of operation, which allows the driver output transistors to turn on and off as fast as possible with no limit on the rise and fall slopes. The rise and fall slopes can be adjusted by connecting a resistor between the RS pin and ground. The slope will be proportional to the output current of the pin. The device driver has a slew rate of approximately 15V/μs for a resistor value of 10kΩ and 10V/μs for a resistor value of 100kΩ. See the Feature Description for more information on slope control.If a logic high is applied to the R_S pin, then the 65HVD233,65HVD234,65HVD235 enter a low-current standby (listen-only) mode in which the driver is turned off and the receiver remains active. If the local protocol controller needs to send a message to the bus, the device must be returned to high speed mode or ramp control mode via the R_S pin.Loopback (65HVD233): When the 65HVD233's loopback (LBK) pin (pin 5) is logic high,it places the bus outputs and bus inputs in a high impedance state.The D to R path inside the device remains active and can be used for driver-to-receiver loopback, enabling the self-diagnostic node function to be performed without disturbing the bus.For more information on the loopback mode, see the Feature Description.Ultra-Low Current Sleep (65HVD234): If a logic low is applied to the EN pin (pin 5), the 65HVD234 enters an ultra-low

current sleep mode in which the driver and receiver circuits are deactivated. The device will remain in this sleep mode until the circuitry is activated by applying a logic high to pin 5.

Auto-Baud Loopback (65HVD235): The AB pin (pin 5) of the 65HVD235 implements a bus listen-only loopback feature that allows the local node controller to synchronize its baud rate with that of the CAN bus.In auto baud mode, the driver's bus output is in a high impedance state while the receiver's bus input remains active.

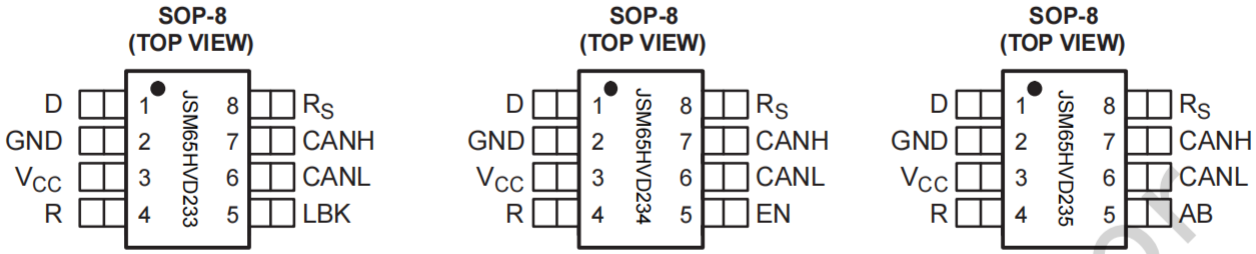
The device has an internal loopback path from the D pin to the R pin to help the controller perform baud rate detection or autobaud functions.

See the Feature Description for more information on Auto-Baud mode.

Order Information

Order number	Package	Marking information	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
SN65HVD233DR	SOP-8	JSM65HV233	-40 to 125°C	3	T&R, 2500	Rohs
SN65HVD234DR	SOP-8	JSM65HV234	-40 to 125°C	3	T&R, 2500	Rohs
SN65HVD235DR	SOP-8	JSM65HV235	-40 to 125°C	3	T&R, 2500	Rohs

4 Pin Configuration and Functions



Pin		I/O	Description
Name	No.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
V_{CC}	3	Supply	Transceiver 3.3V supply
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called output
LBK	5	I	65HVD233: Loopback mode input pin
EN			65HVD234: Enable input pin. Logic high for enabling a normal mode (high speedor slope control) mode. Logic low for sleep mode.
AB			65HVD235: Autobaud loopback mode input pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
R_S	8	I	Mode select pin: strong pulldown to GND = high speed mode, strong pullup to V_{CC} = low power mode, 10KΩ to 100kΩ pulldown to GND = slope control mode

5 Specifications

5.1 Absolute Maximum Ratings(1)(2)

See over operating free-air temperature range unless otherwise noted

Parameter	Description	MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.3	7	V
	voltage at any bus terminal (CANH or CANL)	-40	40	V
V_I	Input voltage(D,R_S,EN,LBK,AB)	–0.5	7	V
V_O	Output voltage	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Operating junction temperature		150	°C
T_{stg}	Storage temperature		125	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage Values, except differential I/O bus voltages, are with respect to network ground pin.

5.2 ESD Ratings

			Value	Unit
V(ESD) Electrostatic discharge	Human body model (HBM)	CANH, CANL and GND	±16000	V
		All pins	±4000	
	Charged-device model (CDM)		±2000	

5.3 Recommended Operating Condition

Parameter	Description		MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
	voltage at any bus terminal (separately or common mode)		-7	12	V
V_{IH}	High-level input voltage	D,EN,AB,LBK	2	5.5	V
V_{IL}	Low-level input voltage	D,EN,AB,LBK	0	0.8	V
V_{ID}	Differential input voltage between CANH and CANL		-6	6	V
	Resistance from R_S to ground		0	100	kΩ
$V_{I(Rs)}$	Input voltage at R_S for standby		0.75V_{CC}	5.5	V
I_{OH}	High-level output current	Driver	-50		mA
		Receiver	-10		
I_{OL}	Low-level output current	Driver		50	mA
		Receiver		10	
T_J	Operating junction temperature	65HVD233/4/5		150	°C
T_A	Operating free-air temperature(1)	65HVD233/4/5	-40	125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

5.4 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

Parameter	Description		Test Conditions	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	D at 0V, R_S at 0V, See Figure1and Figure 2	2.45		V_{CC}	V
		CANL		0.5		1.0	V
V_O	Bus output voltage (Dominant)	CANH	D at 3V, R_S at 0V, See Figure1 and Figure 2		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D at 0V, R_S at 0V, See Figure1 and Figure 2	1.5	2	3	V
			D at 0V, R_S at 0V, See Figure 2 and Figure 3	1.2	2	3	
V_{OD}	Differential output voltage (Recessive)		D at 3V, R_S at 0V, See Figure1 and Figure 2	-120		12	mV
			D at 3V, R_S at 0V, No Load	-0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 9		1		V
I_{IH}	High-level input current	D,EN,LBK,AB	D = 2V or EN = 2V or LBK=2V or AB=2V	-10	-2.5	10	µA
I_{IL}	Low-level input current	D,EN,LBK,AB	D = 0.8V or EN = 0.8V or LBK=0.8V or AB=0.8V	-15	-6.0	15	µA
I_{OS}	Short-circuit output current		VCANH = -7V, CANL Open, See Figure 14	-250			mA
			VCANH = 12V, CANL Open, See Figure 14			1	
			VCANL = -7V, CANH Open, See Figure 14	-1			
			VCANL = 12V, CANH Open, See Figure 14			250	
$I_{IRs(s)}$	R_S input current for standby		R_S at 0.75V_{CC}	-10			µA
I_{CC}	Supply current	Sleep	EN at 0V, D at V_{CC}, R_S at 0V or V_{CC}		0.2	2	µA
		Standby	R_S at V_{CC}, D at V_{CC}, AB at 0V,LBK at 0V,EN at V_{CC}		400	600	
		Dominant	D at 0V, No Load, AB at 0V,LBK at 0V,R_S at 0V, EN at V_{CC}		1	2	mA
		Recessive	D at V_{CC}, No Load, AB at 0V,LBK at 0V,R_S at 0V, EN at V_{CC}		1	2	

(1) All typical Values are at 25°C and with a 3.3V supply

5.5 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

Parameter	Description		Test Conditions		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		AB at 0V,LBK at 0V,EN at V_{CC}, See Table 1			800	900	mV
V_{IT-}	Negative-going input threshold voltage				500	700		
V_{hys}	Hysteresis voltage (V_{IT+} –V_{IT-})					100		
V_{OH}	High-level output voltage		I_O = –4mA, See Figure 6		2.4			V
V_{OL}	Low-level output voltage		I_O = 4mA, See Figure 6				0.4	
I_I	Bus input current		CANH or CANL at 12V	Other bus pin at 0V, D at 3V, EN at V_{CC}	150		500	µA
			CANH or CANL at 12V,V_{CC} at 0V		200		600	
			CANH or CANL at –7V		-610		-150	
			CANH or CANL at –7V,V_{CC} at 0V		-450		-130	
R_{ID}	Differential input resistance		D at 3V,EN at V_{CC}		40	70	100	kΩ
R_{IN}	Input resistance (CANH or CANL) to ground				20	35	50	
I_{CC}	Supply current	Sleep	EN at 0V, D at V_{CC}, R_S at 0V or V_{CC}			0.2	2	µA
		Standby	R_S at V_{CC}, D at V_{CC},AB at 0V,LBK at 0V,EN at V_{CC}			400	600	
		Dominant	D at 0V, No Load, AB at 0V,LBK at 0V,R_S at 0V, EN at V_{CC}			1	2	mA
		Recessive	D at V_{CC}, No Load, AB at 0V,LBK at 0V,R_S at 0V, EN at V_{CC}			1	2	

(1) All typical Values are at 25°C and with a 3.3V supply.

5.6 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Test Conditions	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_S at 0V, See Figure 4		55	85	ns
		R_S with 10KΩ to ground, See Figure 4		80	125	
		R_S with 100KΩ to ground, See Figure 4		110	160	
t_{PHL}	Propagation delay time, high-to-low-level output	R_S at 0V, See Figure 4		80	120	ns
		R_S with 10kΩ to ground, See Figure 4		130	180	
		R_S with 100kΩ to ground, See Figure 4		170	240	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_S at 0V, See Figure 4		25		ns
		R_S with 10kΩ to ground, See Figure 4		50		
		R_S with 100kΩ to ground, See Figure 4		60		
t_r	Differential output signal rise time	R_S at 0V, See Figure 4	25	50	100	ns
t_f	Differential output signal fall time		30	40	70	
t_r	Differential output signal rise time	R_S with 10kΩ to ground, See Figure 4	40	70	150	ns
t_f	Differential output signal fall time		45	60	100	
t_r	Differential output signal rise time	R_S with 100kΩ to ground, See Figure 4	60	100	200	ns
t_f	Differential output signal fall time		70	90	140	
$t_{en(s)}$	Enable time from standby to dominant	See Figure 7 and Figure 8		0.6	1.5	μs
$t_{en(z)}$	Enable time frome sleep to dominant			1	5	

(1) All typical Values are at 25°C and with a 3.3V supply.

5.7 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Test Conditions	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				10	
t_r	Output signal rise time				1.5	
t_f	Output signal fall time				1.5	

(1) All typical Values are at 25°C and with a 3.3V supply.

5.8 Switching Characteristics: Device

over operating free-air temperature range (unless otherwise noted)

Parameter			Test Conditions	MIN	TYP(1)	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	65HVD233	See Figure 11		7.5	12	ns
$t_{(AB1)}$	Loopback delay, driver input to receiver output	65HVD235	See Figure 12		10	20	
$t_{(AB2)}$	Loopback delay, driver input to receiver output	65HVD235	See Figure 13		35	60	
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		R_S at 0V, See Figure 10		90	130	ns
			R_S with 10kΩ to ground, See Figure 10		135	205	
			R_S with 100KΩ to ground, See Figure 10		180	260	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		R_S at 0V, See Figure 10		120	140	ns
			R_S with 10KΩ to ground, See Figure 10		180	215	
			R_S with 100KΩ to ground, See Figure 10		240	280	

(1) All typical Values are at 25°C and with a 3.3V supply.

6 Parameter Measurement Information

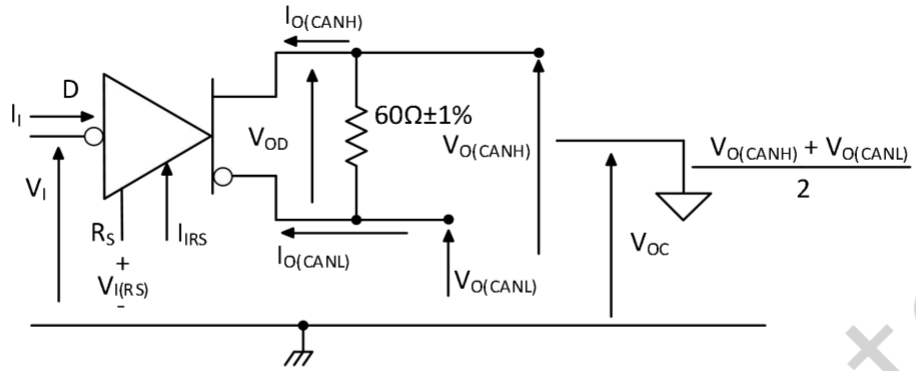


Figure 1.Driver Voltage,Current,and Test Definition

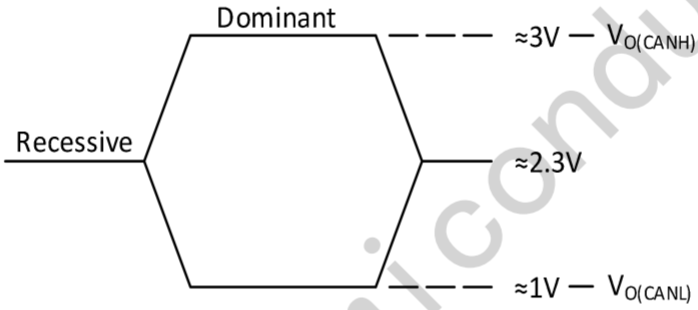


Figure 2.Bus Logic State Voltage Definitions

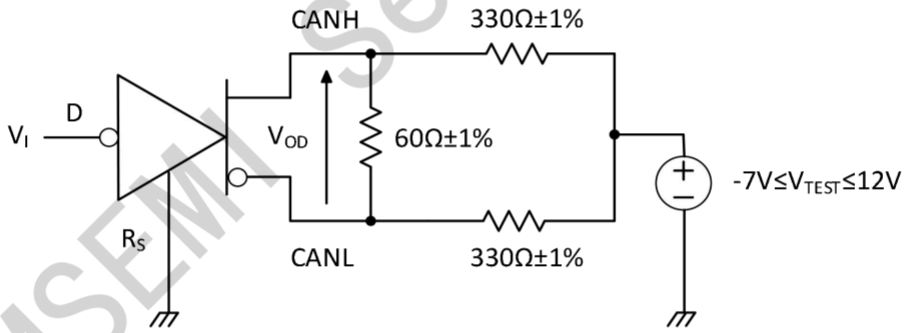
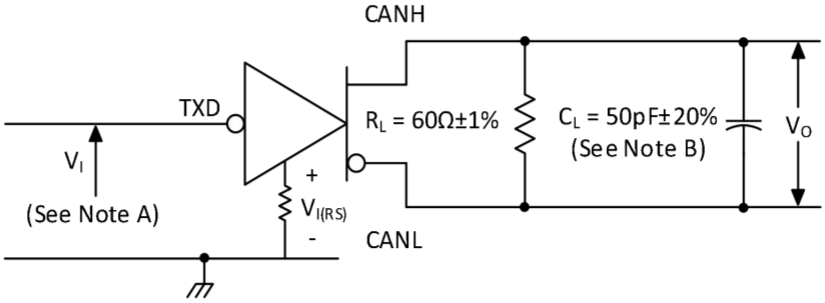
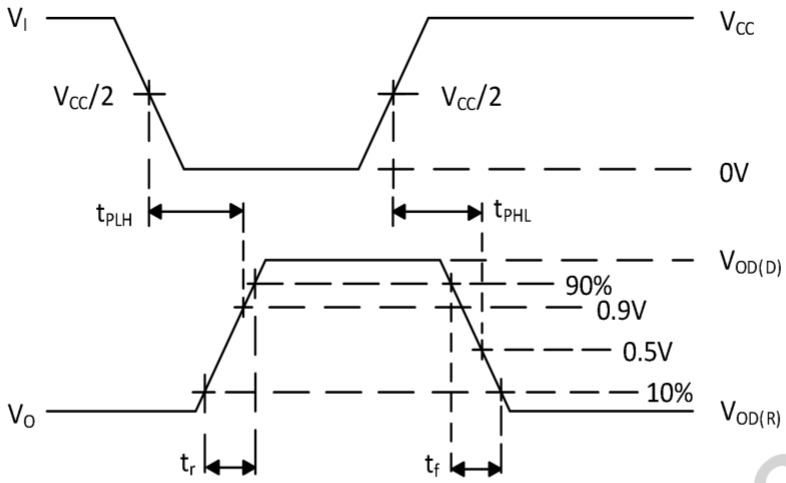


Figure 3.DriverV_{OD}





A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. CL includes fixture and instrumentation capacitance.

Figure 4.Driver Test Circuit and Voltage Waveforms

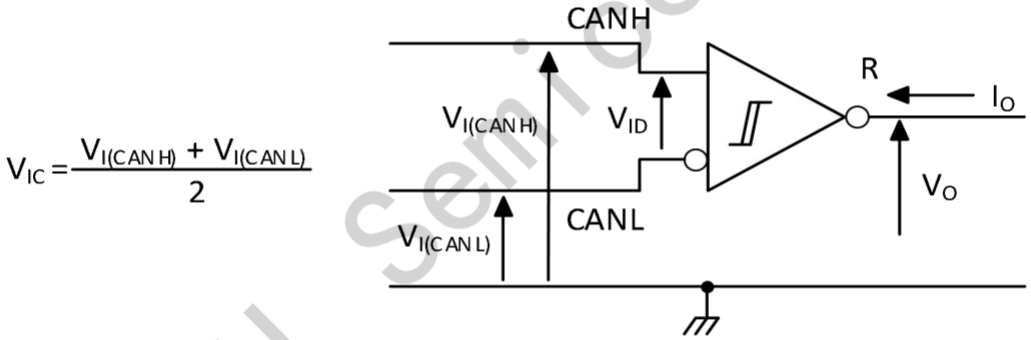
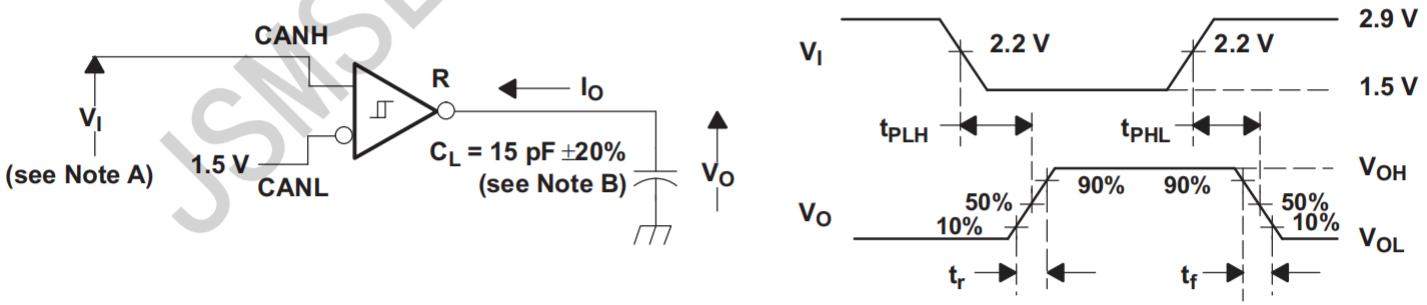


Figure 5.Receiver Voltage and Current Definitions



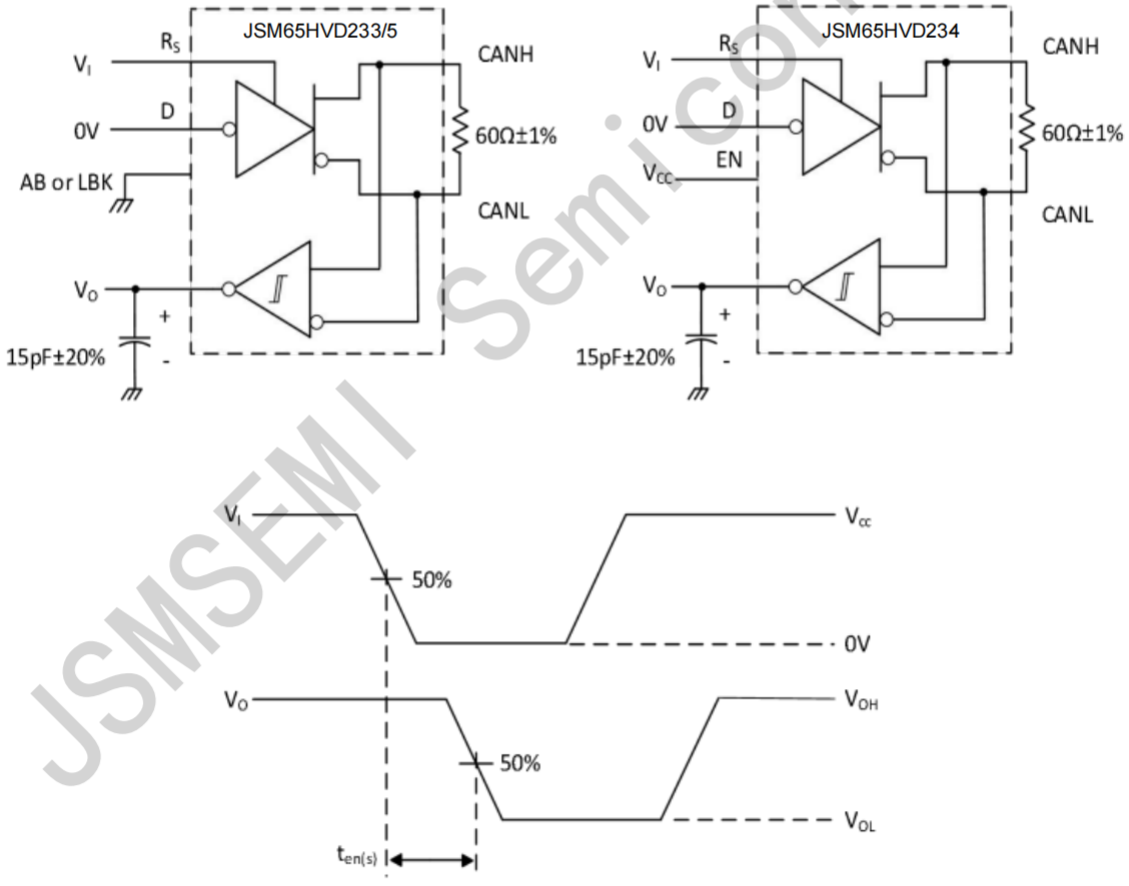
A.The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B.CL includes fixture and instrumentation capacitance.

Figure 6.Receiver Test Circuit and Voltage Waveforms

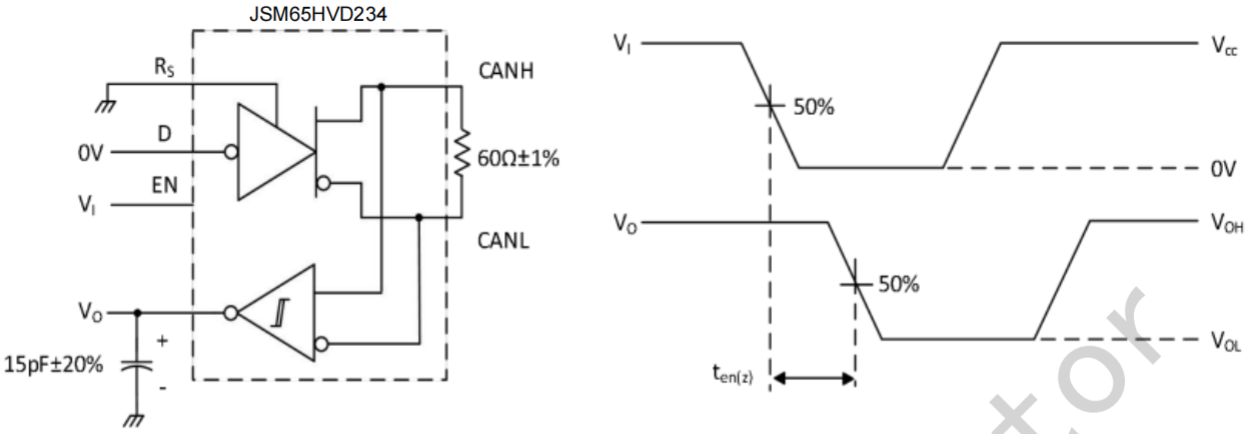
Table 1.Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
VCANH	VCANL	R		|VID|
–6.1V	–7V	L	VOL	900mV
12V	11.1V	L		900mV
–1V	–7V	L		6V
12V	6V	L		6V
–6.5V	–7V	H	VOH	500mV
12V	11.5V	H		500mV
–7V	–1V	H		6V
6V	12V	H		6V
Open	Open	H		X



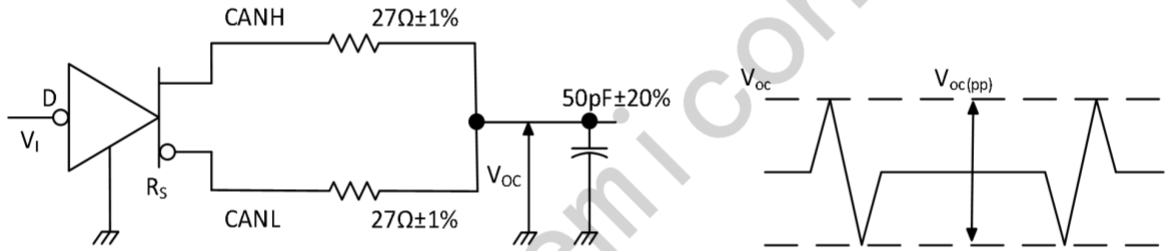
NOTE: All VI input pulses are supplied by a generator having the following characteristics: t_r or t_f≤6ns, pulse repetition rate (PRR) = 125kHz, 50% duty cycle.

Figure 7.$T_{en(s)}$ Test Circuit and Voltage Waveforms



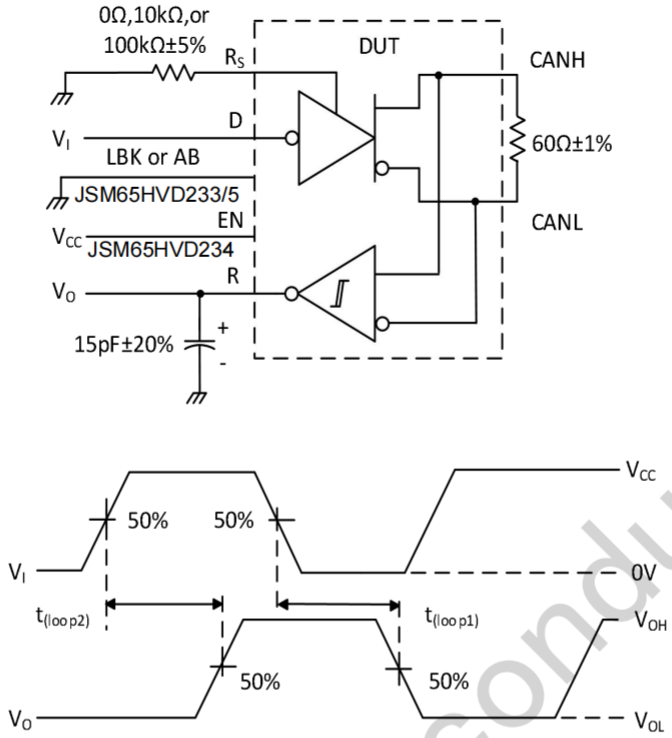
NOTE: All VI input pulses are supplied by a generator having the following characteristics: t_r or t_f≤6ns, pulse repetition rate (PRR) = 50kHz, 50% duty cycle.

Figure 8.Ten(z)Test Circuit and Voltage Waveforms



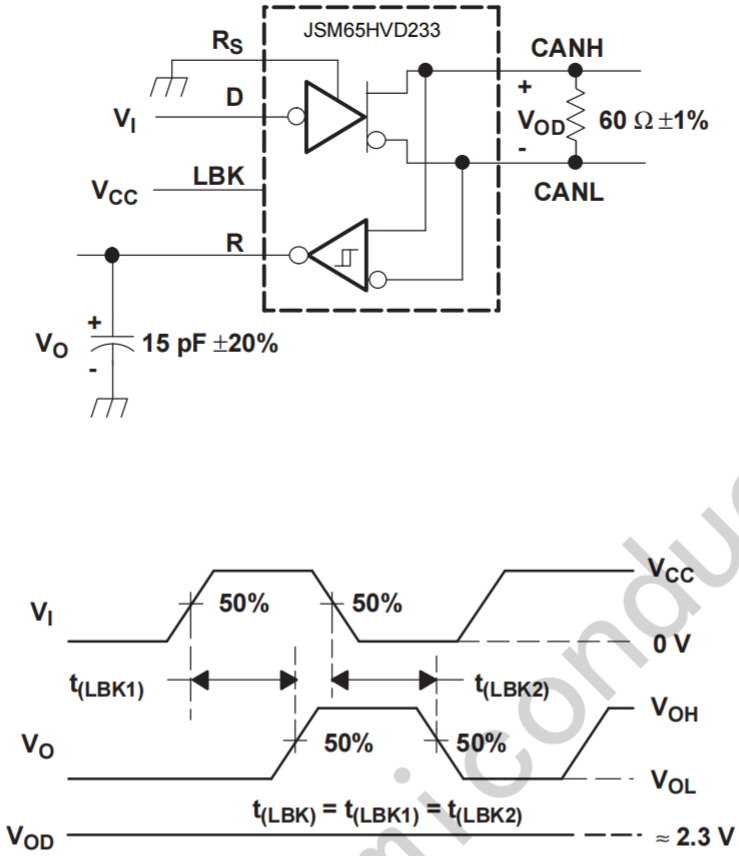
NOTE: All VI input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤6ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9.$V_{OC(pp)}$ Test Circuit and Voltage Waveforms



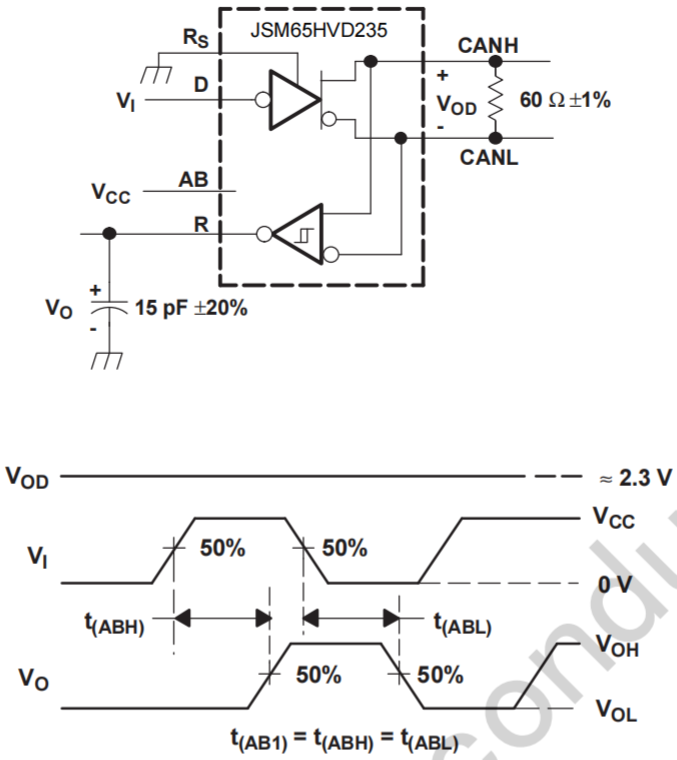
NOTE: All VI input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤6ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10.$T_{(loop)}$ Test Circuit and Voltage Waveforms



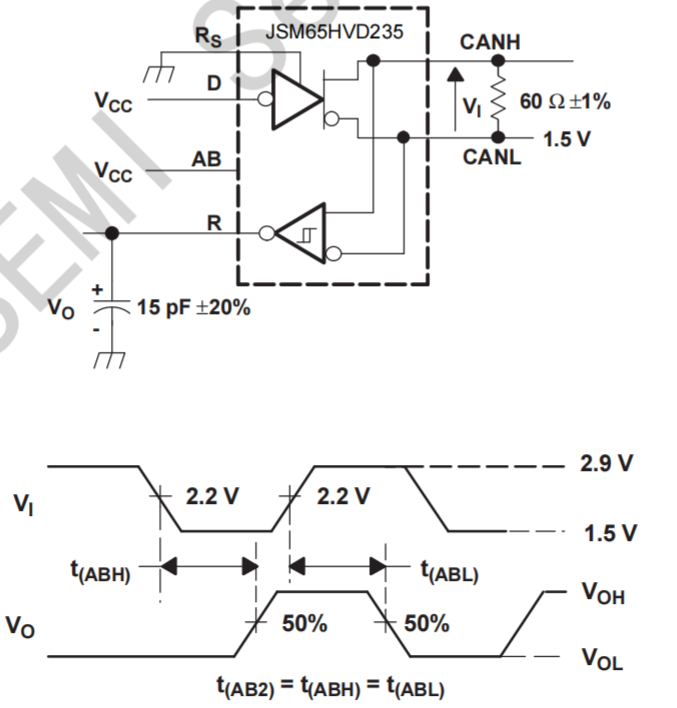
NOTE: All VI input pulses are supplied by a generator having the following characteristics: tr or tf ≤ 6ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11.$T_{(LBK)}$ Test Circuit and Voltage Waveforms



NOTE: All VI input pulses are supplied by a generator having the following characteristics: tr or tf ≤ 6ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 12.$T_{(AB1)}$ Test Circuit and Voltage Waveforms



NOTE: All VI input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 13.$T_{(AB2)}$ Test Circuit and Voltage Waveforms

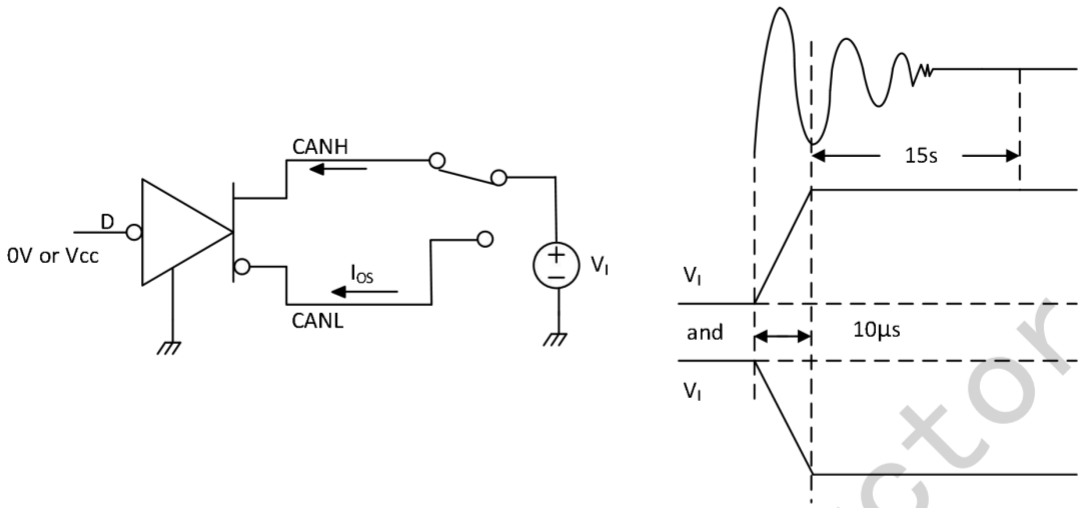
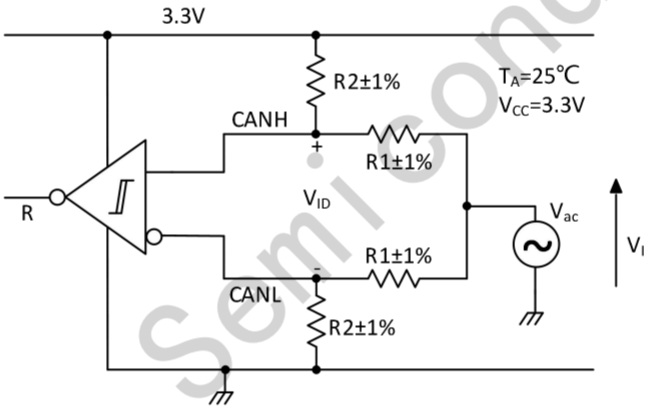
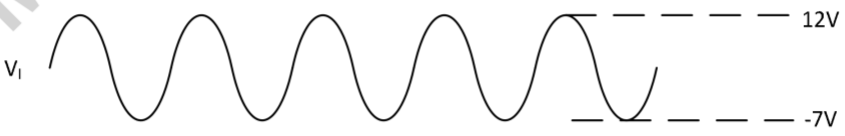


Figure 14.I_{os} Test Circuit and Waveforms



The R Output State Does Not Change During Application of the Input Waveform.

VID	R1	R2
500mV	50	280
900mV	50	130



NOTE: All input pulses are supplied by a generator with f ≤ 1.5MHz

Figure 15.Common-Mode Voltage Rejection

7 Detailed Description

7.1 Overview

This family of CAN transceivers is compatible with the ISO11898-2 High-Speed CAN (controller area network) physical layer standard. They are designed to interface between the differential bus lines in CAN and the CAN protocol controller at data rates up to 1Mpbs.

7.2 Functional Block Diagrams

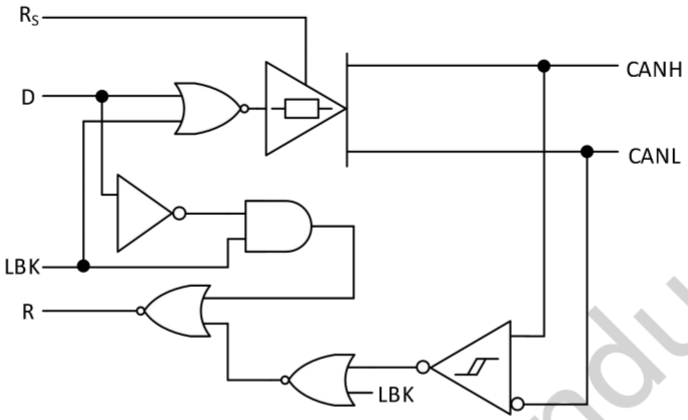


Figure 16.65HVD233 Functional Block Diagram

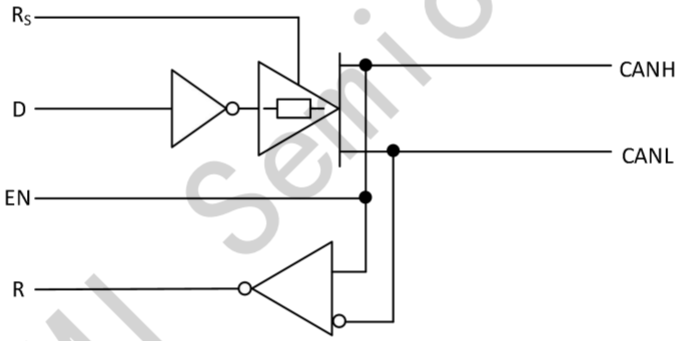


Figure 17.65HVD234 Functional Block Diagram

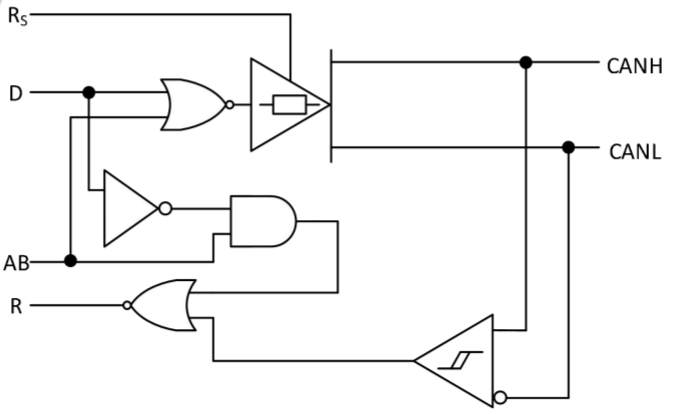


Figure 18.65HVD235 Functional Block Diagram

7.3 Feature Description

7.3.1 Diagnostic Loopback (65HVD233)

The diagnostic loopback or internal loopback function of the 65HVD233 is enabled with a high-level input on pin 5, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (transmit data) through logic to the received data output pin), thus creating an internal loopback of the transmit to receive data path. This mimics the loopback that occurs normally with a CAN transceiver because the receiver loops back the driven output to the R (receive data) pin. This mode allows the host protocol controller to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 23. If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low- level input) and may be left open if not in use.

7.3.2Autobaud Loopback (65HVD235)

The autobaud loopback mode of the 65HVD235 is enabled by placing a high level input on pin 5, AB. In autobaud mode ,the driver output is disabled, thus blocking the D pin to bus path and the bus transmit function of the transceiver. The bus pins remain biased to recessive. The receiver to R pin path or the bus receive function of the device remains operational, allowing bus activity to be monitored. In addition, the autobaud mode adds an internal logic loopback path from the D pin to R pin so the local node may transmit to itself in sync with bus traffic while not disturbing messages on the bus. Thus if the local node's CAN controller generates an error frame, it is not transmitted to the bus, but is detected only by the local CAN controller. This is especially helpful to determine if the local node is set to the same baud rate as the network, and if not adjust it to the network baud rate (autobaud detection).

Autobaud detection is best suited to applications that have a known selection of baud rates. For example, a popular industrial application has optional settings of 125kbps, 250kbps, or 500kbps. Once the 65HVD235 is placed into autobaud loopback mode the application software could assume the first baud rate of 125kbps. It then waits for a message to be transmitted by another node on the bus. If the wrong baud rate has been selected, an error message is generated by the local CAN controller because the sample times will not be at the correct time. However, because the bus-transmit function of the device has been disabled, no other nodes receive the error frame generated by this node's local CAN controller.

The application would then make use of the status register indications of the local CAN controller for message received and error warning status to determine if the set baud rate is correct or not. The warning status indicates that the CAN controller error counters have been incremented. A message received status indicates that a good message has been received. If an error is generated, the application would then set the CAN controller with the next possibly valid baud rate, and wait to receive another message. This pattern is repeated until an error free message has been received, thus the correct baud rate has been selected. At this point the application would place the 65HVD235 in a normal transmitting mode by setting pin 5 to a low-level, thus enabling bus-transmit and bus-receive functions to normal operating states for the transceiver.

If the AB pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low- level input) and may be left open if not in use.

7.3.3 Slope Control

The rise and fall slope of the 65HVD233,65HVD234,65HVD235 driver output can be adjusted by connecting a resistor from the Rs (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 19.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor Value of 10KΩ to achieve a ~15V/μs slew rate, and up to 100KΩ to achieve a ~10V/μs slew rate . A typical slew rate Verses pulldown resistance graph is shown in Figure 20. Typical driver output wave forms with slope control are displayed in Figure 25.

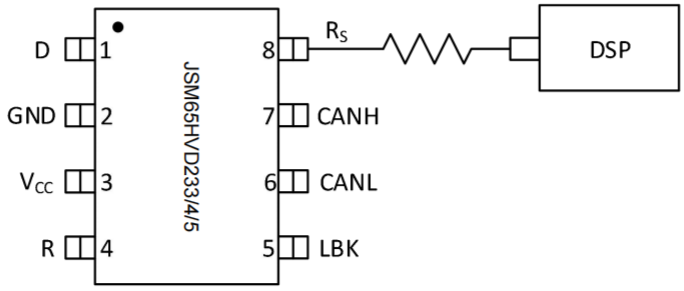


Figure 19. Slope Control/Standby Connection to a DSP

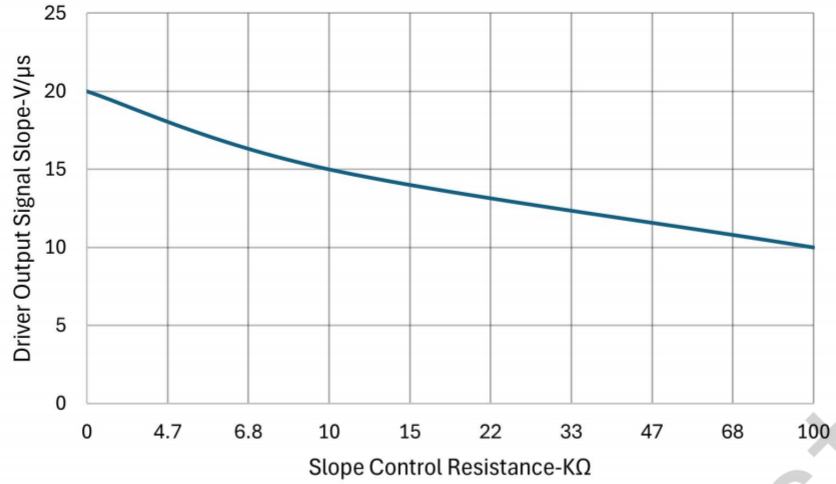


Figure 20. HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

7.3.4 Standby

If a high-level input (> 0.75V_{CC}) is applied to R_S (pin 8), the circuit enters a low-current, listen only standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the R output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the R_S pin low to return to slope control mode or high-speed mode.

7.3.5 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the D pin to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are high impedance biased to recessive level during a thermal shutdown, and the receiver to R pin path remains operational.

7.4 Device Functional Modes

Table 2.Driver(65HVD233 or 65HVD235)

INPUTS			OUTPUTS		
D	LBK/AB	Rs	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

Table 3.Receiver(65HVD233)

INPUTS				OUTPUT
BUS STATE	VID = V(CANH)–V(CANL)	LBK	D	R
Dominant	VID ≥ 0.9 V	L or open	X	L
Recessive	VID ≤ 0.5 V or open	L or open	H or open	H
?	0.5 V < VID <0.9 V	L or open	H or open	?
X	X	H	L	L
X	X		H	H

Table 4.Receiver(65HVD235)(1)

INPUTS				OUTPUT
BUS STATE	VID = V(CANH)–V(CANL)	AB	D	R
Dominant	VID ≥ 0.9 V	L or open	X	L
Recessive	VID ≤ 0.5 V or open	L or open	H or open	H
?	0.5 V < VID <0.9 V	L or open	H or open	?
Dominant	VID ≥ 0.9 V	H	X	L
Recessive	VID ≤ 0.5 V or open	H	H	H
Recessive	VID ≤ 0.5 V or open	H	L	L
?	0.5 V < VID <0.9 V	H	L	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

Table 5.Driver(65HVD234)

INPUTS			OUTPUTS		
D	EN	Rs	CANH	CANL	BUS STATE
L	H	≤ 0.33V_{CC}	H	L	Dominant
H	X	≤ 0.33V_{CC}	Z	Z	Recessive
Open	X	X	Z	Z	Recessive
X	X	> 0.75V_{CC}	Z	Z	Recessive
X	L or open	X	Z	Z	Recessive

Table 6.Receiver(65HVD234)(1)

INPUTS			OUTPUT
BUS STATE	VID =V(CANH)–V(CANL)	EN	R
Dominant	VID≥ 0.9V	H	L
Recessive	VID ≤ 0.5V or open	H	H
?	0.5V <VID <0.9V	H	?
X	X	L or open	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

8 Application and Implementation

8.1 Application Information

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the D and R pins. See Figure 21 and Figure 22.

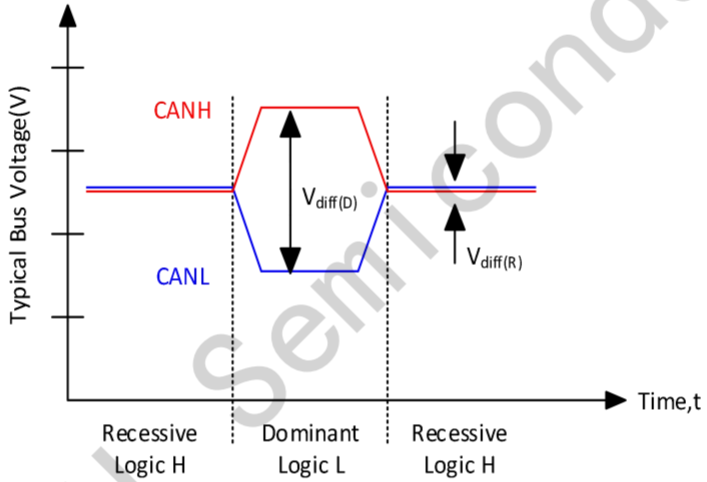


Figure 21.Bus States(Physical Bit Representation)

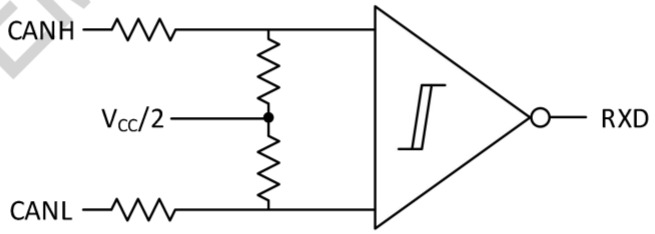


Figure 22.Simplified Recessive Common Mode Bias and Receiver

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.

8.2 Typical Application

8.2.1 Design Requirements

8.2.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898 Standard specifies up to a data rate of 1Mbps, maximum CAN bus cable length of 40 m, maximum drop line (stub) length of 0.3 m and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CAN open, CAN Kingdom, Device Net and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the 65HVD23X CAN family. ISO 11898-2 specifies the driver differential output with a 60Ω load (two 120 Ω termination resistors in parallel) and the differential output must be greater than 1.5V.

The 65HVD23x devices are specified to meet the 1.5V requirement with a 60Ω load,
and additionally specified with a differential output voltage minimum of 1.2V across a common mode range of
- 2V to 7V through a 330Ω coupling network. This network represents the bus loading
of 120 65HVD23x transceivers based on their minimum differential input resistance of 40KΩ. Therefore, the 65HVD23x supports up to 120 transceivers on a single bus segment with margin to the 1.2V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the Various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

8.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

8.2.2 Detailed Design Procedure

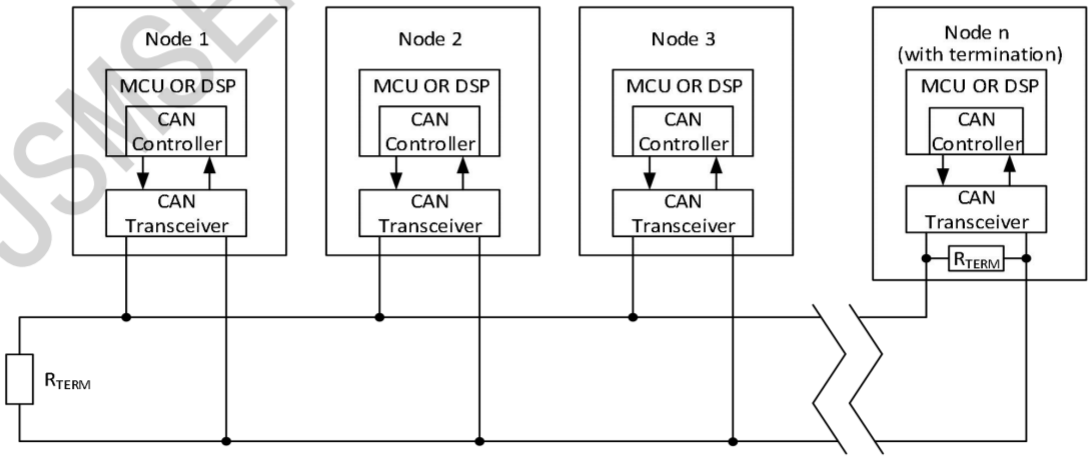


Figure 23.Typical CAN Bus

Termination is typically a 120Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 24). Split termination uses two 60Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.
Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

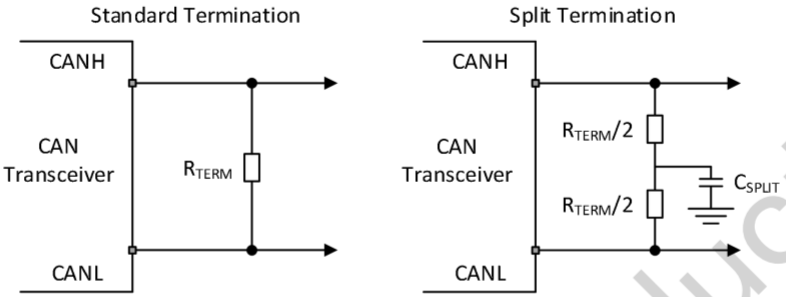


Figure 24.CAN Bus Termination Concepts

8.2.3 Application Curve

Figure 25 shows 3 typical output waveforms for the 65HVD233 device with three different connections made to the R_S pin. The top waveform show the typical differential signal when transitioning from a recessive level to a dominant level on the CAN bus with R_S tied to GND through a 0Ω resistor. The second waveform shows the same signal for the condition with a 100kΩ resistor tied from R_S to ground.

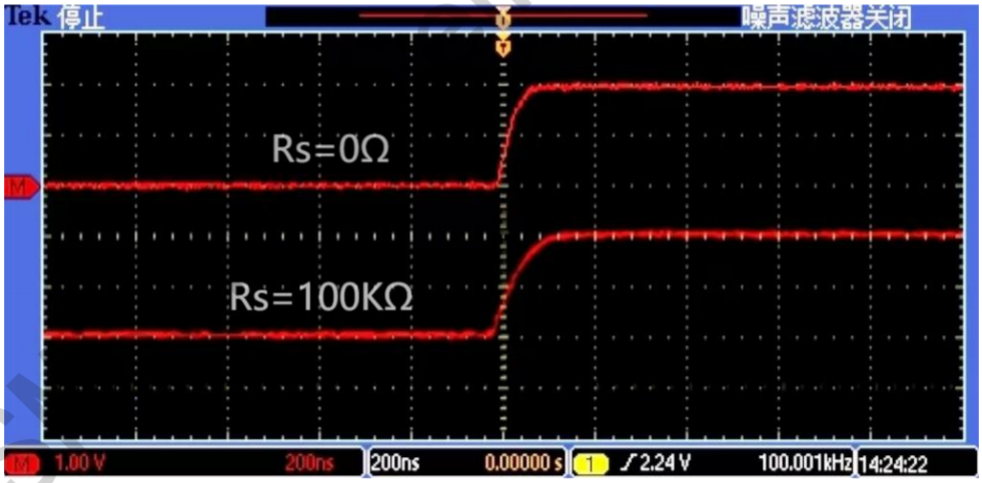


Figure 25.Typical 65HVD233 Output Waveforms With Different Slope Control Resistor Values

8.3 System Example

8.3.1 ISO 11898 Compliance of 65HVD23x Family of 3.3V CAN Transceivers

8.3.1.1 Introduction

Many users Value the low power consumption of operating their CAN transceivers from a 3.3V supply. However, some are concerned about the interoperability with 5V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

8.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the 65HVD23x is greater than 1.5V and less than 3V across a 60 ohm load as defined by the ISO 11898 standard. These are the same limiting Values for 5V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver. A CAN receiver is required to output a recessive state when less than 500mV of differential voltage exists on the bus, and a dominant state when more than 900mV of differential voltage exists on the bus. A CAN receiver must do this with common-mode input voltages from -2V to 7V.

The 65HVD23x family receivers meet these same input specifications as 5V supplied receivers.

8.3.1.3 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias voltage of the recessive state of the device is dependent on V_{CC}, any noise present or Variation of V_{CC} will have an effect on this bias voltage seen by the bus. The 65HVD23x family has the recessive bias voltage set higher than $0.5*V_{CC}$ to comply with the ISO 11898-2 CAN standard. The caveat to this is that the common mode voltage will drop by a couple hundred millivolts when driving a dominant bit on the bus. This means that there is a common mode shift between the dominant bit and recessive bit states of the device. While this is not ideal, this small Variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

8.3.1.4 Interoperability of 3.3V CAN in 5V CAN Systems

The 3.3V supplied 65HVD23x family of CAN transceivers are fully compatible with 5V CAN transceivers. The differential output voltage is the same, the recessive common mode output bias is the same, and the receivers have the same input specifications. The only slight difference is in the dominant common mode output voltage which is a couple hundred millivolts lower for 3.3V CAN transceiver than 5V supplied transceiver.

To help ensure the widest interoperability possible, the 65HVD23x family has successfully passed the internationally recognized GIFT/ICT conformance and interoperability testing for CAN transceivers. Electrical interoperability does not always assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. This comes only with thorough equipment testing.

9 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the V_{CC} supply pins as possible.

10 Layout

10.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or Varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 26.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 26 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground Via capacitor C6. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends. See the application section for information on power ratings needed for the termination resistor(s).

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}).

Use at least two Vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and Via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Since the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1kΩ to 10kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open drain host processor is used to drive the D pin of the device an external pull-up resistor between 1KΩ and 10KΩ and V_{CC} should be used to drive the recessive input state of the device.

Pin 8: is shown assuming the mode pin, R_S, will be used. If the device will only be used in normal mode or slope control mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

10.2 Layout Example

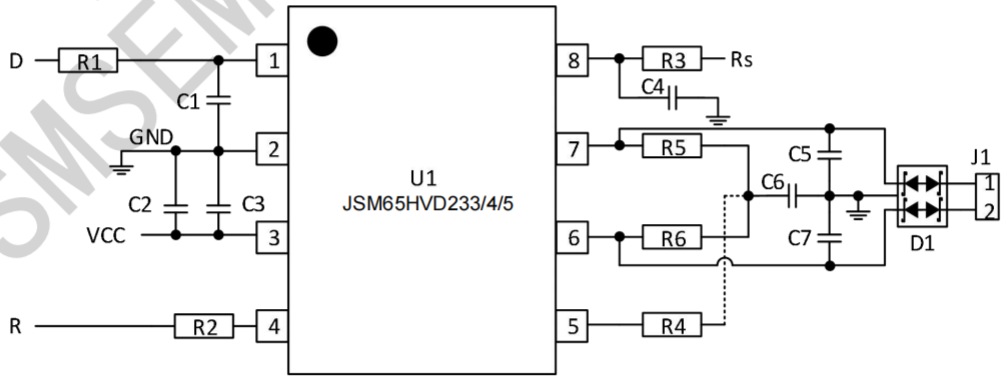
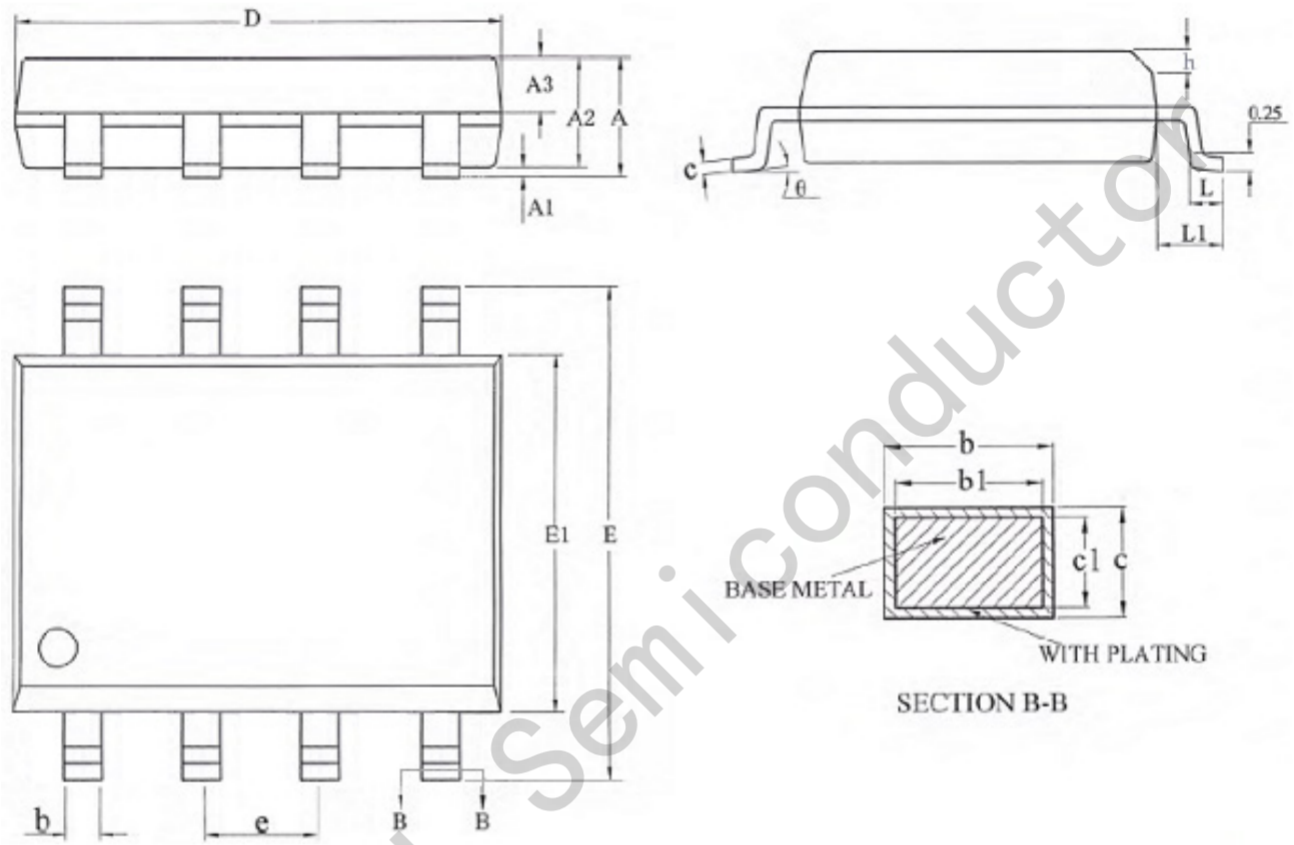


Figure 26.Layout Example Schematic

SOIC-8 Package Outlines



SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	2/23/2024

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