Truesemi®

TSA35N50M

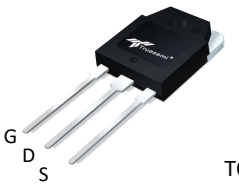
500V N-Channel MOSFET

General Description

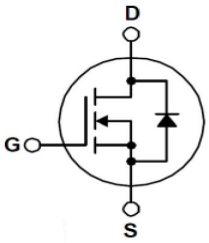
This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

- 35A,500V,Max.RDS(on)=0.155Ω @ VGS =10V
- Low gate charge: Qg=142nC (Typ.)
- 100% avalanche tested
- RoHS compliant device



TO-3P



Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		500	V
V_{GS}	Gate-Source Voltage		± 30	V
I_D	Drain Current	T_C = 25℃	35	A
		T_C = 100℃	22	A
I_{DM}	Pulsed Drain Current *		140	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		2940	mJ
I_{AS}	Repetitive avalanche current (Note 2)		23	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		50	mJ
P_D	Power Dissipation (T_C = 25℃)		500	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

* Limited only maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	--	0.25	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	--	62.5	℃/W

Electrical Characteristics T_C=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D =17.5A	--	0.13	0.155	Ω
R_g	Internal gate resistance	Open drain, f=1MHz	--	0.8	--	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
I_{DSS}	Drain-source cut-off current	V_{DS} =500 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 500 V, T_C = 125℃	--	--	100	uA
I_{GSSF}	Gate-Body Leakage Current,Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current,Reverse	V_{GS} =- 20 V, V_{DS} = 0 V	--	--	-100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	6970	--	pF
C_{oss}	Output Capacitance		--	520	--	pF
C_{rss}	Reverse Transfer Capacitance		--	50	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DD} =250V, I_D = 35A, R_G = 25 Ω (Note 3,4)	--	83	--	ns
t_r	Turn-On Rise Time		--	45	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	375	--	ns
t_f	Turn-Off Fall Time		--	63	--	ns
Q_g	Total Gate Charge	V_{DS} =400 V, I_D =35A, V_{GS} = 10 V (Note 3,4)	--	142	--	nC
Q_{gs}	Gate-Source Charge		--	31	--	nC
Q_{gd}	Gate-Drain Charge		--	46	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	35	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	140	A
V_{SD}	Source-Drain Diode Forward Voltage	I_S =35A, V_{GS} = 0 V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S =35A, V_{GS} = 0 V di_F/dt = 100 A/μs (Note 3，4)	--	530	--	ns
Q_{rr}	Reverse Recovery Charge		--	7.86	--	uC

NOTES:

1. Repeated rating: Pulse width limited by safe operating area
2. L=10mH, I_{AS}=23A, V_{DD}=50V, R_G=25Ω, Starting TJ=25℃
3. Pulse test: Pulse width≤300us, Duty cycle≤2%
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Fig. 1 Typical Output Characteristics

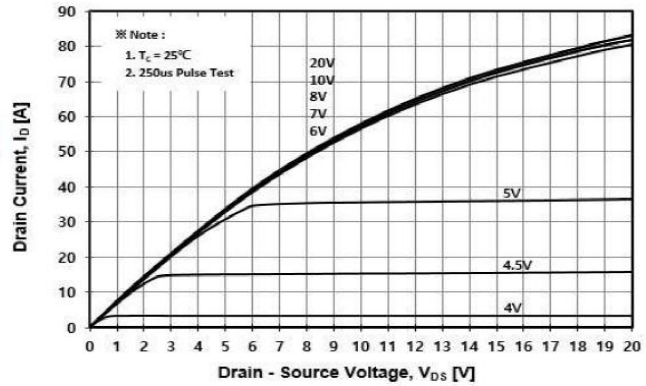


Fig. 2 Typical Transfer Characteristics

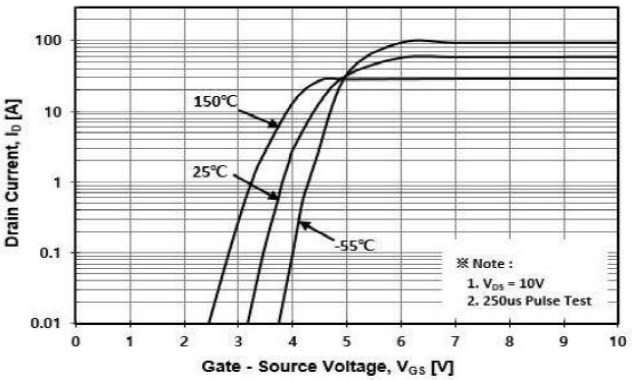


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

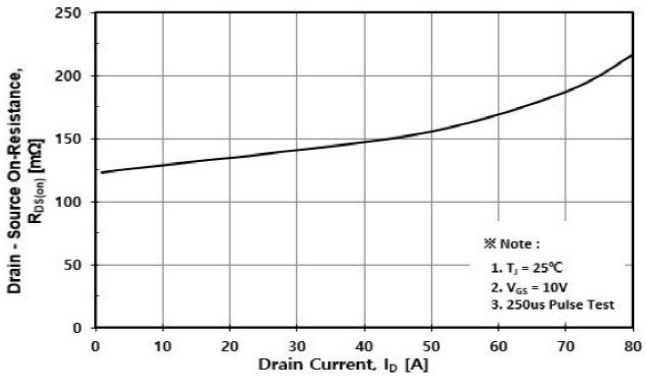


Fig. 4 Body Diode Forward Voltage Variation with Source Current

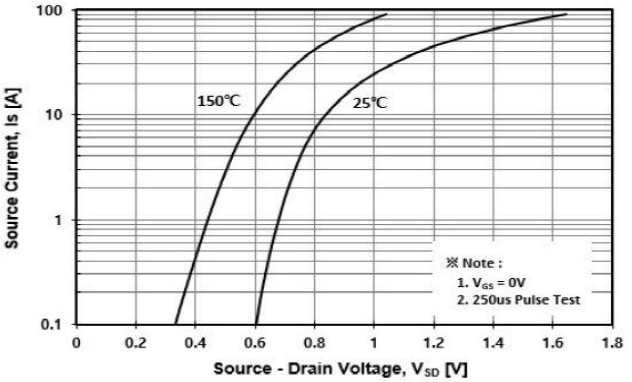


Fig. 5 Typical Capacitance Characteristics

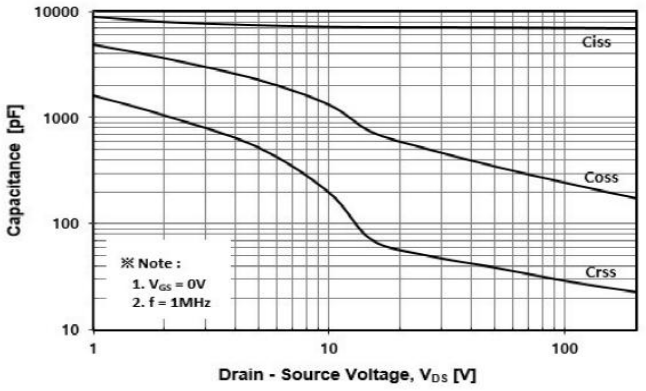
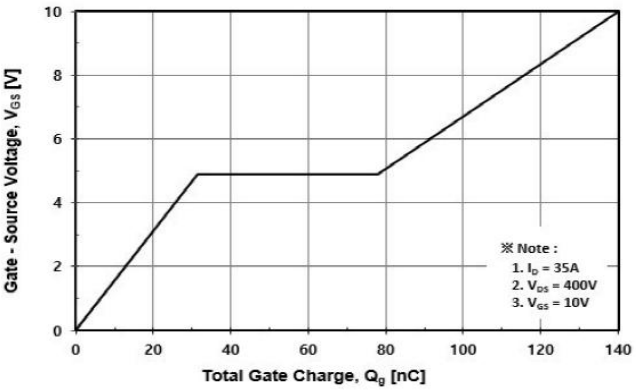


Fig. 6 Typical Total Gate Charge Characteristics



Typical Characteristics Curve (Continue)

Fig. 7 Breakdown Voltage Variation vs. Temperature

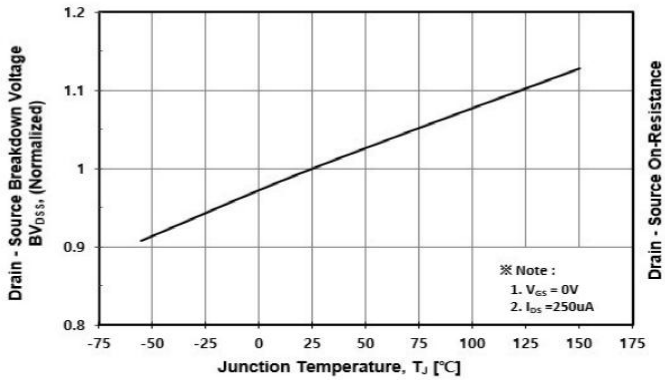


Fig. 8 On-Resistance Variation vs. Temperature

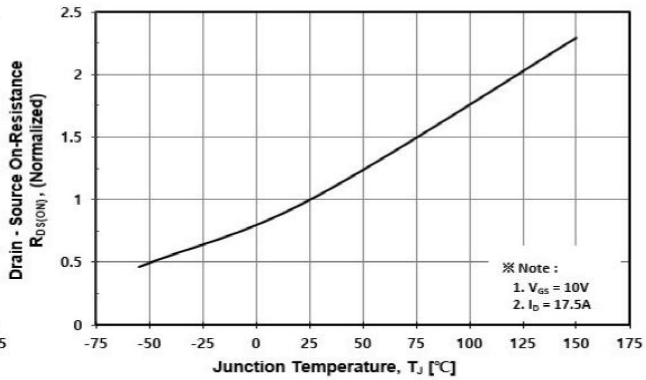


Fig. 9 Maximum Drain Current vs. Case Temperature

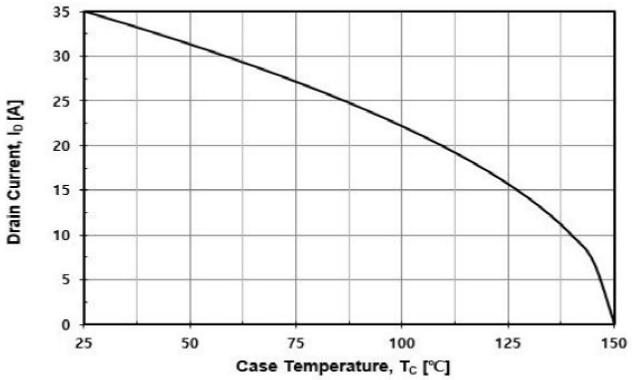


Fig. 10 Maximum Safe Operating Area

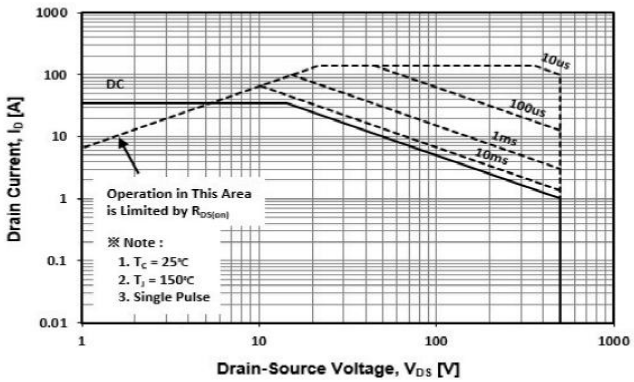


Fig. 11 Transient Thermal Impedance

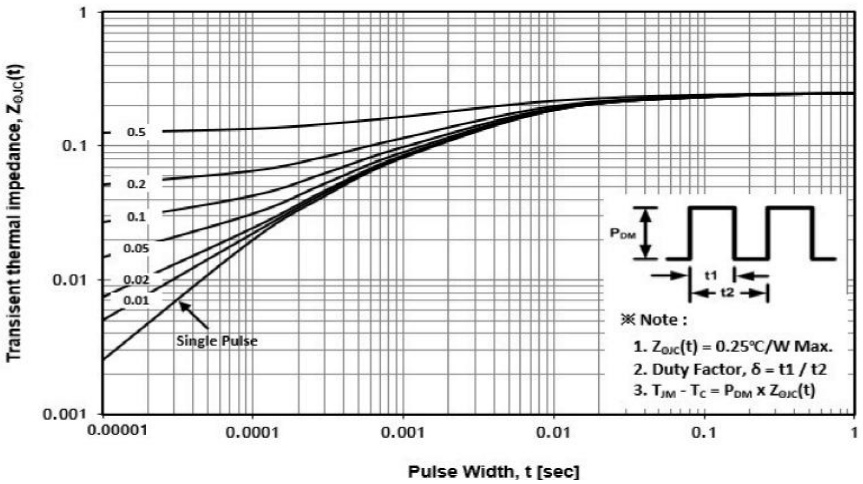
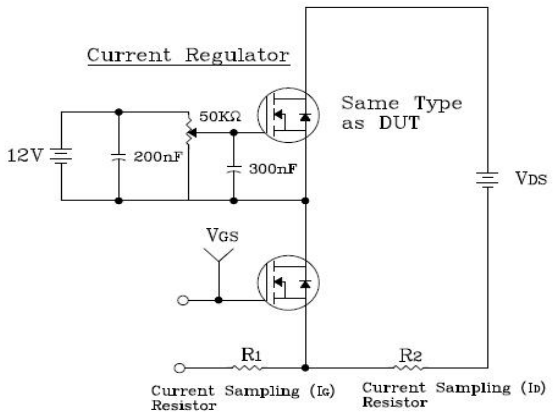


Fig. 12 Gate Charge Test Circuit & Waveform



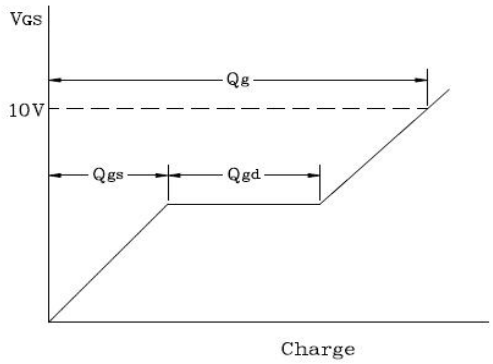
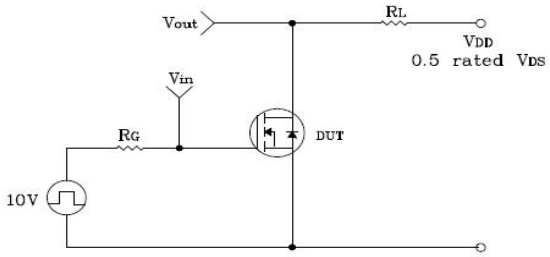


Fig. 13 Resistive Switching Test Circuit & Waveform



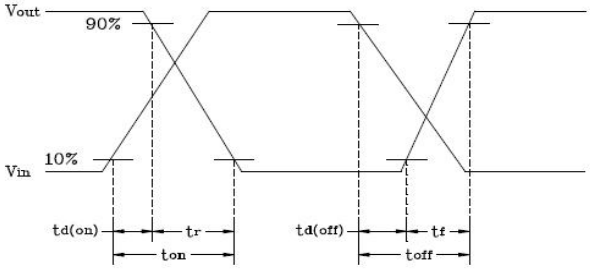
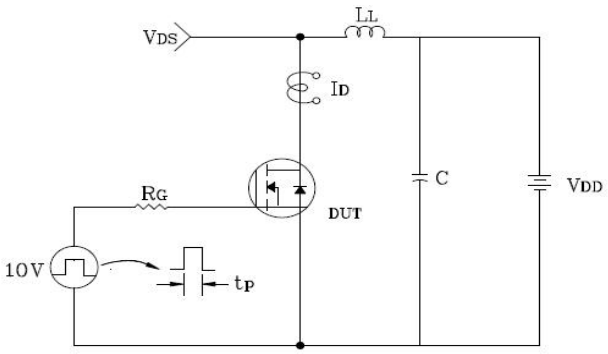


Fig. 14 E_{AS} Test Circuit & Waveform



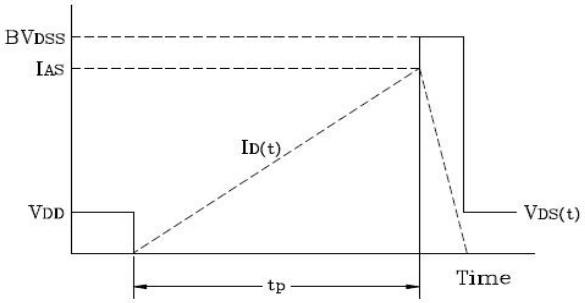


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform