# LP3323
# Boost WLED Backlight Driver with High Accuracy of PWM Dimming

## Features

- Input voltage range: 2.7V to 5.5V
- 0.3%-100% PWM dimming at 10kHz – 100kH
- Support 0.3% PWM dimming with high accuracy
- 1MHz Boost switching frequency
- Support up to 9 LEDs in series
- 200mV voltage reference for LED current sensing
- 90% high efficiency for 4P5S LED connection
- 250uA quiescent current ($V_{FB}$=1V)
- Internal loop compensation
- Protections
  - Soft-start
  - Input under-voltage lockout (UVLO)
  - Boost cycle-by-cycle current-limit protection
  - 33V over-voltage protection against LED open fault
  - Thermal shutdown protection
- Packaging
  - DFN2x2x0.75mm - 6L
  - SOT23-6
  - RoHS compliant and halogen free
  - 100% lead (Pb) free

## Applications

- Smart phones
- Portable devices with LED display
- Portable media players

## General Description

The LP3323 is a white LED driver for LED backlighting applications. A Boost converter is built in to step up output voltage up to 33V to drive up to 9 LEDs in series. The high-efficiency Boost converter runs at 1MHz allowing low-profile inductor and ceramic capacitors.

The white LED current is programmed with a resistor connected at FB pin. The voltage at FB pin is regulated at 200mV at full scale. A PWM signal can be applied to CTRL pin to adjust DC voltage at FB pin and thus program LED current without generating audible noise. LP3323 supports 0.3%-100% PWM dimming at wide frequency range between 10kHz and 100kHz with high accuracy of regulation.

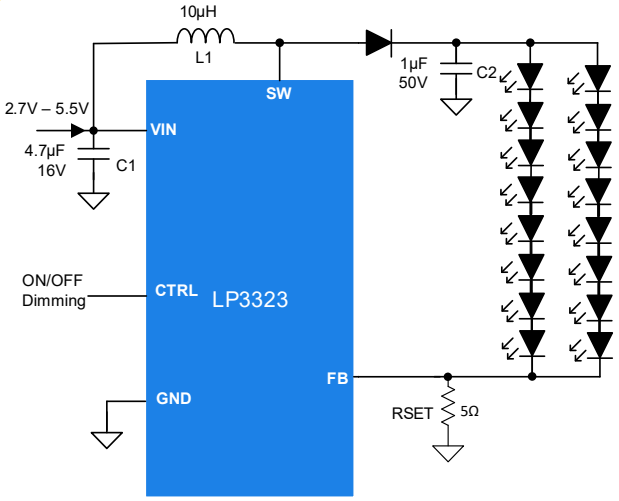
LP3323 offers low noise, small size, high efficiency and robust protections. The protection features include under-voltage lockout (UVLO), internal soft-start, Boost cycle-by-cycle current limit, output over-voltage protection for LED open fault as well as thermal shutdown. The LP3323 is available in a low-profile space-saving DFN2x2x0.75 6-lead package and SOT23-6 package.

## Order Information

LP3323 □□ □

- F: Pb-Free
- Package Type
  - QV: DFN-6L
  - B6: SOT23-6L

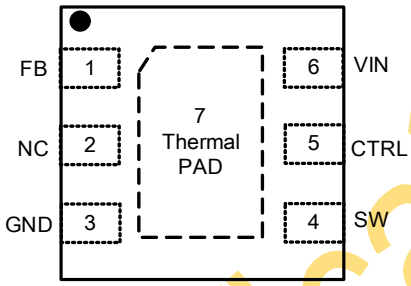
## Typical Application Circuit



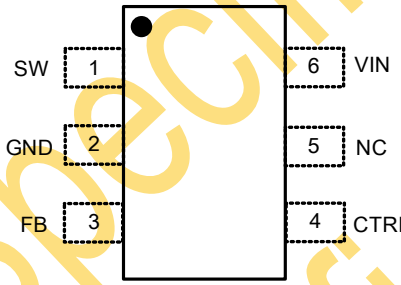
## Device Information

| Part Number | Top Marking | Package | Moisture Sensitivity Level | Shipping |
|---|---|---|---|---|
| LP3323QVF | LPS<br>FoYW | DFN2x2-6L | MSL3 | 4K/REEL |
| LP3323B6F | LPS<br>FoYWX | SOT23-6L | MSL3 | 3K/REEL |
| Marking indication: Y: Year code. W: Week code. X: Batch numbers. | | | | |

## Pin Diagram




DFN2x2-6L (Top View)




SOT23-6L (Top View)

## Pin Description

| Pins DFN | Pins SOT23 | Name | Description |
|---|---|---|---|
| 1 | 3 | FB | Current feedback input. Connect LED current sense resistor $R_{SET}$ from FB pin to GND. |
| 2 | 5 | NC | No connection. |
| 3 | 2 | GND | Ground. |
| 4 | 1 | SW | Switching node. Connect this pin to a terminal of Boost input inductor. This pin is also used to sense the LED output voltage for protection against LED open fault. |
| 5 | 4 | CTRL | Enable and PWM dimming input. |
| 6 | 6 | VIN | Supply input. Connect a 4.7μF ceramic capacitor from this pin to GND. |
| 7 | N/A | Thermal PAD | Thermal pad and ground. The exposed thermal pad must be connected to PCB ground to provide both electrical contact and rated thermal performance. Ground layers are connected to thermal pad through vias under thermal pad. |

## Absolute Maximum Ratings (Note)

VIN, FB, CTRL Voltage to GND ---------- -0.3V to 6V
SW Voltage to GND ---------- -0.3V to 35V
Maximum Junction Temperature (Tj) ---------- 150℃
Operation Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range---------- -60℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec)---------- 260℃

**Note**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Ratings

HBM (Human Body Model) ---------- +/-2kV
MM (Machine Model) ---------- +/-200V
CDM (Charge Discharge Model) ---------- +/-500V

## Thermal Information

$\theta_{JA}$ (Junction-to-Ambient Thermal Resistance) for DFN2x2 ---------- 82℃/W

## Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VIN | Input Voltage | 2.7 | | 5.5 | V |
| ILED | LED Output Current | | | 260(1) | mA |
| VOUT | LED Output Voltage | VIN+1V | | 31 | V |
| TJ | Operating Junction Temperature Range (TJ) | -40 | | 125 | ℃ |
| TA | Ambient Temperature Range | -40 | | 85 | ℃ |
| L | Boost Inductance | 7 | 10 | 26 | μH |
| CIN | Input Capacitance (2) (3) | 1.4 | 4.7 | 26.4 | μF |

**Notes:**
(1) The output current is also limited by the Boost input current limit and thermal performance
(2) The values recommended in the table are effective inductance and capacitance.
(3) X7R or X5R 10V (or 16V) voltage rating capacitors are recommended
(4) X7R or X5R 50V voltage rating capacitors are recommended

## Electrical Characteristics

(The specifications are at $V_{IN}$=3.7V and Tj=25 except otherwise specified)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| INPUT VOLTAGE AND CURRENT | | | | | | |
| $V_{IN}$ | Input Voltage Range | | 2.7 | | 5.5 | V |
| $I_{SHDN}$ | Input Supply Current | EN disabled | | | 1 | μA |
| $V_{IN\_UVLO}$ | Under Voltage Lockout of $V_{IN}$ | $V_{IN}$ Rising | 2.35 | 2.44 | 2.55 | V |
| $V_{IN\_UVLO\_HYS}$ | $V_{UVLO}$ Hysteresis | $V_{IN}$ Falling | | 250 | | mV |
| $I_{SD}$ | Shutdown current | $V_{CTRL}$ = 0 for > 2.5ms | | | 1 | μA |
| $I_Q$ | Quiescent current | $V_{FB}$ = 1.2V | | 250 | | μA |
| BOOST CONVERTER | | | | | | |
| $F_{SW}$ | Switching Frequency | | | 1.0 | | MHz |
| $I_{LIM}$ | Switch Current Limit | | | 1.5 | | A |
| $D_{MAX}$ | Maximum Duty Cycle | | | 92 | | % |
| $R_{DSON\_LS}$ | Low-side MOSFET On-resistance | | | 0.25 | | Ω |
| $V_{OVP1}$ | SW Over-voltage Protection | | 31.5 | 33 | 34.5 | V |
| $V_{FB\_LOW}$ | FB voltage low | VFB falling | | 33 | | mV |
| $V_{FB\_LOW}$ | FB voltage low | VFB rising | | 50 | | mV |
| $V_{FB\_REF}$ | FB Reference Voltage | 100% PWM duty cycle | 194 | 200 | 206 | mV |
| $V_{FB\_REF\_PWM}$ | FB Reference Voltage Under PWM Dimming | 10% PWM duty cycle | 19.3 | 20 | 20.6 | mV |
| | | 1% PWM duty cycle, $V_{IN}$ = 2.7V – 4.5V | 1.85 | 2.1 | 2.35 | mV |
| | | 0.3% PWM Duty, $V_{IN}$ = 2.7V – 4.5V | | 0.7 | | mV |
| $T_{SOFT\_START}$ | Soft-start Time | | | 3 | | ms |

## Electrical Characteristics (Continued)

(The specifications are at $V_{IN}$=3.7V and $T_J$ = 25°C for typical values unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| PWM CONTROL | | | | | | |
| $T_{OFF}$ | CTRL Shutdown Deglitch time | CTRL high to low | 2.5 | | | ms |
| $T_{REF}$ | VREF_FB Filter Time Constant | | | 400 | | μs |
| $f_{CTRL}$ | PWM Dimming Frequency | | 10 | | 100 | kHz |
| $D_{PWM}$ | PWM Dimming Duty Cycle | | 0.3 | | 100 | % |
| $t_{MIN\_ON}$ | PWM minimum on time | | | 30 | 50 | ns |
| LOGIC I/O | | | | | | |
| $V_{CTRL\_HIGH}$ | CTRL Logic High | VIN=2.7V to 5.5V | 1.4 | | | V |
| $V_{CTRL\_LOW}$ | CTRL Logic LOW | VIN=2.7V to 5.5V | | | 0.4 | V |
| $R_{CTRL}$ | CTRL Pull Down Resistor | | | 600 | | kΩ |
| THERMAL SHUTDOWN PROTECTION | | | | | | |
| $T_{SHUT}$ | Thermal Shutdown | Temperature Rising | | 140 | | ℃ |
| $T_{SHUT\_HYST}$ | Thermal Shutdown Hysteresis | Temperature Falling | | 20 | | ℃ |

## Typical Characteristics

(L1=10μH, C1=4.7μF, C2=1μF and $T_J$ = 25°C unless otherwise noted and the schematic and BOM is as shown in Figure 15)

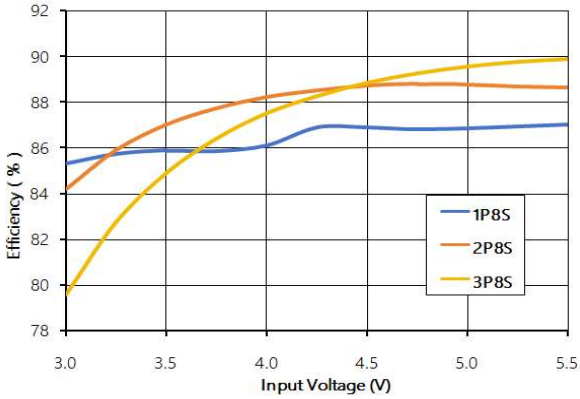



Figure 1. Efficiency vs. Input Voltage
(L1: 2.5mmx2.0mmx1.2mm, DCR=480mΩ)

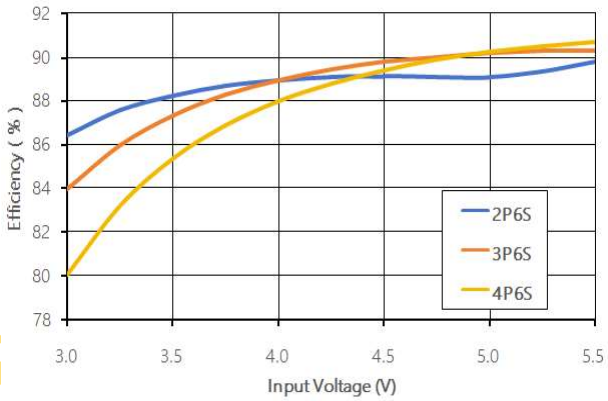



Figure 2. Efficiency vs. Input Voltage
(L1: 2.5mmx2.0mmx1.2mm, DCR=480mΩ)

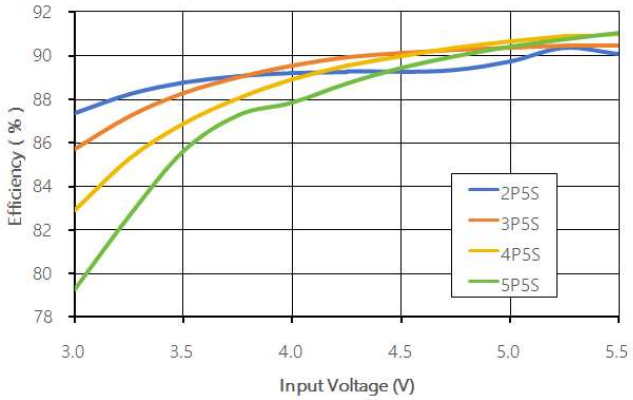



Figure 3. Efficiency vs. Input Voltage
(L1: 2.5mmx2.0mmx1.2mm, DCR=480mΩ)

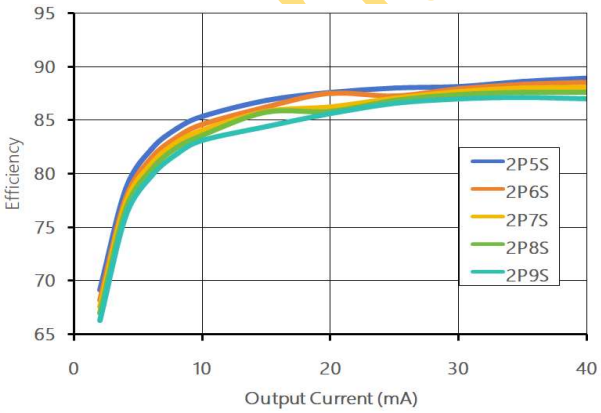



Figure 4. Efficiency vs. Output Current
($V_{IN}$=3.7V, L1: 2.5mmx2.0mmx1.2mm, DCR=480mΩ)

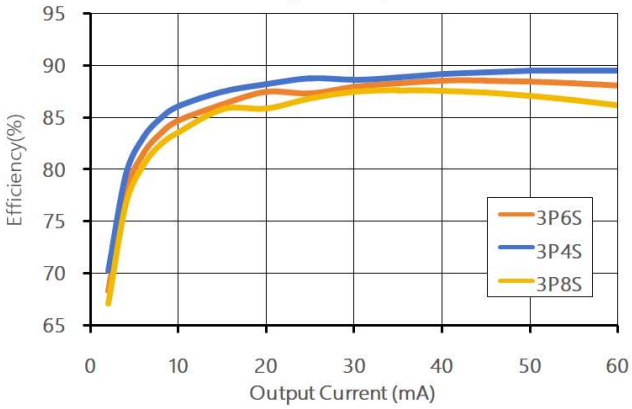



Figure 5. Efficiency vs. Output Current
($V_{IN}$=3.7V, L1: 2.5mmx2.0mmx1.2mm, DCR=480mΩ)

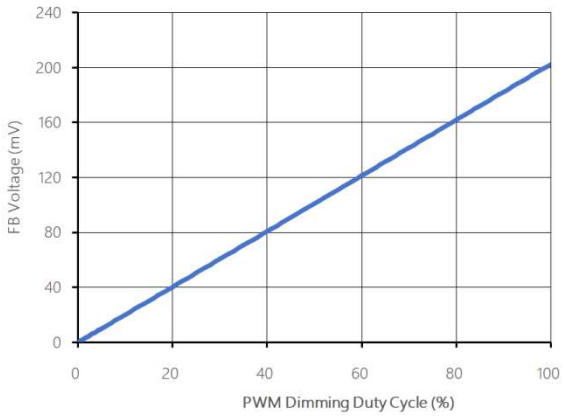



Figure 6. FB Voltage vs. PWM Dimming Duty Cycle

## Typical Characteristics

(L1=10μH, C1=4.7μF, C2=1μF and $T_J$ = 25°C unless otherwise noted and the schematic and BOM is as shown in Figure 15)

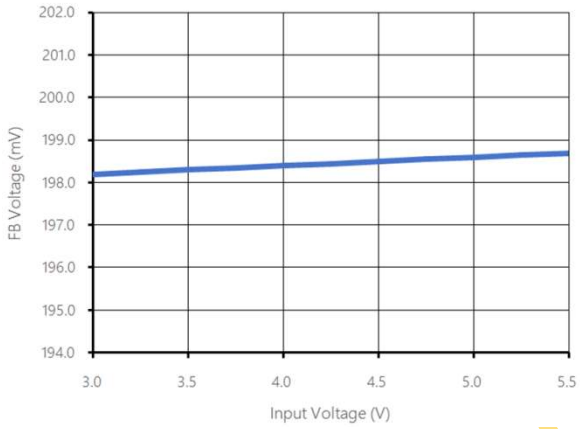



Figure 7. FB Voltage vs. Input Voltage (PWM Dimming Duty = 100%)

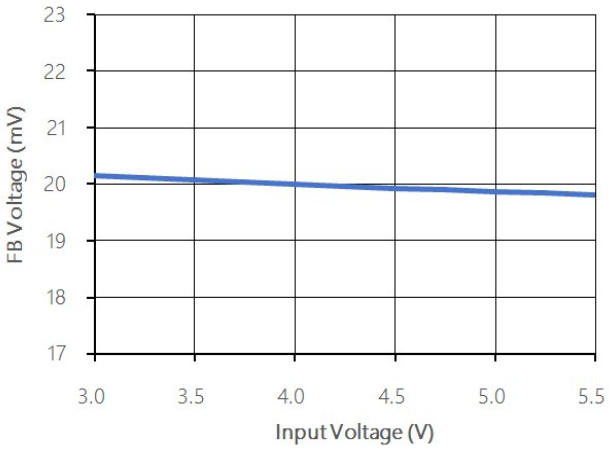



Figure 8. FB Voltage vs. Input Voltage (PWM Dimming Duty = 10%)

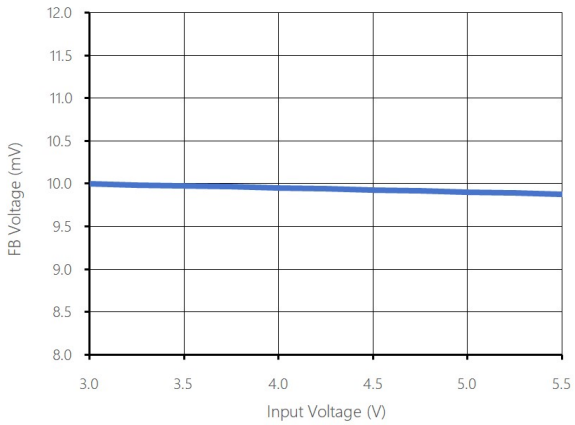



Figure 9. FB Voltage vs. Input Voltage (PWM Dimming Duty = 5%)

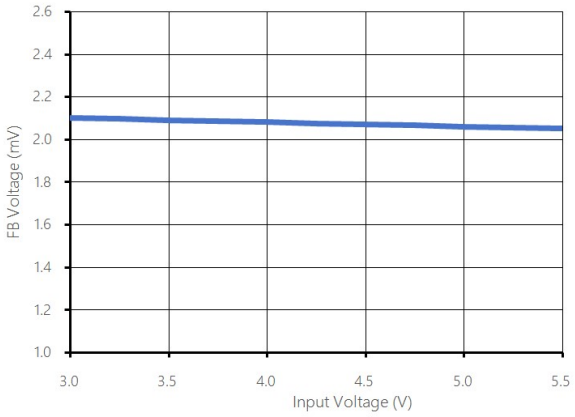



Figure 10. FB Voltage vs. Input Voltage (PWM Dimming Duty = 1%)

## Typical Characteristics

(L1=10μH, C1=4.7μF, C2=1μF and $T_J$ = 25°C unless otherwise noted and the schematic and BOM is as shown in Figure 15)

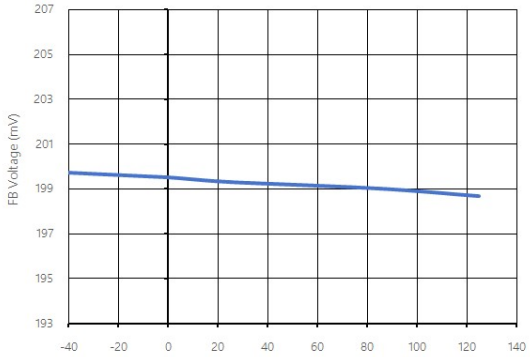



Figure 11. FB Voltage vs. Junction Temperature
($V_{IN}$=3.7V, PWM Dimming Duty = 100%)

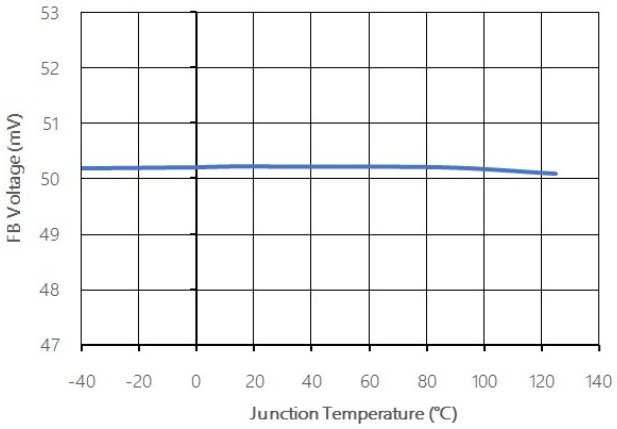



Figure 12. FB Voltage vs. Junction Temperature
($V_{IN}$=3.7V, PWM Dimming Duty = 25%)

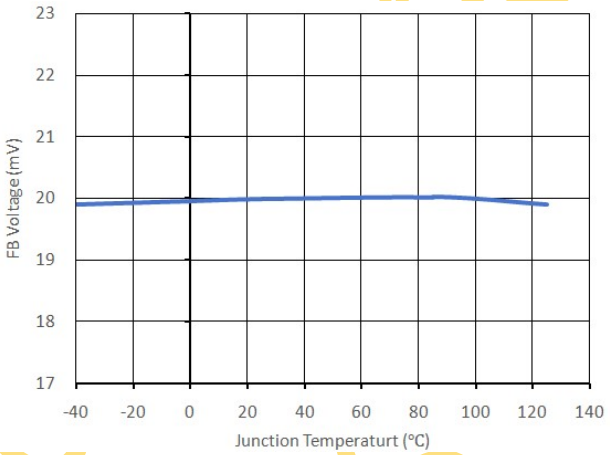



Figure 13. FB Voltage vs. Junction Temperature
($V_{IN}$=3.7V, PWM Dimming Duty = 10%)

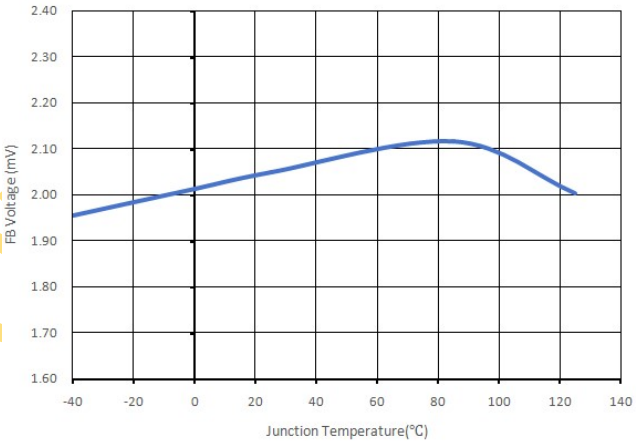
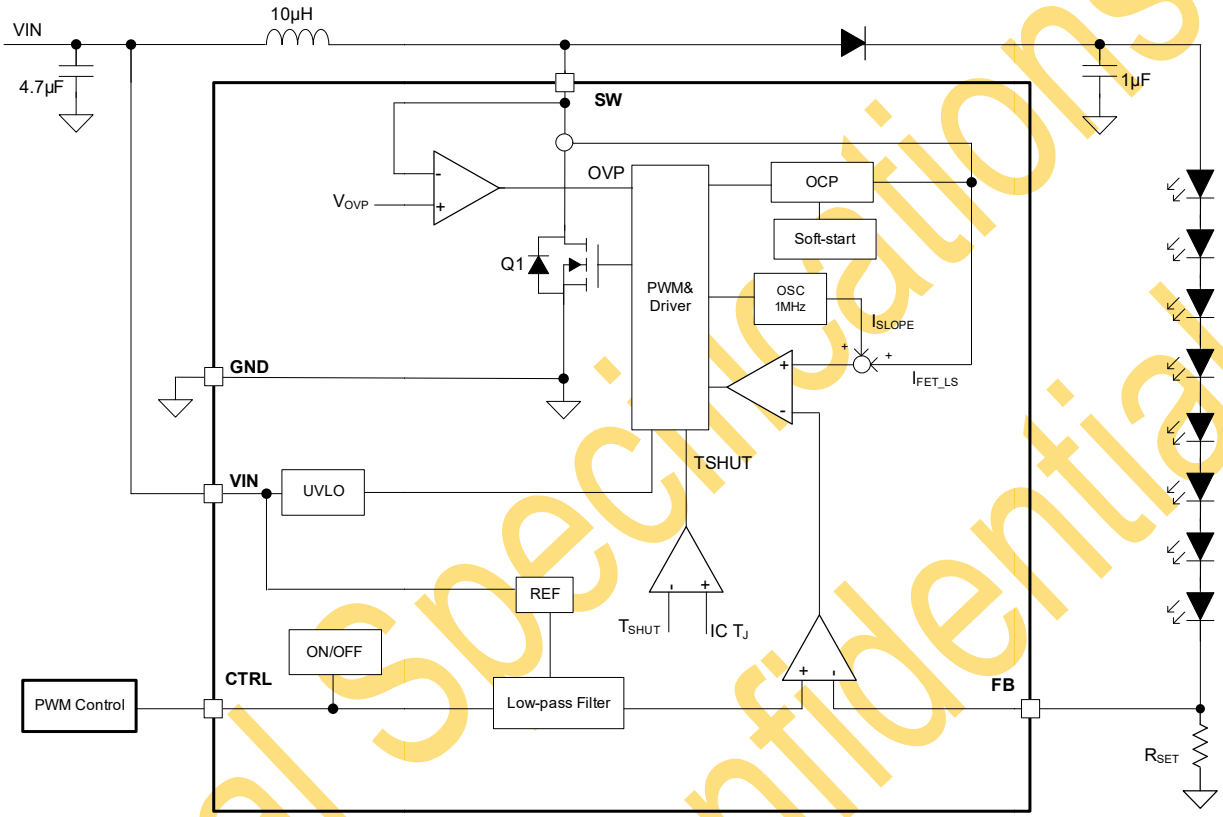



Figure 14. FB Voltage vs. Junction Temperature
($V_{IN}$=3.7V, PWM Dimming Duty = 1%)

## Functional Block Diagram



# Detailed Description

## Overview

The LP3323 is a high-efficiency high-output-voltage Boost LED driver. The serial LED connection provides even illuminations by sourcing the same output current through LEDs in series. The device integrates Boost converter high voltage low-side NFET that operates in pulse width modulation (PWM) to regulate output FB voltage at a reference voltage adjustable by PWM dimming input at CTRL pin. The LED current is sensed by the current sensing resistor $R_{SET}$ and fed back to FB pin. The voltage at FB pin is regulated at reference voltage that is dimmable by PWM control input at CTRL pin. Under 100% duty cycle at CTRL input, the FB pin is regulated at 200mV. The LED current can be dimmed by a PWM input, the FB pin voltage is regulated at 200mV * (PWM duty cycle). LP3323 also supports multiple strings of LEDs in parallel and the combined string LED current is fed back to FB pin and therefore the LED current is programmable by $R_{SET}$ and dimmable by PWM duty cycle.

## Under Voltage Lockout (UVLO)

The LP3323 integrates an under-voltage lockout block (UVLO) that enables the device after the voltage on the VIN pin exceeds the UVLO threshold. The device is disabled as soon as the VIN voltage falls below the UVLO falling threshold.

## Soft Startup

When the device is enabled, the over current protection limit increases to full scale in a specific time, which prevents input rush current and LED current output voltage from overshooting.

## Boost Converter

The LP3323 integrates a PWM non-synchronous Boost converter operating with peak current mode control. Schottky diode is added externally from SW pin to an output capacitor. The LED current is fed back to an error amplifier (E/A) by FB pin and the E/A output is sent to PWM modulation to determine the Boost duty cycle. Slope compensation is implemented to eliminate sub-harmonic oscillation at high duty cycle (D>0.5).

## Over Current Protection

The LP3323 integrates a cycle-by-cycle over current protection. Once the inductor peak current hits the over current limit, the low-side MOSFET turns off immediately for the rest of the cycle. During the soft-start time, the cycle-by-cycle over current limit ramps up into full scale.

## Open LED Protection

At FB pin open or short to ground, the feedback voltage at FB pin falls to ground level causing output voltage of the E/A goes up and Boost duty cycle increase. As a result, the LED output voltage goes up until it hits the over voltage protection threshold. The LED output voltage is detected from SW pin when NFET switch is off. When the NFET turns on, the voltage at SW pin is pulled to ground, and inductor is charged by the input voltage. Once the NFET turns off, the inductor current is discharged to the LED through the external schottky diode and the voltage at SW pin reflect the LED output voltage as $V_{SW} = V_{LED}+V_F$. If the LED voltage detected at SW pin is over the OVP threshold $V_{OVP}$ for 4 times, the Boost converter latches off. The Boost converter is re-enabled under either of the two conditions:

- VIN is recycled
- CTRL pin is pulled low for > $T_{OFF}$ and re-enabled

## Shutdown

The CTRL pin is used for device enabling, shutdown and PWM dimming. If CTRL pin voltage is from high to low for more than $T_{OFF}$, the device shuts down.

## Thermal Shutdown Protection

The LP3323 device enters over temperature protection and shuts down if its junction temperature exceeds $T_{SHUT}$. Once the junction temperature falls below the hysteresis threshold, the device restarts.

## Application Information

The LP3323 device can be used to drive 3 to 9 LEDs in series and 1 to 6 strings in parallel. The total number of LED is limited by cycle by cycle current and thermal limit. The LED current is programmable by a current sensing resistor connected from FB pin to ground. ON/OFF control and/or PWM dimming can be implemented by connecting a control signal to CTRL pin.

### PWM Brightness Dimming

If CTRL pin is constantly pulled high, the FB pin voltage is regulated to 200mV. If a PWM signal with a fixed duty cycle (D) is applied to CTRL pin, the FB voltage is regulated at $V_{FB}$ = 200mV * D. The corresponding LED current is equal to $V_{FB}$ / $R_{SET}$. The allowed PWM signal frequency is 10kHz to 100kHz.

### LED Current Setting

The LED current is set by a resistor RSET connected from FB to ground. The full scale LED current with 100% duty cycle or CTRL pin constantly pulled high is: ILED = 200mV / $R_{SET}$, where $R_{SET}$ is the resistor resistance between FB pin to ground.

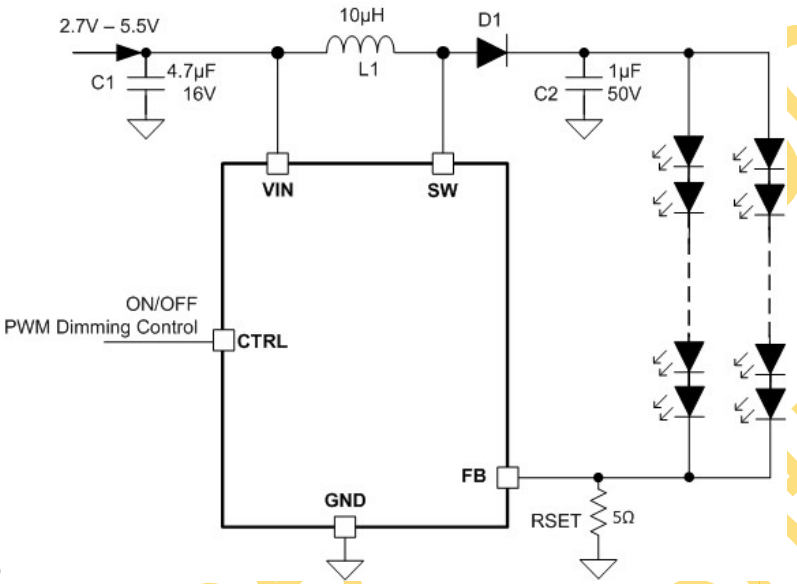
### Inductor Selection

A 10μH inductor is recommended for typical applications. If less than total 10 LEDs (including parallel and series) are used, a 20μH inductor is recommended to reduce inductor current ripple for higher efficiency.

### Capacitor Selection

A 4.7μF or higher values of low ESR ceramic capacitors are recommended for Boost input capacitor, and 1μF or higher values of low ESR ceramic capacitors are recommended for Boost output capacitor as shown in the table of Recommended Operating Conditions.

## Application Schematic

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| Designator | Values | Part Number(s) | Manufacturer | Package Size | Specifications |
|---|---|---|---|---|---|
| C1 | 4.7μF ±10% | 0402ZD475KAT2A | Murata | 0402 | 10V Ceramic, X5R |
| D1 | 40V/1A | STPS140Z | ST | SOD-123 | Schottky 40V/1A |
| | 40V/1A | CUS10S40 | Toshiba | SOD-123 | Schottky 40V/1A |
| C2 | 1.0μF ±15% | C1608X5R1H105K080AB | TDK | 0603 | 50V Ceramic, X5R |
| | 1.0μF ±20% | GRT188R61H225ME13 | MuRata | 0603 | 50V Ceramic, X5R |
| L1 | 10 μH ±30% | DFE252010C | Toko | 2.5x2.0x1.0 | Irate=1.1A, DCR=689mΩ |
| | 10 μH ±30% | BWMR00252012100 | Hilisin | 2.5x2.0x1.2 | Irate=1.0A, DCR=480mΩ |
| | 10 μH ±30% | 0410CDMCCDS-100MC | Sumida | 4.4x4.2x0.8 | Irate=1.4A, DCR=318mΩ |

Figure 15.Typical Backlight Application

## Application and Implementation

### Application Curves

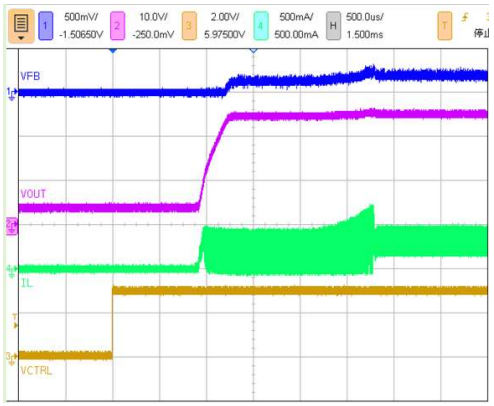



Figure 16. Startup

($V_{IN}$=3.7V, PWM Dimming Duty = 100%)

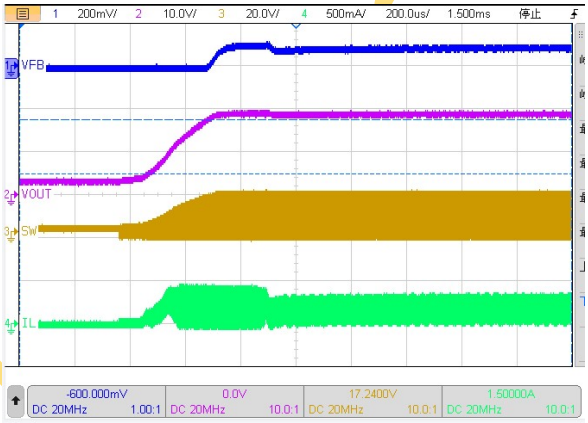



Figure 17. Startup

($V_{IN}$=3.7V, PWM Dimming Duty = 40%)

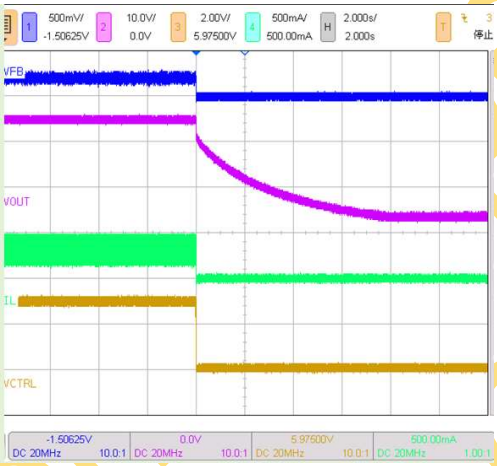



Figure 18. Shutdown

($V_{IN}$=3.7V, PWM Dimming Duty = 100%)

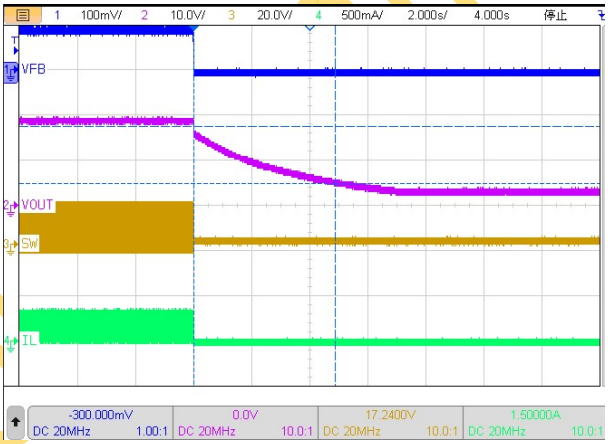



Figure 19. Shutdown

($V_{IN}$=3.7V, PWM Dimming Duty = 40%)

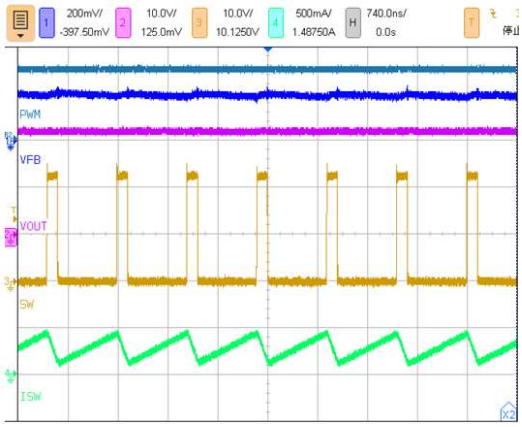



Figure 20. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 100%)

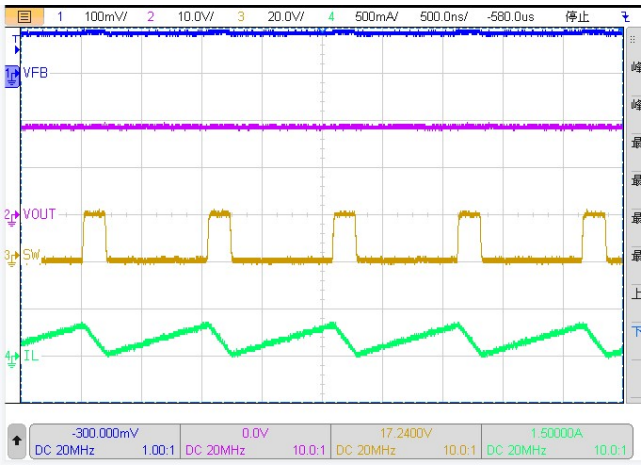



Figure 21. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 40%)

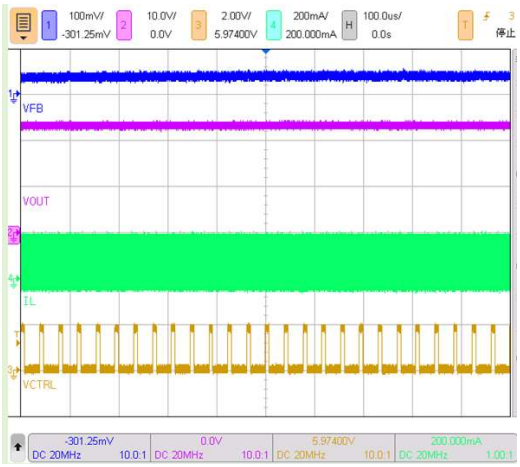



Figure 22. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 20%)

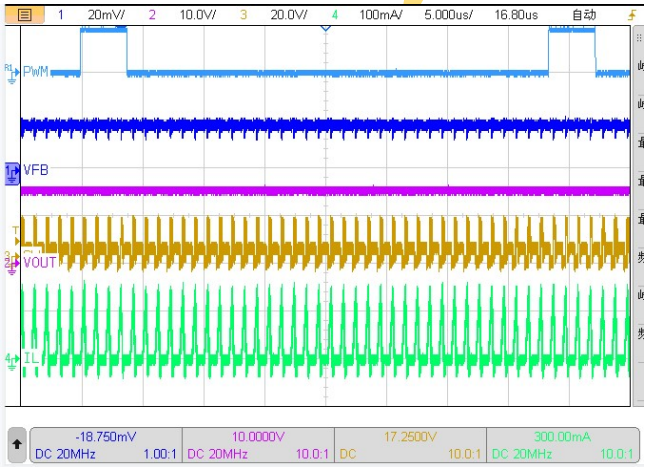



Figure 23. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 10%)

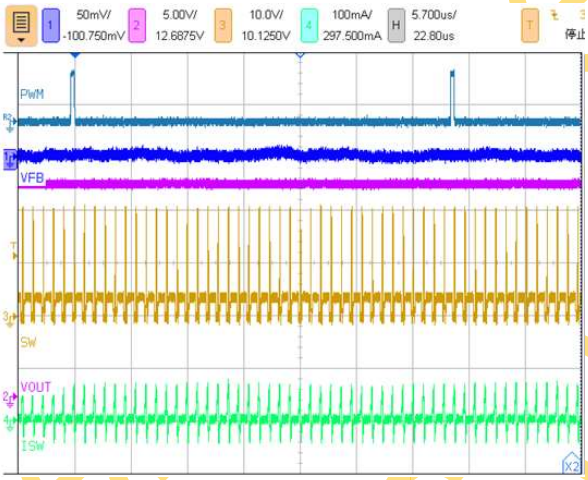



Figure 24. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 1%)

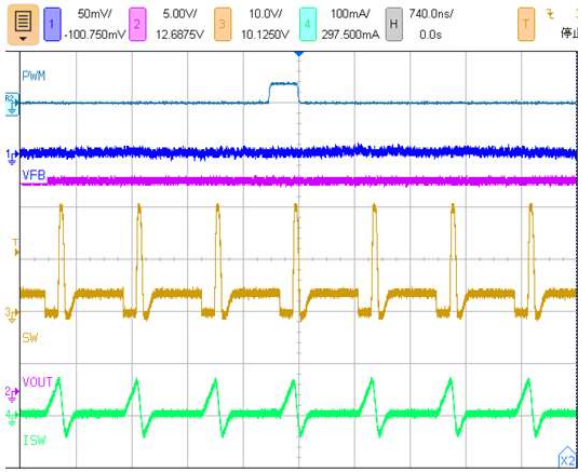



Figure 25. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 1%)

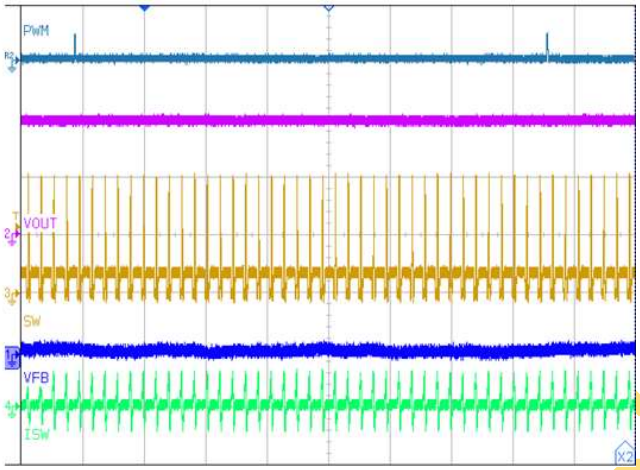



Figure 26. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 0.3%)

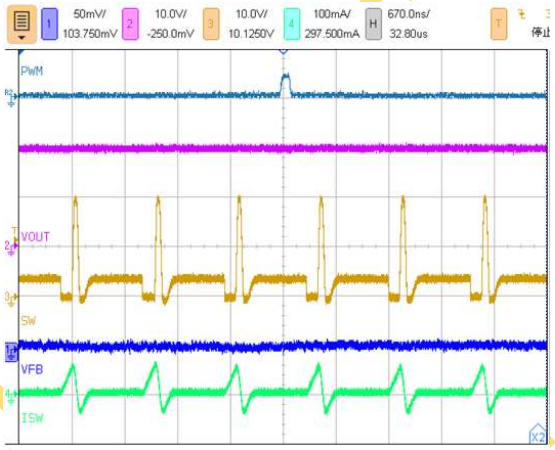



Figure 27. Steady state

($V_{IN}$=3.7V, PWM Dimming Duty = 0.3%)

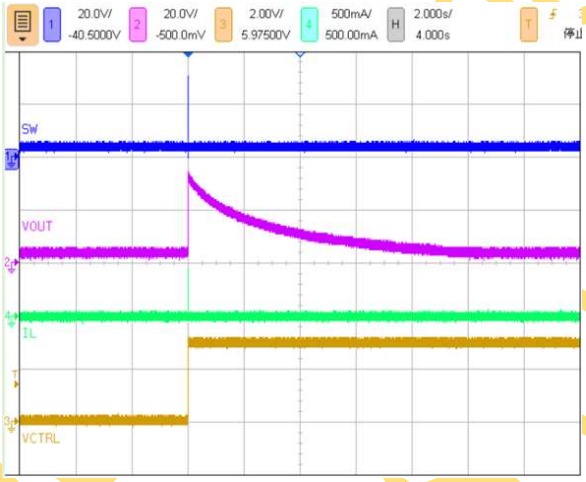



Figure 28. Startup with FB pin open

($V_{IN}$=3.7V, PWM Dimming Duty = 100%)

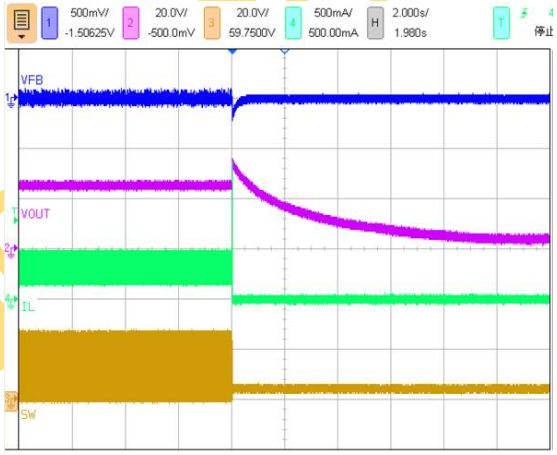



Figure 29. LED open during operation

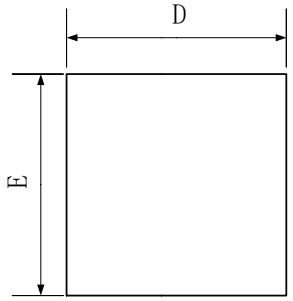
($V_{IN}$=3.7V, PWM Dimming Duty = 40%)

## PCB Layout Guideline

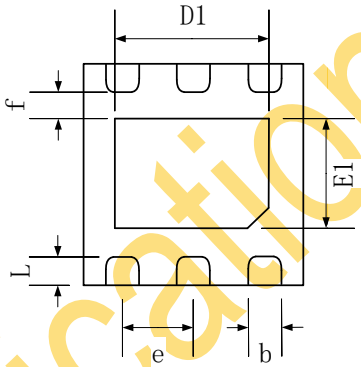
Appropriate PCB layout is important in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. The following design considerations are recommended:

- Input and output capacitors are replaced closed to the IC and connected to ground plane to reduce noise coupling
- Connect IC GND pad to the ground plane on the bottom side with multiple vias that is for both heat dissipation and electrical connection.
- Minimize switching SW node size and trace lengths and keep it away from RSET.
- Place feedback resistor RSET close to the IC and keep it away from noisy trace and components.

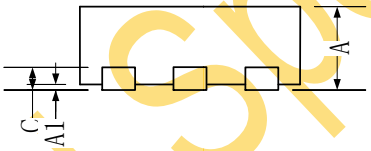
## Package Information (DFN2x2-6L)



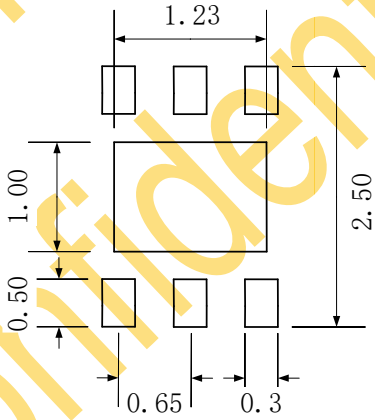

TOP VIEW




BOTTOM VIEW



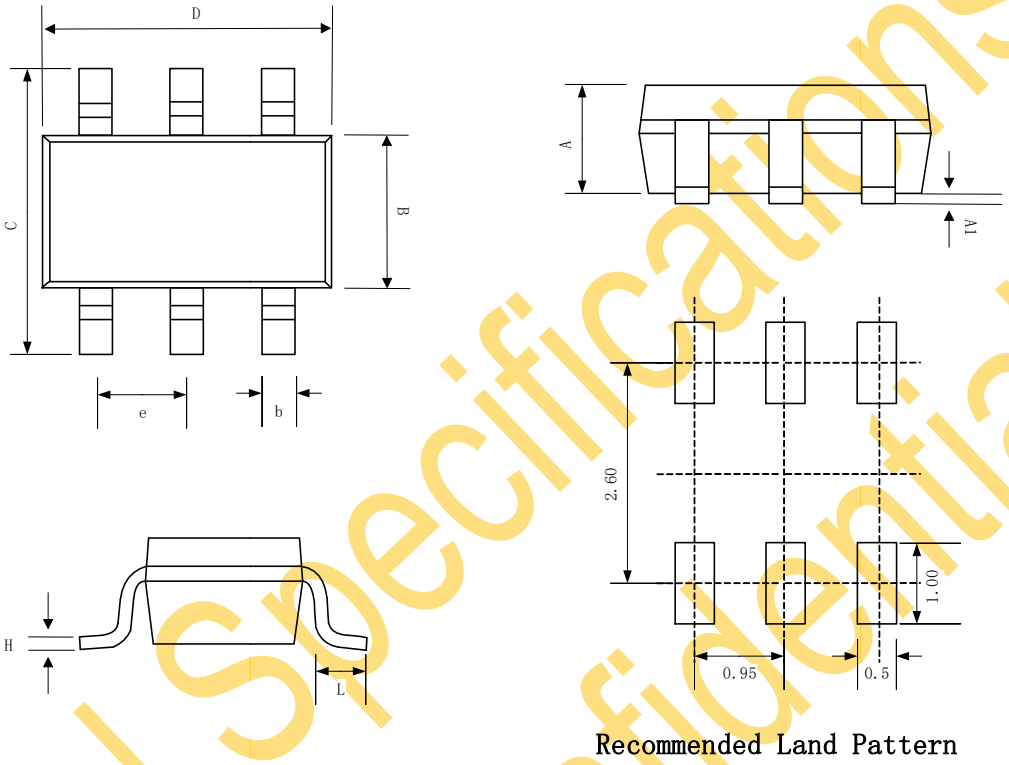

SIDE VIEW




Recommended Land Pattern

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.22 | 0.30 | 0.35 |
| c | 0.18 | 0.20 | 0.25 |
| D | 1.90 | 2.00 | 2.10 |
| D1 | 1.00 | 1.23 | 1.70 |
| E | 1.90 | 2.00 | 2.10 |
| E1 | 0.50 | 0.70 | 1.10 |
| e | 0.65 BSC | | |
| L1 | 0.20 | 0.30 | 0.40 |
| f | 0.20 | - | - |

Package Information (SOT23-6L)

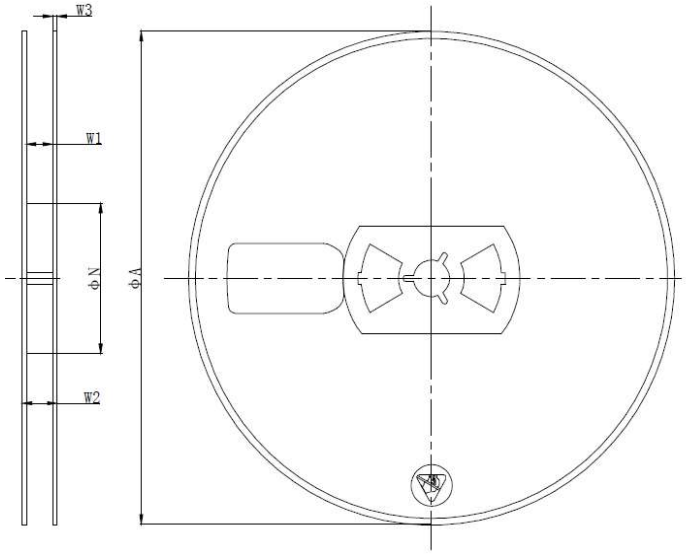



Recommended Land Pattern

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.889 | 1.100 | 1.295 |
| A1 | 0.000 | 0.050 | 0.152 |
| B | 1.397 | 1.600 | 1.803 |
| b | 0.28 | 0.35 | 0.559 |
| C | 2.591 | 2.800 | 3.000 |
| D | 2.692 | 2.920 | 3.120 |
| e | 0.95BSC | | |
| H | 0.080 | 0.152 | 0.254 |
| L | 0.300 | 0.450 | 0.610 |

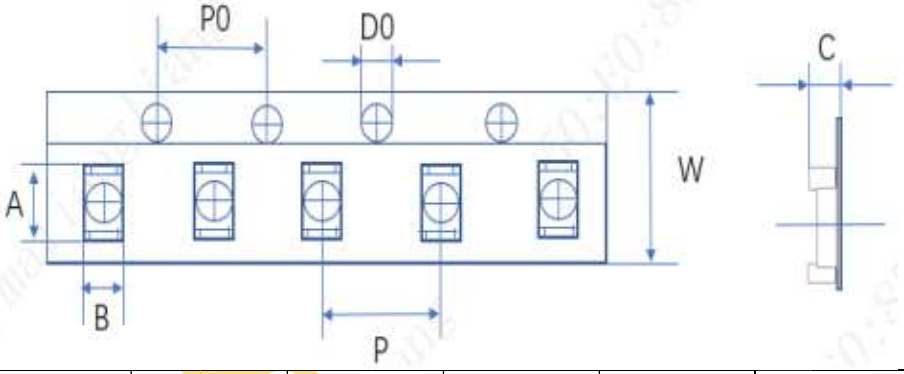
## Carrier Information

Reel Dimensions (Unit: mm)



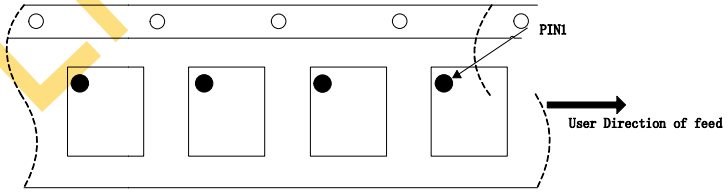

| Device | ΦA | W2 |
|---|---|---|
| LP3323QVF | 180±4 | 12±3 |
| LP3323B6F | 180±4 | 12±3 |

Tape Dimension (Unit: mm)




| Device | A | B | P0 | P | D0 | W | C |
|---|---|---|---|---|---|---|---|
| LP3323QVF | 2.15±0.30 | 2.15±0.30 | 4.00±0.20 | 4.00±0.20 | 1.50±0.20 | 8.00±0.30 | 1.00±0.20 |
| LP3323B6F | 3.20±0.30 | 3.26±0.30 | 4.00±0.20 | 4.00±0.20 | 1.50±0.20 | 8.00±0.30 | 1.40±0.20 |

DFN-6L




SOT23-6L