LP5307AQVF

28V/5A Over-Voltage Protection Switch with Integrated TVS

Features

- Input voltage range 3V to 28V
- Low on-state resistance to 40mΩ
- 80μA low current consumption
- Programmable Over-Voltage Lockout
  - External Adjustable via OVLO
  - Default 6.8V with grounded OVLO
- Under-voltage lockout: 2.7V
- OVP threshold adjustable range: 4V to 25V
- Active-low Enable Control
- Ultra-fast OVP Response Time: <50ns
- Open-drain Power-OK Indicator
- Thermal shutdown protection
- Integrated TVS on IN (±80V Surge)
- ESD Protection:
  - Human Body Model: 4kV
  - Charged Device Model: 0.5kV
- Package: DFN-8, 2mm x 3mm

Applications

- Notebook and PC
- Cell phone and PDAs
- USB or other peripheral ports
- Camera

General Description

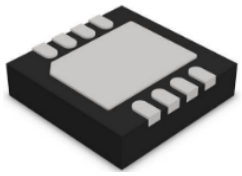
The LP5307A is an OVP power switch device provides full protection to systems and loads which may encounter input over-voltage conditions.

The device contains a 40mΩ MOSFET which can operate over an input voltage range from 3.0V to 28V. It can support maximum continuous current up to 5A.

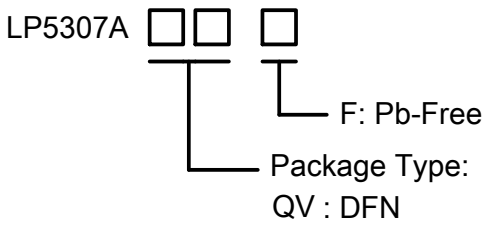
The OVP will disconnect IN and OUT when the voltage on IN is higher than over voltage threshold. The device is controlled by an active-low logic pin. Thermal shutdown protection is integrated which shuts off the switch to prevent damage to the part when the temperature is higher than threshold.

The input of LP5307A has internal TVS integrated. It can handle up to ±80V surge event based on IEC61000-4-5.

These parts are available in space-saving wafer level package DFN-8.



Marking Information



Ordering and Package Information

Part Number	Top Mark	Package	T&R
LP5307AQVF	LPS 5307A YWX	DFN-8	4K/REEL
Marking indication: Y: Production Year, W: Production week, X: Series Number			

Typical Application Circuitry

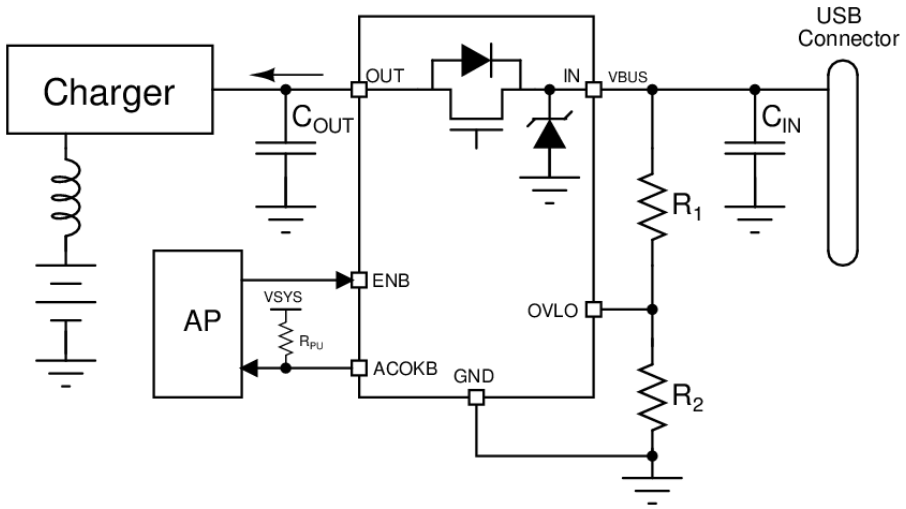
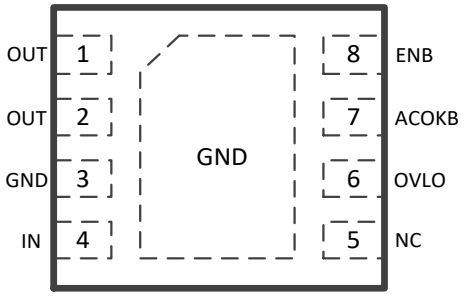


Figure 1. Typical Application Circuitry

Pin Configuration



DFN-8 (Top View)

Pin Description

Pin	Description
GND	Ground
IN	Power supply and input of power switch
OUT	Output of power switch
ACOKB	Open-drain Power Good indicator
ENB	Active-low device enable pin
OVLO	Over-Voltage Lockout adjustment pin
NC	Not connected

Functional Block Diagram

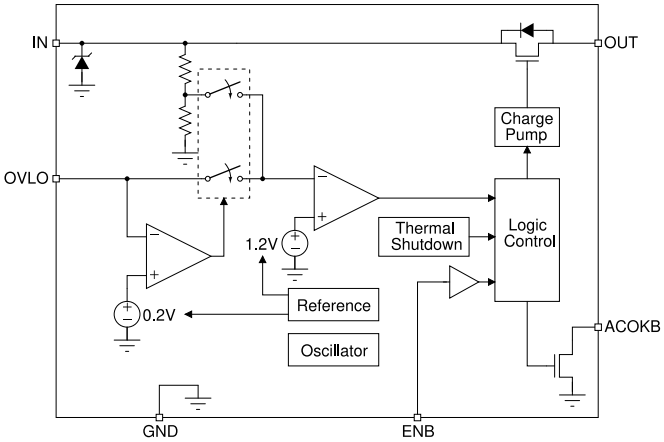


Figure 2. Internal Block Diagram

Absolute Maximum Ratings

- IN to GND ---------- -0.3V to +29V
- OUT to GND ---------- -0.3V to V_{IN} + 0.3V
- ENB to GND ---------- -0.3V to +7V
- OVLO to GND ---------- -0.3V to +7V
- ACOKB to GND ---------- -0.3V to +7V
- Maximum Junction Temperature (T_A) ---------- 150°C
- Maximum Soldering Temperature (at leads, 10 seconds) ---------- 260°C

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, instead of functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- Maximum Power Dissipation (T_A <= 25℃) ---------- 0.95W
- Thermal Resistance (θJA) (Note 2) ---------- 84.1°C/W

Note 2: It is based on 2S2P JEDEC standard PCB.

ESD Ratings

- HBM (Human Body Model, JEDEC JS-001) ---------- ±4000V
- CDM (Charged Device Model, JEDEC JS-002) ---------- ±500V

Recommended Operating Conditions

- Input Voltage ---------- 3.0V to 28V
- Output Voltage ---------- 0V to V_{IN}
- I/O (ENB, OVLO, ACOKB) Voltage ---------- 0V to 5.5V
- Input Capacitance ---------- 4.7μF
- Output Capacitance ---------- 1μF
- Ambient Temperature ---------- -40°C to 85°C

Electrical Characteristics

The following parameters are guaranteed under condition V_{IN} =5V, T_A = -40°C to 85°C unless otherwise noted. T_A = 25°C for typical value.

Parameters	Symbol	Test conditions	Min	Typ	Max	Unit
On-resistance	$R_{DS(ON)}$	V_{IN} = 5V, I_{OUT}=200mA, T_A=25°C		40		mΩ
Input quiescent current	I_Q	V_{IN} = 5V, OUT floating, V_{ENB} = 0V		65	130	μA
Input current at OVP condition	I_{IN_OVLO}	V_{IN} = 5V, V_{OVLO} = 1.4V, OUT grounded		70	140	μA
Input Surge protection level	V_{SURGE}	C_{IN} = 4.7μF, IEC61000-4-5 (8/20μs)		80		V
Under-Voltage Lockout level	V_{UVLO_F}	IN voltage falling	2.7	2.8		V
	V_{UVLO_R}	IN voltage rising		2.9	3.0	V
Default OVP level	V_{OVP}	IN voltage rising, V_{OVLO} = 0V		6.8		V
OVLO trigger level	V_{OVLO_TH}	OVLO voltage rising		1.2		V
OVLO hysteresis	V_{OVLO_HYS}			3		%
OVP default level threshold	V_{OVLO_SEL}	V_{IN} = 8V, OVLO level to trigger OVP	0.1		0.2	V
OVP level adjustable range	V_{OVP_RNG}		4		25	V
Over-Voltage Protection response time	t_{OVP}	V_{IN} rising from 5V with 30V/μs, R_{OUT} = 100Ω, C_{OUT} = 0, time from V_{IN} > V_{OVP} to OUT voltage stop rising		30	50	ns
Output auto discharge	R_{DIS}	V_{IN} = 5V, V_{EN} = 0V		3		kΩ
Enable logic high voltage level	V_{IH}	V_{IN} = 2.4V to 6V	1.4			V
Enable logic low voltage level	V_{IL}	V_{IN} = 2.4V to 6V			0.4	V
Load switch turned on delay	t_{DON}	V_{IN} = 5V, R_{OUT} = 100Ω, C_{OUT} = 22μF, time from enabled to V_{OUT} = 0.5		15		ms
Start-up time	t_{START}	V_{ENB} = 0V, R_{PU} = 10kΩ, time from V_{IN} > V_{UVLO_R} to ACOKB = 0		30		ms
Output rising time	t_R	V_{IN} = 5V, R_{OUT} = 100Ω, C_{OUT} = 22μF, time from V_{OUT} = 0.1×V_{IN} to 0.9×V_{IN}		1.2		ms
Load switch turned off delay	t_{OFF}	V_{IN} = 5V, R_{OUT} = 500Ω, C_{OUT} = 0.1μF, time from disabled to V_{OUT} = 0.9×V_{IN}		10		μs
Thermal shutdown trigger	T_{SD}	Temperature rising		150		°C
Thermal shutdown release	T_{SD_REL}	Temperature falling		130		°C

Note 3. The parameter is guaranteed by design and characterization.

Typical Timing Diagram

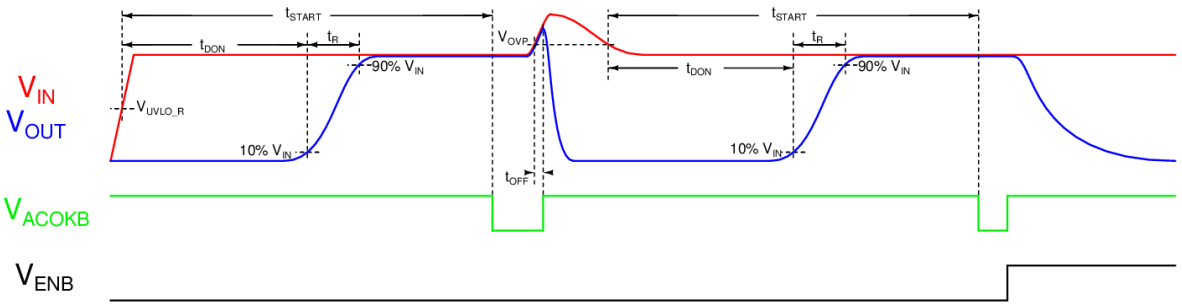


Figure 3. Start-up and over current protection

Typical Performance Characteristics

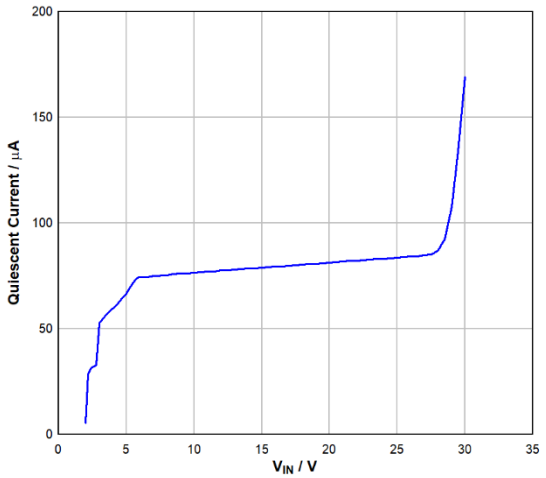


Figure 4. Quiescent Current vs V_{IN}
(V_{OVLO} = 1V, V_{ENB} = 0V, no load, T_A = 25°C)

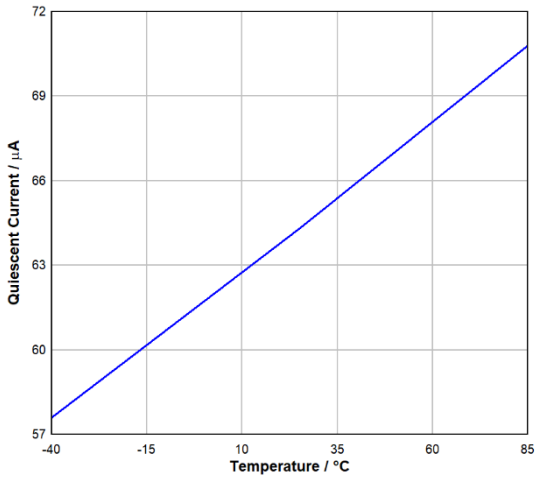


Figure 5. Quiescent Current vs Temperature
(V_{IN} = 5V, V_{OVLO} = 1V, V_{ENB} = 0V, no load)

Typical Operating Waveforms

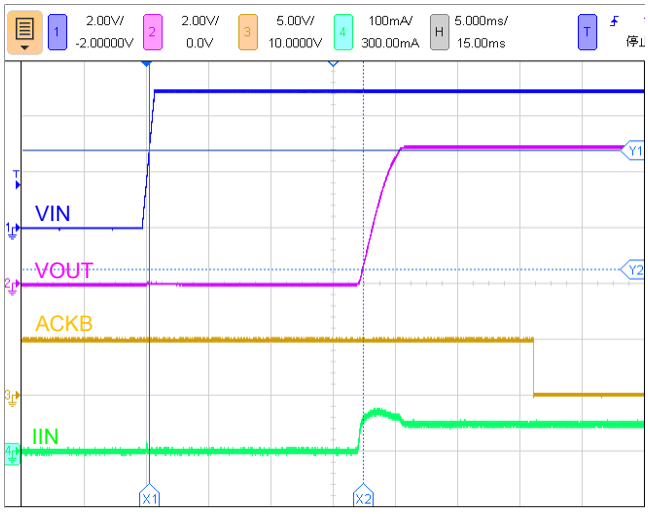


Figure 6. Start-up with VIN ramp-up
(V_{ENB} = 0V, C_{IN} = 1µF, C_{OUT} = 22µF, R_{LOAD} = 100Ω)

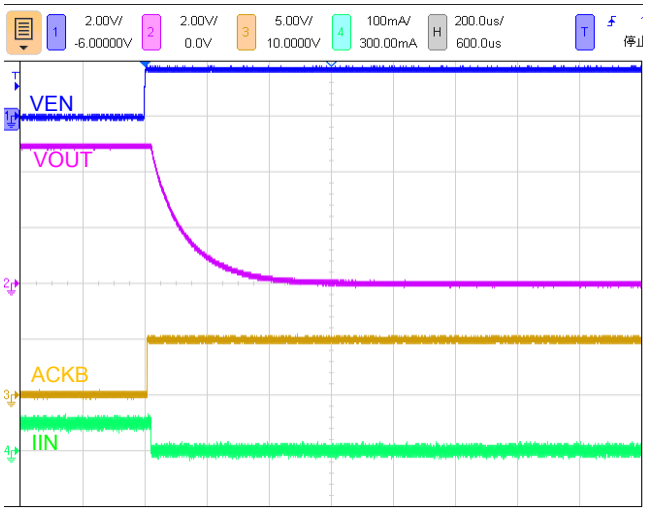


Figure 7. Disabled by ENB
(V_{IN} = 5V, C_{IN} = C_{OUT} = 1µF, R_{LOAD} = 100Ω)

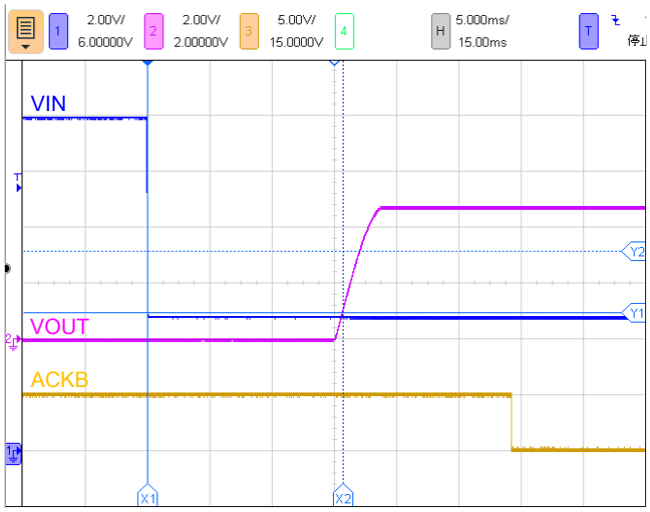


Figure 8. Recover from OVP condition

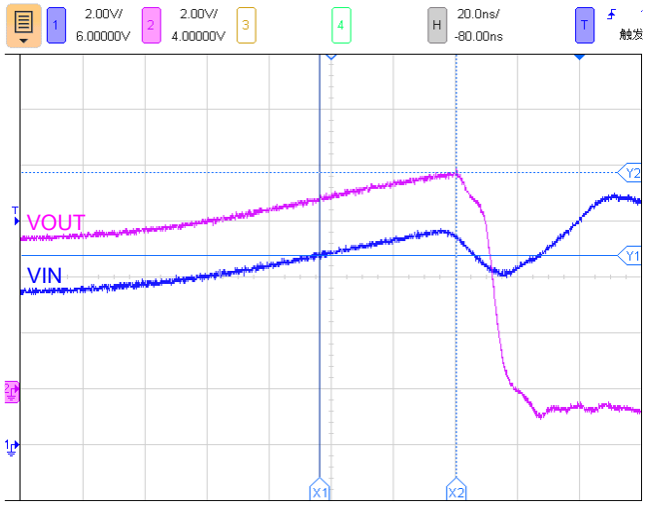


Figure 9. OVP response with 100V surge test (V_{IN_BIAS} = 5V, C_{IN} = C_{OUT} = 0, R_{LOAD} = 100Ω)

Function Description

General Description

LP5307A is an OVP power switch integrated TVS to protect systems and loads which can be damaged or disrupted by the external surge event from input. The device contains a 40mΩ N-channel MOSFET and a controller capable of working over a wide input operating range of 3V to 28V. The controller protects against system malfunctions includes over-voltage protection (adjusted via external resistor ladder), under-voltage lockout and thermal shutdown.

Enable Control

The ENB pin controls the state of the switch. When ENB is pulled low or floating more than 15ms de-bounce time, the load switch is turned on. Activating ENB continuously holds the switch in the on state so long as there is no fault. An under-voltage, over-voltage condition on VIN or a junction temperature in excess of 150°C overrides the ENB control to turn off the switch.

The enable pin ENB's control voltage and VIN pin have independent recommended operating ranges. The ENB pin voltage can be driven by a voltage level higher than the input voltage. There is internal pull-down resistor on ENB pin. Leave the pin floating will active the device as well.

Surge Protection

The LP5307A integrates a TVS for surge protection. The surge event, based on IEC61000-4-5, energy will be absorbed by the device. The surge level is up to ±80V.

ACOKB Indicator

The LP5307A has an open-drain output pin ACOKB to indicate the device status. When ENB is LOW, the ACOKB will be pulled down to ground as long as the input voltage not in UVLO or OVLO status for more than 30ms. Otherwise, the ACOKB will present a floating status and be pulled up by external resistor R_{PU} (***Figure 1***). The ACOKB indication will also be impact by thermal shutdown. When the temperature is higher than protection threshold, the ACOKB will be in Hi-Z status until the temperature drops back for more than 30ms.

Over-Voltage Protection

The LP5307A has Over-Voltage protection to prevent high voltage on IN passing through to OUT. Once the voltage on input exceeds the OVP threshold, the power FET will be turned off immediately. When VIN drop back below OVP release level, the switch will be turned on again after a 15ms de-bounce time.

The LP5307A keeps detecting OVLO pin voltage for default OVP voltage level selection. It has a default OVP at 6.8V(Typical) if OVLO pin is grounded. When the OVLO pin is not grounded, the OVP threshold of LP5307A can be programmed via external resistor divider. Refer to ***Figure 1***, the OVP level can be calculated by the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \frac{R_1 + R_2}{R_2}$$

Under-Voltage Lockout

The under-voltage lockout turns-off the switch if the input voltage drops below the under-voltage lockout threshold. With the ENB pin active, the input voltage rising above the under-voltage lockout threshold more than 15ms will cause a controlled turn-on of the power switch which limits current over-shoots.

Thermal Shutdown

The thermal shutdown protects the device from internally or externally generated excessive temperatures. During an over temperature condition, the switch is turned off. The switch automatically turns on again if the temperature drops below the threshold temperature more than 15ms.

USB On-The-Go Operation

The LP5307A supports USB OTG application. If ENB is pulled down or floated, and OUT is supplied 5V by OTG source while IN is not supplied, the voltage on IN will be pulled up through MOSFET body diode. The IN voltage is initiated to about V_{OUT} – 0.7V. The internal MOSFET will be turned on after IN voltage is higher than V_{UVLO} for 15ms and the voltage drop on IN will be minimized then.

Application Information

Capacitor consideration

External capacitors on IN and OUT are recommended in application, 0.1μF for C_{OUT} and 1μF for C_{IN} at least. Closer placement of the capacitors to the device, both IN and OUT, would be better for stability.

Power Dissipation

The internal power dissipation from the power MOSFET, when it is turned on, is the main source of junction temperature rising. In this case, the power dissipation and the junction temperature in conducting mode can be calculated as following:

$$P_D = R_{ON} \times I_{OUT}^2$$

P_D: Power Dissipation (W)

V_{IN}: Input voltage (V)

V_{OUT}: Output voltage (V)

I_{OUT}: Output current (A)

$$T_J = P_D \times \theta_{JA} + T_A$$

T_J: Junction temperature (°C)

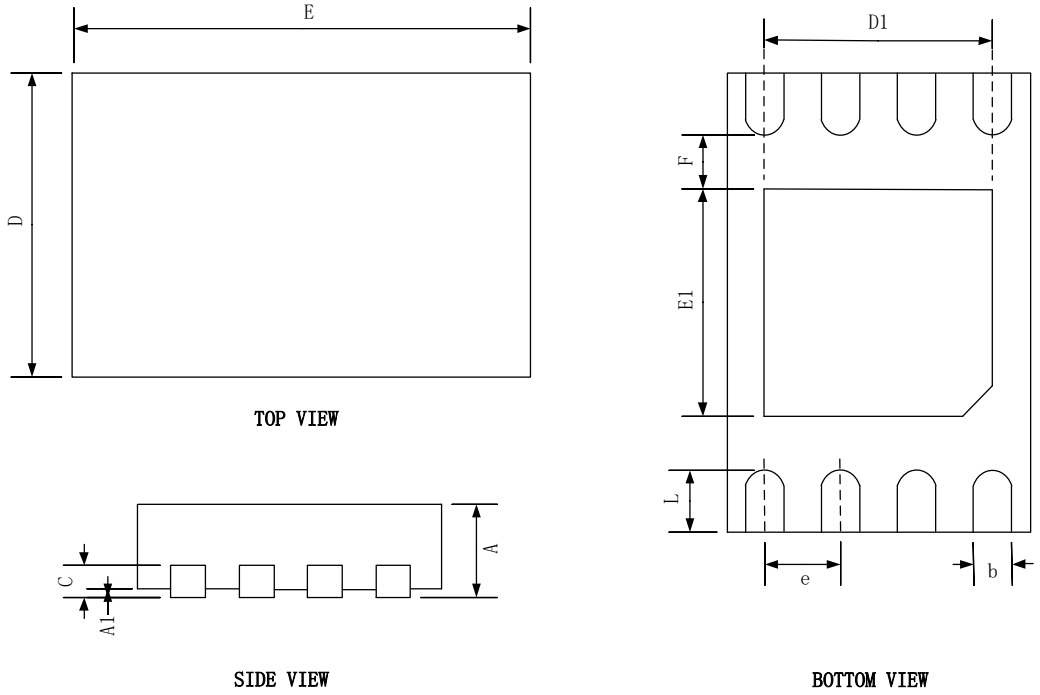
θ_{JA}: Package thermal resistance (°C /W) (Note 4)

T_A: Ambient temperature (°C)

***Note 4: The calculation base on thermal resistance is only valid in Lab condition. The value of θ_{JA} could change in customer PCB environment.**

Package Information

DFN-8 2mm x 3mm



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c		0.20 REF	
D	1.90	2.00	2.10
D1	1.40	1.50	1.60
E	2.90	3.00	3.10
E1	1.50	1.60	1.70
e		0.50 BSC	
L	0.30	0.40	0.50
F	0.20	-	-