

Features ➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low $R_{DS(ON)}$	B_{vds}	R_{dson}	I_D
	60V	2.1mΩ	160A
Application ➤ DC-DC Converters ➤ Synchronous-rectification applications ➤ Power management functions			
Package			
Marking and pin assignment	TO-263 top view	Schematic diagram	

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
S160N06	S160N06HG	TO-263	800

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}@10V^{1,6}$	$T_C=25^\circ\text{C}$	160	A
	$T_C=100^\circ\text{C}$	101.2	A
Pulsed Drain Current ²	I_{DM}	640	A
Single Pulse Avalanche Energy ³	E_{AS}	352.8	mJ
Avalanche Current	I_{AS}	51	A
Total Power Dissipation ⁴	$T_C = 25^\circ\text{C}$	96	W
Storage Temperature Range ¹	T_{STG}	-55 ~ 150	$^\circ\text{C}$
Operating Junction Temperature Range ¹	T_J	-55 ~ 150	$^\circ\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	48	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.3	$^{\circ}\text{C}/\text{W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS160N06HG	TO-263	1	2	3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu\text{A}$	60	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_J=100^{\circ}\text{C}$	-	-	-	
Gate-Source Leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2	2.8	4	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=24A$	-	2.1	3	m Ω
		$V_{GS}=4.5V, I_D=12A$	-	-	-	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=24A$	-	89	-	S
Gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	-	2.2	-	Ω
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=10V, I_D=24A$	-	68	-	nC
Gate-Source Charge	Q_{gs}		-	16	-	
Gate-Drain Charge	Q_{gd}		-	20.5	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=30V, I_D=24A,$ $R_{GEN}=3\Omega$	-	17	-	ns
Rise Time	T_R		-	17.8	-	
Turn-Off Delay Time	$T_{d(off)}$		-	40	-	
Fall Time	T_f		-	21	-	
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V, f=1\text{MHz}$	-	4070	-	pF
Output Capacitance	C_{oss}		-	1053	-	
Reverse Transfer Capacitance	C_{rss}		-	31	-	
Continuous Source Current ^{1,4}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	160	A
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=24A, T_J=25^{\circ}\text{C}$	-	-	1.2	V
Reverse Recovery time	t_{rr}	$I_F=24A, di/dt=100A/\mu\text{s},$	-	56	-	ns



Reverse Recovery Charge	Q_{rr}	$T_J=25^\circ\text{C}$	-	67.5	-	nC
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Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.4\text{mH}$, $I_{AS}=51\text{A}$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

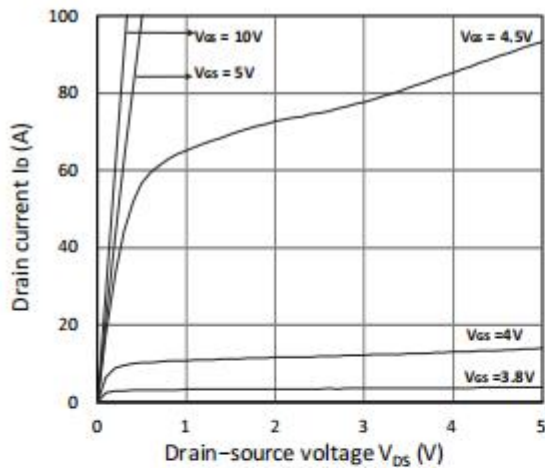


Figure 1. Output Characteristics

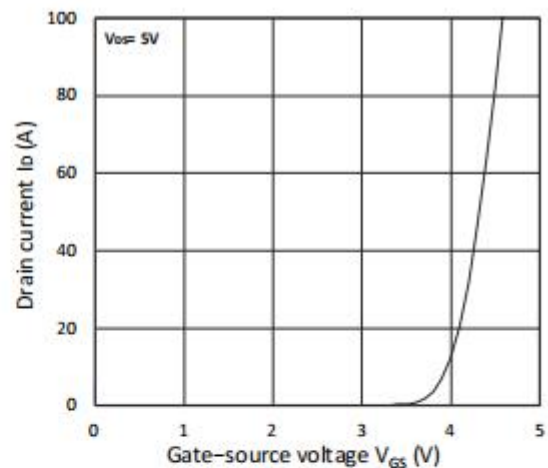


Figure 2. Transfer Characteristics

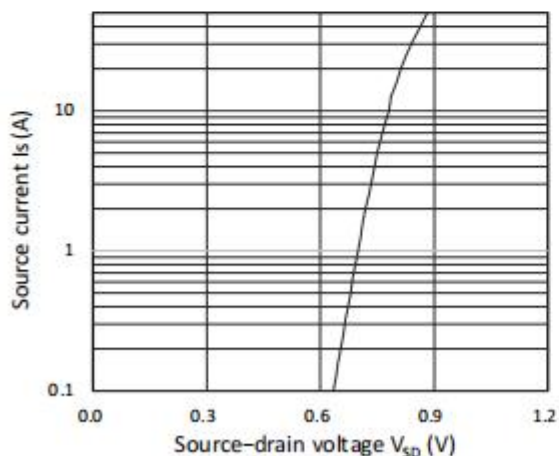


Figure 3. Forward Characteristics of Reverse

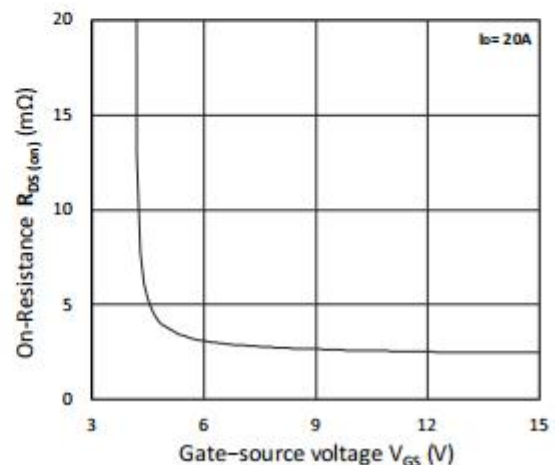


Figure 4. $R_{DS(on)}$ vs. V_{GS}

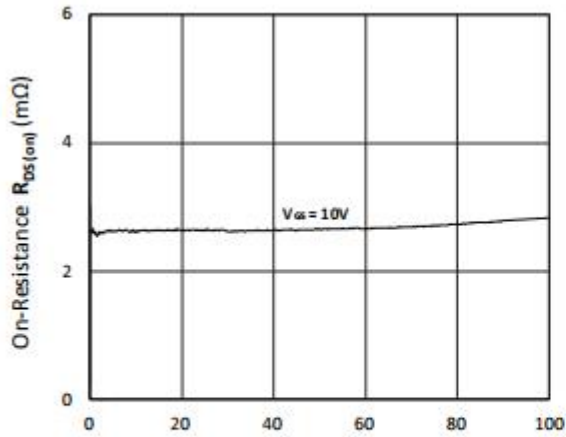


Figure 5. $R_{DS(on)}$ vs. I_D

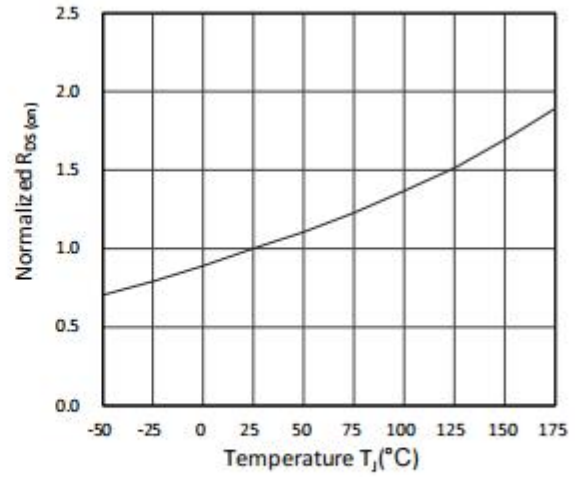


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

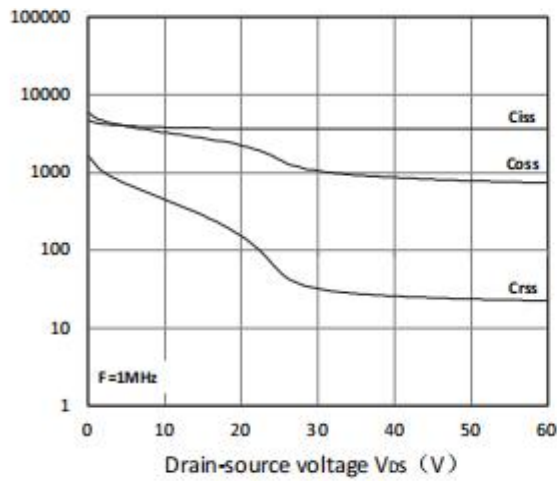


Figure 7. Capacitance Characteristics

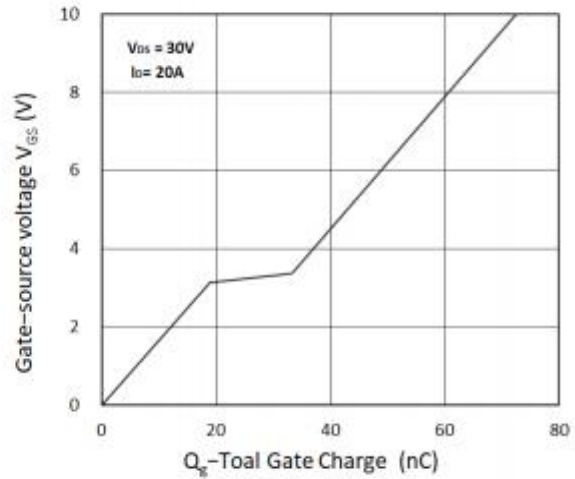


Figure 8. Gate Charge Characteristics

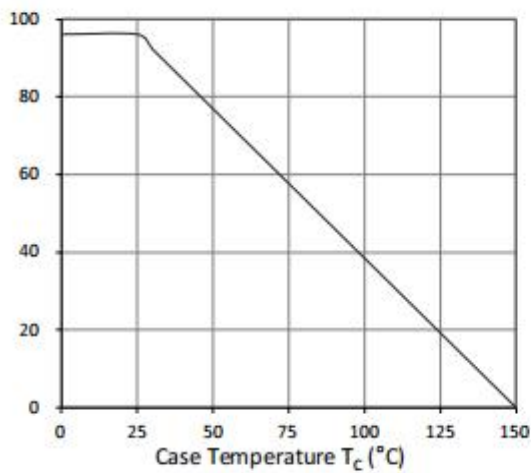


Figure 9. Power Dissipation

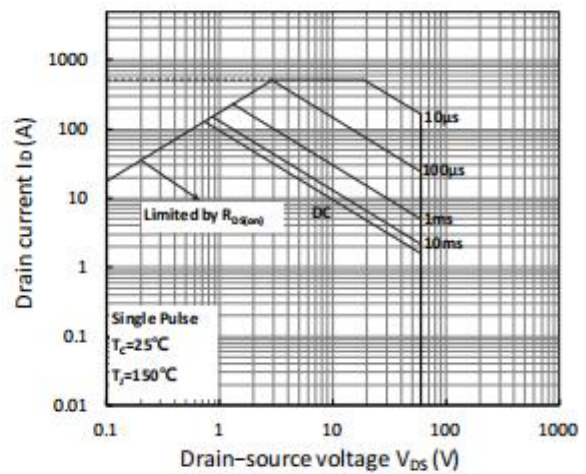


Figure 10. Safe Operating Area

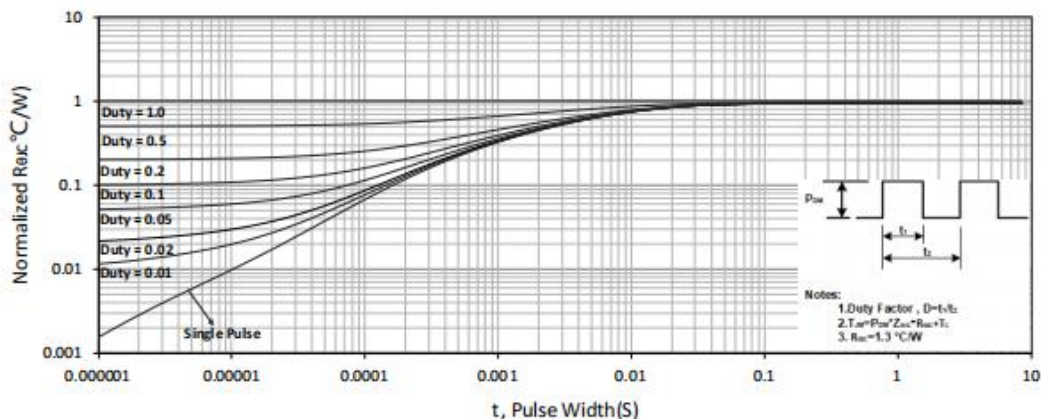
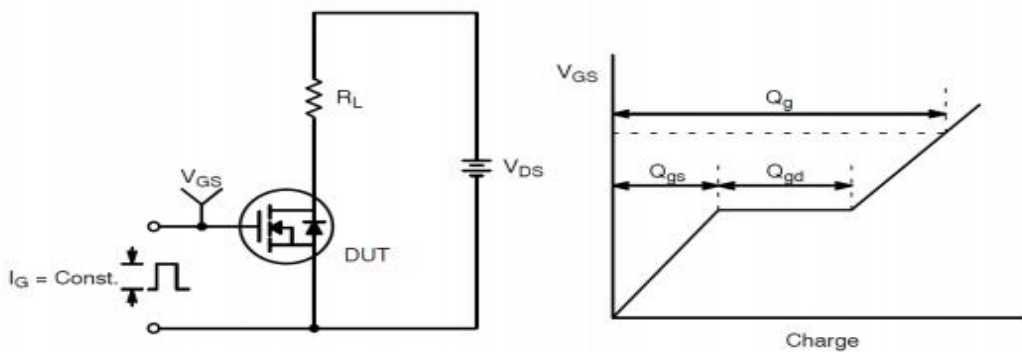
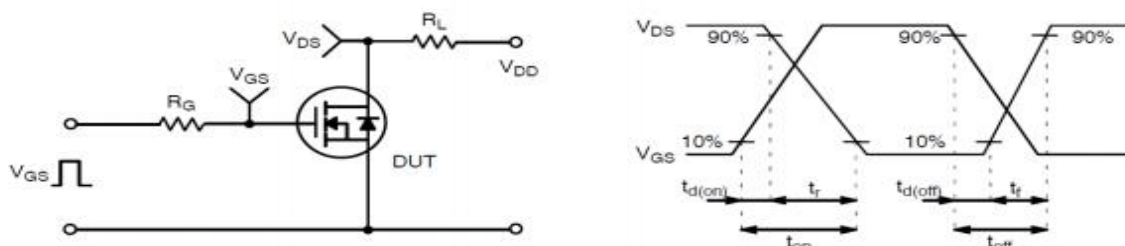


Figure 11. Normalized Maximum Transient Thermal Impedance

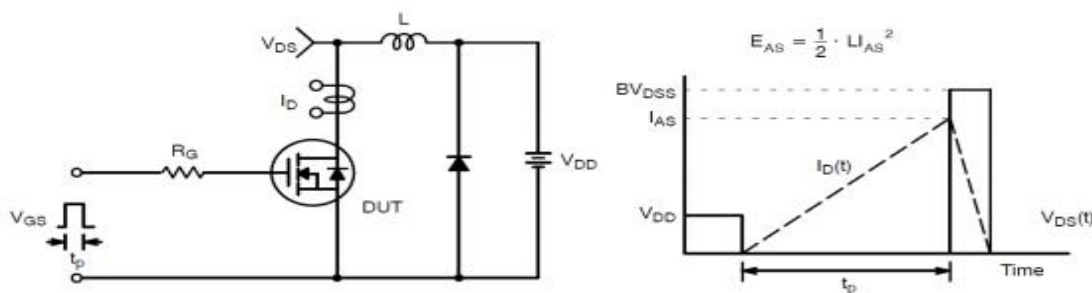
Test Circuit and Waveform:



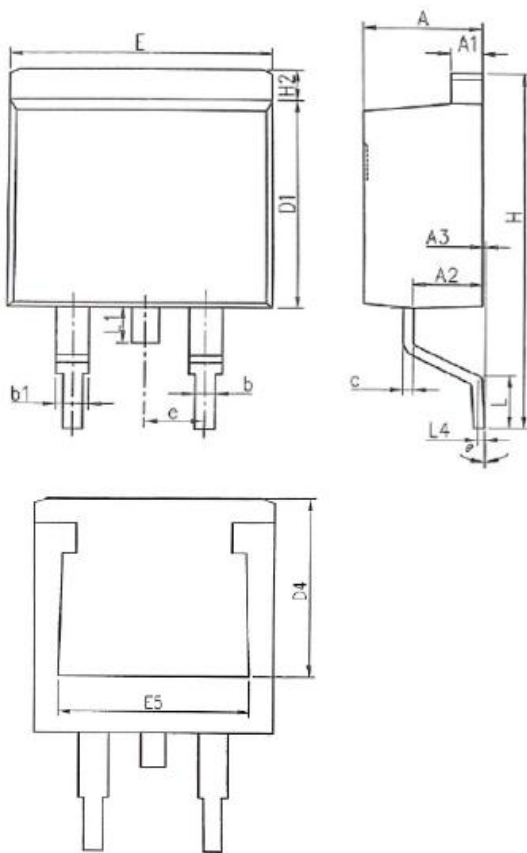
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

Package Dimensions TO263
COMMON DIMENSIONS


SYMBOL	MM	
	MIN	MAX
A	4.37	4.89
A1	1.17	1.42
A2	2.20	2.90
A3	0.00	0.25
b	0.70	0.96
b1	1.17	1.47
c	0.28	0.60
D1	8.45	9.30
D4	6.60	-
E	9.80	10.40
E5	7.06	-
e	2.54BSC	
H	14.70	15.70
H2	1.07	1.47
L	2.00	2.80
L1	-	1.75
L4	0.254BSC	
θ	0°	9°



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