

Features ➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low $R_{DS(ON)}$	B_{vds}	R_{dson}	ID
	40V	0.75mΩ	320A
Application ➤ DC-DC Converters ➤ Power management functions ➤ Synchronous-rectification applications			

Package			
	Marking and pin assignment	TOLL-8L top view	Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
320N04TL	S320N04TL	TOLL-8L	2000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}@10V^1$	$T_C=25^{\circ}\text{C}$	I_D	320
	$T_C=100^{\circ}\text{C}$	I_D	160
Pulsed Drain Current ²	I_{DM}	720	A
Single Pulse Avalanche Energy ³	EAS	450	mJ
Total Power Dissipation ⁴	$T_C=25^{\circ}\text{C}$	P_D	114
Operating Junction Temperature Range	T_J	-55 ~ 150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ 150	$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient ¹	$R_{\theta JA}$	55	$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	1.1	$^{\circ}\text{C}/\text{W}$



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS320N04TL	TOLL-8	1	9	2,3,4,5,6,7,8	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	-	-	1	μA
	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_J=100^{\circ}\text{C}$	-	-	100	μA
Gate-body Leakage current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.3	1.7	2.3	V
Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A$	-	0.75	1.1	m Ω
		$V_{GS}=4.5V, I_D=25A$	-	1.4	2	m Ω
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V,$ $f=1\text{MHz}$	-	5500	-	pF
Output Capacitance	C_{oss}		-	1850	-	
Reverse Transfer Capacitance	C_{rss}		-	65	-	
Gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	-	3.5	-	Ω
Total Gate Charge	Q_g	$V_{DS}=20V, V_{GS}=10V,$ $I_D=50A$	-	87	-	nC
Gate-Source Charge	Q_{gs}		-	18	-	
Gate-Drain Charge	Q_{gd}		-	15	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=50A,$ $R_G=3\Omega, V_{GS}=10V$	-	14	-	ns
Rise Time	t_r		-	15	-	
Turn-Off Delay Time	$t_{d(off)}$		-	84	-	
Fall Time	t_f		-	44	-	
Continuous Source Current ^{1,4}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	320	A
Pulsed Source Current ^{2,4}	I_{SM}		-	-	720	A
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=-1A, T_J=25^{\circ}\text{C}$	-	-	1.2	V
Reverse Recovery time	t_{rr}	$I_F=50A, dI/dt=100A/\mu s,$ $T_J=25^{\circ}\text{C}$	-	55	-	ns
Reverse Recovery Charge	Q_{rr}		-	53	-	nC

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.The EAS data shows Max.rating . The test condition is $T_J=25^{\circ}\text{C}, V_{DD}=25V, V_{GS}=10V, L=0.5\text{mH}$.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

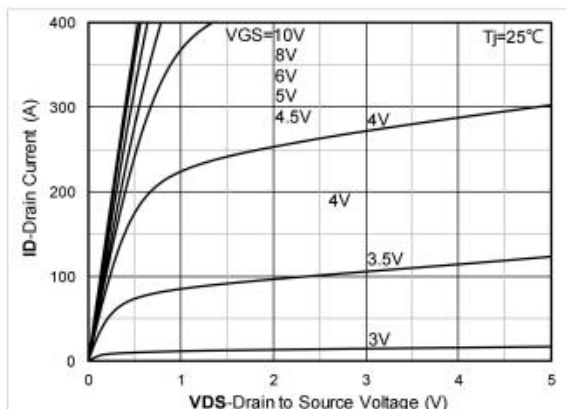


Figure 1. Output Characteristics

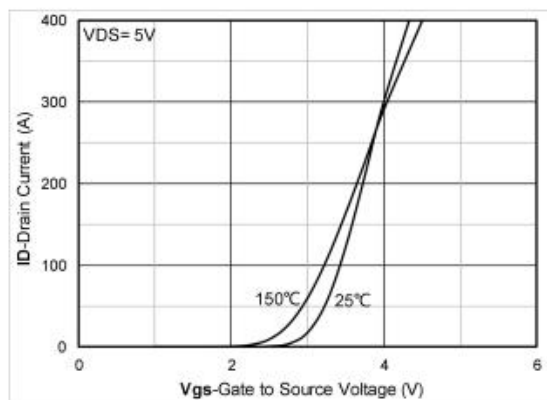


Figure 2. Transfer Characteristics

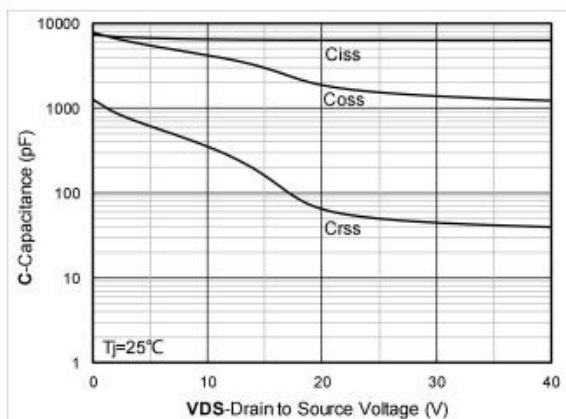


Figure 3. Capacitance Characteristics

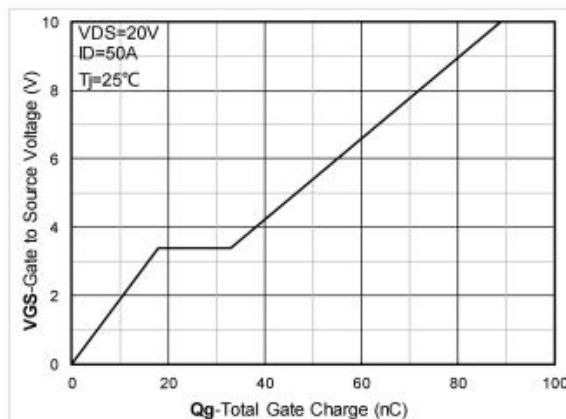


Figure 4. Gate Charge

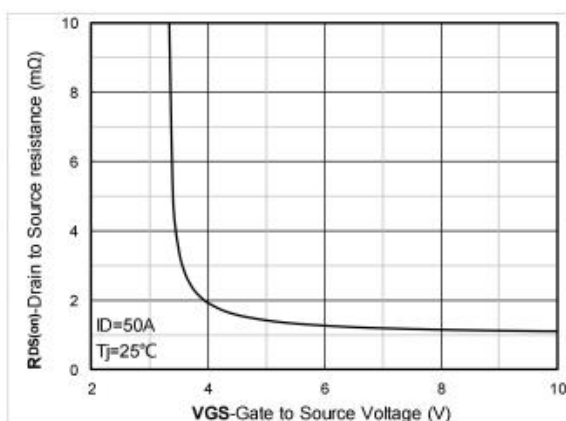


Figure 5. On-Resistance vs Gate to Source Voltage

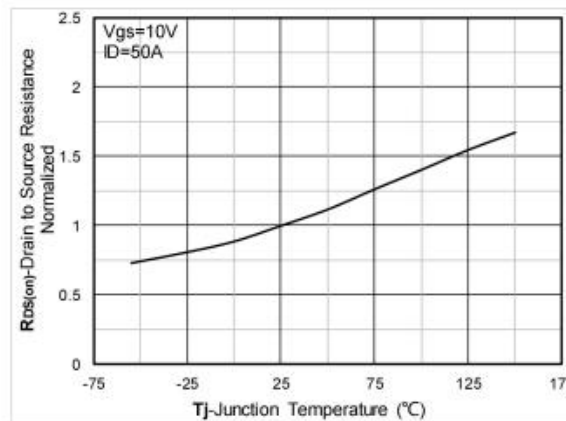


Figure 6. Normalized On-Resistance

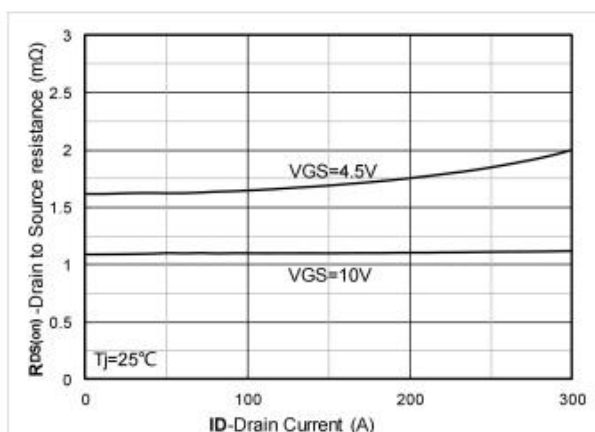


Figure 7. $R_{DS(on)}$ VS Drain Current

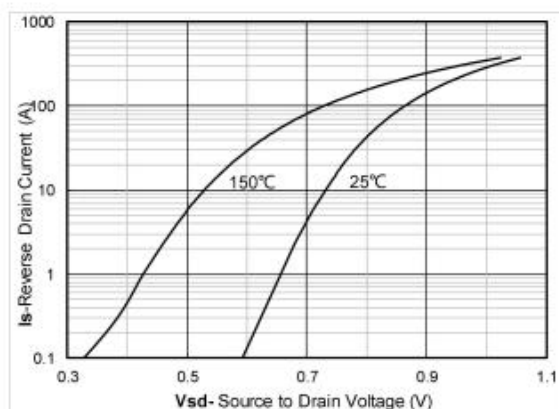


Figure 8. Forward characteristics of reverse diode

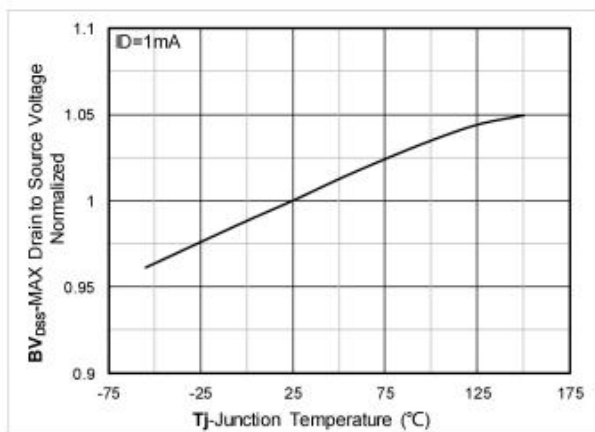


Figure 9. Normalized breakdown voltage

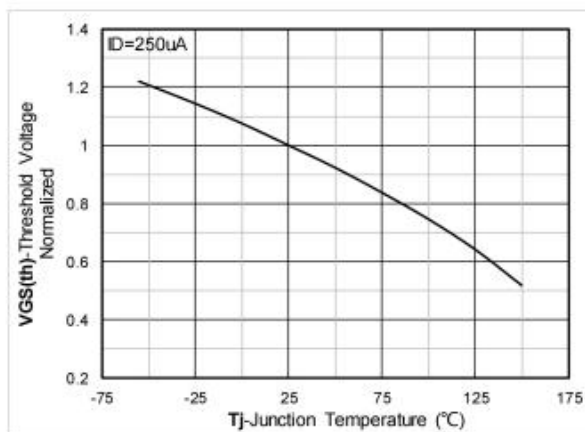


Figure 10. Normalized Threshold voltage

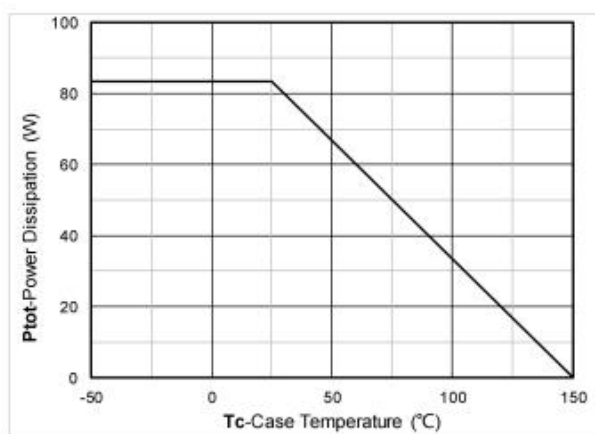


Figure 11. Power dissipation

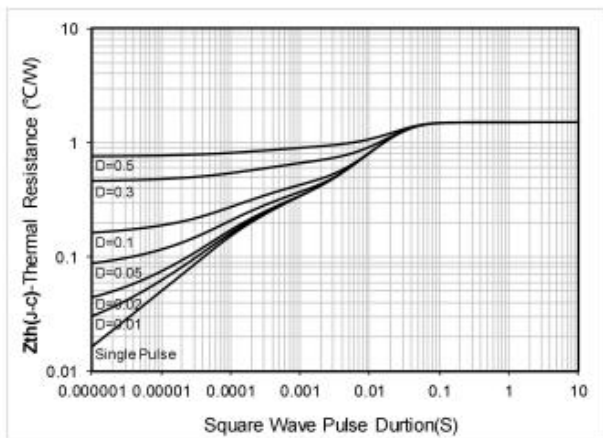


Figure 12. Maximum Transient Thermal Impedance

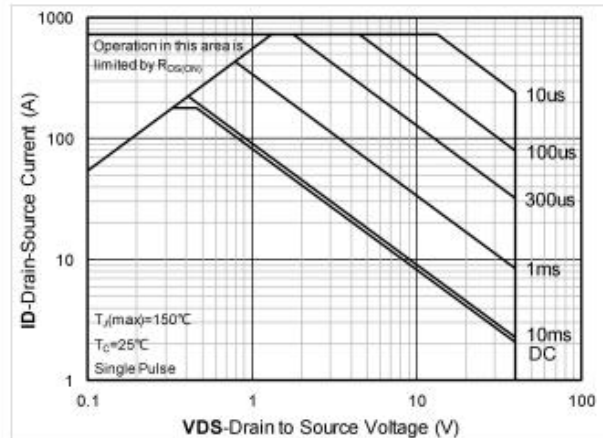
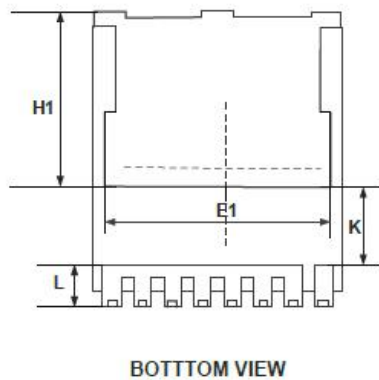
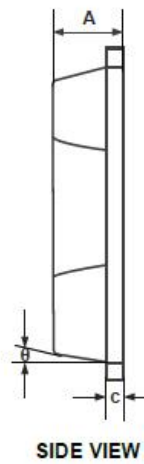
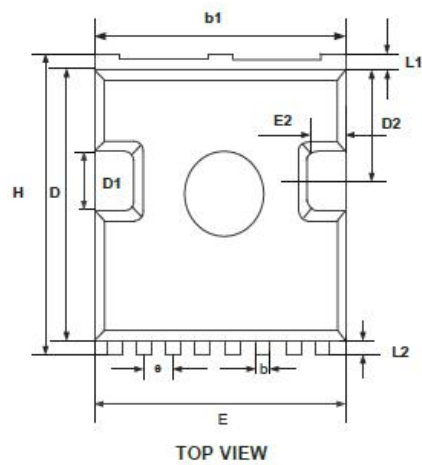


Figure 13. Safe Operation Area



Package Dimensions TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	



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