A33003

Precision Angle Sensor IC
with On-Chip Linearization, SENT, SPI, and PWM Output

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - □ Capable of sensing magnet rotational speeds targeting 12-bit effective resolution with 900 G field
  - □ Circular vertical Hall (CVH) technology provides a single-channel sensor system supporting operation across a wide range of air gaps
- On-chip 32-segment linearization to improve angle accuracy
  - □ Reduces the impact of magnet to sensor misalignment
  - □ Reduces the impact of imperfect magnetization of target magnet
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications
  - □ Single-die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A33003 Safety Manual
  - □ Dual-die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the A33003 Safety Manual
- Programmable via Manchester encoding on the output line to reduce external wiring and enable in-application programming when in PWM or SENT mode

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DESCRIPTION

The A33003 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing to calculate the angular position data, and selectable output protocols (SPI, SENT, or PWM). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles for flexible programming of calibration parameters. The A33003 is ideal for automotive applications requiring 0° to 360° angle measurements and high levels of redundancy, such as electronic power steering (EPS), transmission actuators, and steer-by-wire (SBW) systems.

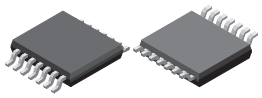
The A33003 includes on-chip 32-segment linearization. This can be used to calibrate out errors due to misalignment between the magnet and the sensor or imperfect magnetization of the target magnet (which can present as a misalignment of the magnet to the sensor).

The A33003 supports customer integration into safety-critical applications.

The A33003 is available in a single- or dual-die 14-pin TSSOP package (suffix LU). The package is lead (Pb) free with 100% matte tin leadframe plating. The 1 mm thin package reduces the minimum air gap between the CVH transducer and the target magnet.

PACKAGE:

Not to scale



14-pin TSSOP
(Suffix LU)

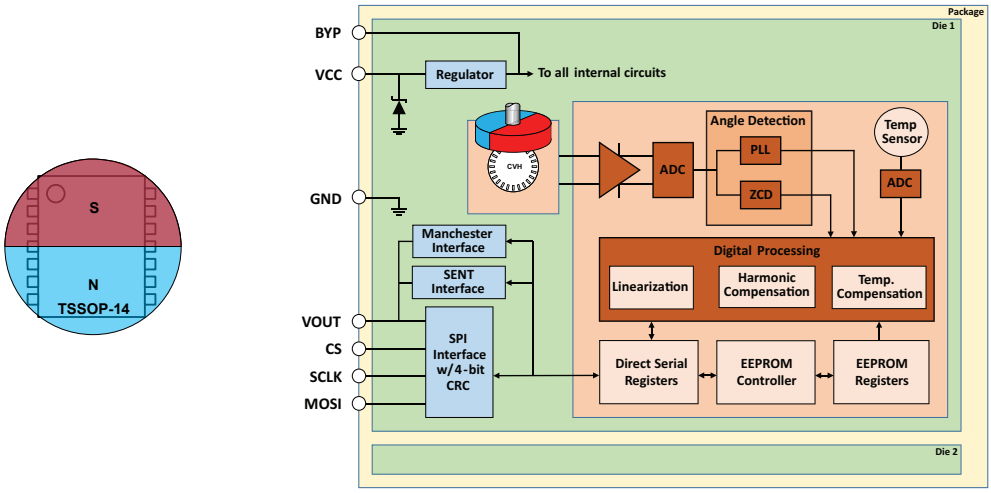


Figure 1: A33003 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- Digital output format selectable between SPI, SENT, or PWM
- SENT output is SAE J2716 JAN2010-compliant with Allegro proprietary enhancements
  - □ Customer-programmable SENT tick times ranging from 0.5 to 7.9 µs
- On-chip EEPROM for storing factory and customer calibration parameters
  - □ Integrated charge pump allows in-application programming without any requirement for high voltages to be supplied to the device during programming
  - □ Single-bit error correction, dual-bit error detection error correction control (ECC)
- Supports operation in harsh conditions, required for automotive and industrial applications
  - □ Operating temperature range from –40°C to 150°C
  - □ Operating supply voltage range from 4.5 to 5.5 V, absolute maximum of 28 V
- Loss of power is indicated by reset flag
- 10 MHz SPI for low-latency angle and diagnostic information; enables multiple independent ICs to be connected to the same bus
  - □ 4-bit CRC
- Multiple programming/configuration formats supported
  - □ The system can be completely controlled and programmed over SPI or Manchester protocol, including EEPROM writes
  - □ For system with limited pins available, writing and reading can be performed over the VOUT pin
  - □ 1 mm thin surface-mount TSSOP package to minimize air gap from target magnet to the CVH transducer for improved field strength

SELECTION GUIDE

Part Number	Hot Trim Temperature	Interface Voltage [1]	System Die	Package	Packing
A33003LLUATR	150°C	3.3 V	Single	14-pin TSSOP	4000 pieces per 13-inch reel
A33003LLUBTR-DD	150°C	3.3 V	Dual		

[1] Contact Allegro MicroSystems for 5 V interface availability.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles, respecting T_J(max)	28	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
VOUT Pin	V_{OUT}		18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		–0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LU-14 package; measured on JEDEC JESD51-7 2s2p board	82	°C/W

[1] Additional thermal information is available on the Allegro website.

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Table of Contents

ALLEGRO microsystems

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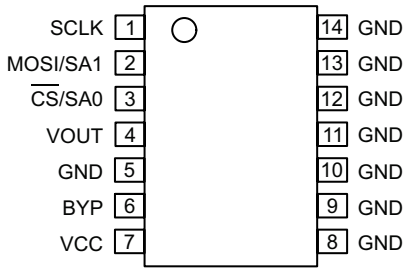
PINOUT DIAGRAMS AND TERMINAL LIST TABLES

Pinout Diagram

LU 14-Pin TSSOP, Single Die

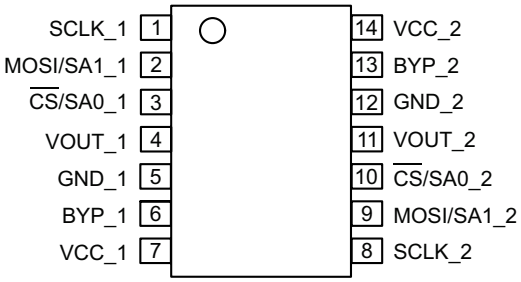


Terminal List Table, Single Die

Pin Number	Pin Name	Function
1	SCLK	SPI: Clock input terminal.
2	MOSI/SA1	SPI: Controller-Out Peripheral-In. Manchester/SENT: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0.
3	$\overline{CS}$/SA0	SPI Chip Select terminal, active low input. Manchester/SENT: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0.
4	VOUT	SPI: Controller In/Peripheral Out, push-pull. SENT/PWM: Input/Output, open drain. Manchester: Input/Output, push-pull.
5, 8–14	GND	Device ground terminal. All GND pins should be connected together.
6	BYP	External bypass capacitor terminal for internal regulator.
7	VCC	Power supply.

Pinout Diagram

LU 14-Pin TSSOP, Dual Die



Terminal List Table, Dual Die

Pin Number	Pin Name	Function
1	SCLK_1	SPI: Clock input terminal. (Die 1)
2	MOSI/SA1_1	SPI: Controller-Out/Peripheral-In. Manchester/SENT: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 1)
3	$\overline{CS}$/SA0_1	SPI chip select terminal, active low input. Manchester/SENT: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 1)
4	VOUT_1	SPI: Controller-In/Peripheral-Out, push-pull. SENT/PWM: Input/Output, open drain. Manchester: Input/Output, push-pull. (Die 1)
5	GND_1	Device ground terminal. (Die 1)
6	BYP_1	External bypass capacitor terminal for internal regulator. (Die 1)
7	VCC_1	Power supply. (Die 1)
8	SCLK_2	SPI: Clock input terminal. (Die 2)
9	MOSI/SA1_2	SPI: Controller-Out/Peripheral-In. Manchester/SENT: Sets bit 1 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 2)
10	$\overline{CS}$/SA0_2	SPI chip select terminal, active low input. Manchester/SENT: Sets bit 0 of address field. Tie to BYP for a logic 1, GND for a logic 0. (Die 2)
11	VOUT_2	SPI: Controller-In/Peripheral-Out, push-pull. SENT/PWM: Input/Output, open drain. Manchester: Input/Output, push-pull. (Die 2)
12	GND_2	Device ground terminal. (Die 2)
13	BYP_2	External bypass capacitor terminal for internal regulator. (Die 2)
14	VCC_2	Power supply. (Die 2)

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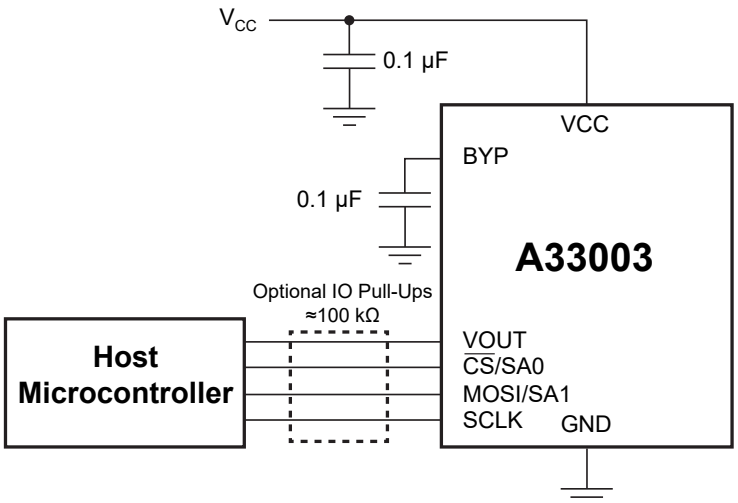

Figure 2: A33003 Typical Setup

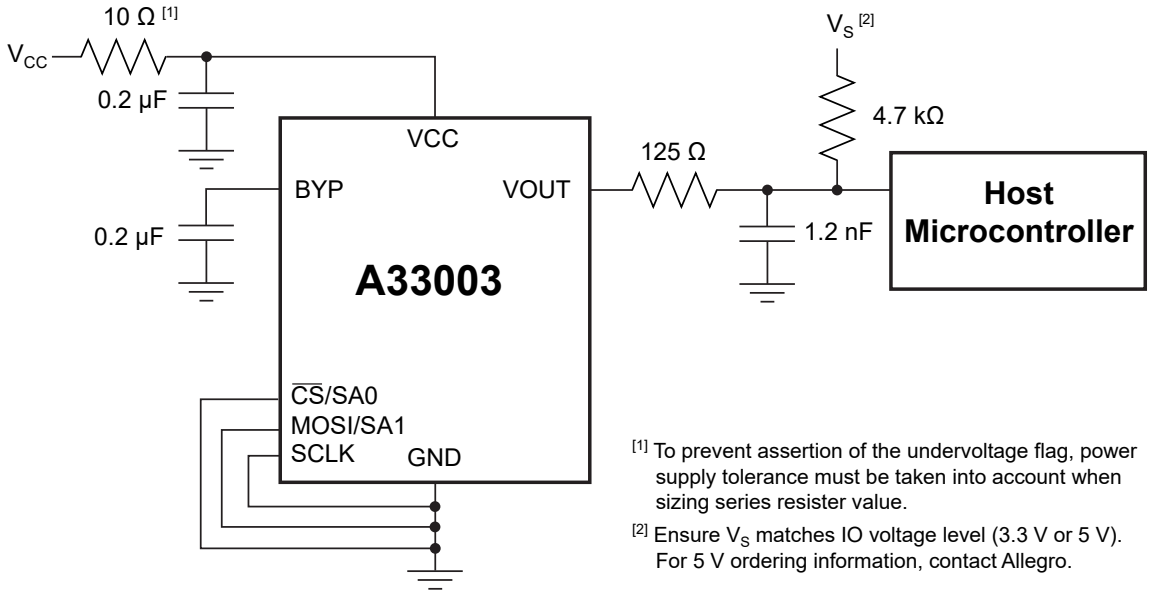

Figure 3: A33003 Reference Design for Stringent EMC Requirements

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OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Customer supply	4.5	–	5.5	V
Supply Current	I_{CC}	Each die	11	13	16	mA
Undervoltage Flag Threshold	V_{UVD}	dV/dt = 1 V/ms, A33003 sampling enabled	4.5	–	4.7	V
Supply Zener Clamp Voltage	V_{ZSUP}	$I_{CC} = I_{CC(max)} + 3$ mA, $T_A = 25°C$	26.5	–	–	V
Reverse Battery Current	I_{RCC}	$V_{RCC} = –18$ V, $T_A = 25°C$	–	–	–5	mA
Power-On Time [1]	t_{PO}	Power-on diagnostics disabled	–	15	–	ms
Bypass Pin Output Voltage [2]	V_{BYP}	$T_A = 25°C$, $C_{BYP} = 0.1$ µF, 3.3 V interface	2.93	3.3	3.63	V
		$T_A = 25°C$, $C_{BYP} = 0.1$ µF, 5.0 V interface, $V_{CC} = 5$ V	4	–	5.5	V
Digital Oscillator Frequency	f_{OSC}	Main digital oscillator	28	32	36	MHz
SPI INTERFACE SPECIFICATIONS (for 3.3 V interface)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	VOUT pins, $C_L = 20$ pF	2.93	3.3	3.63	V
SPI Output Low Voltage	V_{OL}	VOUT pins, $C_L = 20$ pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS (for 5.0 V interface) (*Contact Allegro for 5 V SPI ordering information*)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	VOUT pins, $C_L = 20$ pF	4	5	–	V
SPI Output Low Voltage	V_{OL}	VOUT pins, $C_L = 20$ pF	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [3]	f_{SCLK}	VOUT pins, $C_L = 20$ pF	0.1	–	10	MHz
SPI Clock Duty Cycle [3]	D_{fSCLK}	SPI_{CLKDC}	40	-	60	%
SPI Frame Rate [3]	t_{SPI}	Assuming a 16-bit SPI packet	5.8	–	588	kHz
Chip Select to First SCLK Edge [3]	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time [3]	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time [3]	t_{DAV}	Data output valid after SCLK falling edge	–	–	50	ns
MOSI Setup Time [3]	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time [3]	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time [3]	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns
Load Capacitance [3]	C_L	Loading on digital output (VOUT) pin	–	–	20	pF

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
MANCHESTER INTERFACE SPECIFICATIONS							
Bit Rate		Defined by the input message bit rate sent from the external controller		4	–	40	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps		243	250	257	µs
		Data bit pulse width at 100 kbps		9.5	10	10.5	µs
Bit Time Error	err_{tBIT}	Deviation in t_{BIT} during one command frame		–11	–	11	%
Read Delay	t_{START_READ}	Delay from the trailing edge of a read command frame to the leading edge of the read acknowledge frame		2 × t_{BIT}	–	–	µs
Bit Time Delay	t_b			–	2	–	t_{BIT}
Access Code Timeout	t_{msgRX}			–	–	300	µs
Interrupt Pulse Hold Time	t_{HOLD}	SSENT—Short	F_AUX	56	–	70	ticks
		SSENT—Long	F_AUX	216	–	264	ticks
		ASENT	F_AUX	56	–	70	ticks
		SENT	Aux. interrupt pulse	30	–	–	ticks
		TSENT	Aux. interrupt pulse	30	–	–	ticks
		PWM	Aux. interrupt pulse	2 × PWM period [4]	–	–	µs
Deglitch Gate Time	t_{GATE}			1.0	–	–	µs
INPUT SIGNAL VOLTAGE							
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to PWM/MISO/SENT line		2.8	–	V_{CC}	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to PWM/MISO/SENT line		0.0	–	1.2	V
OUTPUT SIGNAL VOLTAGE							
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{PULLUP} = 5 kΩ		0.9 × V_S	–	–	V
		Maximum R_{PULLUP} = 50 kΩ		0.7 × V_S	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ < R_{PULLUP} < 50 kΩ		–	–	0.1	V

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency [3]	f_{PWM}	PWM frequency min. setting, T_A in specification	–	98	–	Hz
		PWM programmable options	–	128	–	codes
		PWM frequency max. setting, T_A in specification	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
PWM Output Resolution	RES_{PWM}		–	12	–	bit
PWM Output Saturation Voltage	$V_{SAT\_LOW(PWM)}$	Output current = –1 mA, V_{CC} = 5 V, output FET on	–	–	0.25	V
PWM Current Limit	$I_{LIMIT(PWM)}$	Output FET on, T_A = 25°C	20	36	45	mA
PWM Output Impedance [3]	$R_{ON(PWM)}$	PWM driver impedance when pulling to logic low; T_A = 25°C	40	–	250	Ω
SENT SPECIFICATIONS [3]						
SENT Tick Time	t_{TICK}	All SENT modes [5]	0.5	–	7.9375	µs
SENT Tick Time Tolerance	TOL_{tTICK}	All SENT modes	–15	–	15	%
SENT Output Trigger Thresholds	$V_{SENTtrig(L)}$	V_{OUT} falling, 3.3 V digital	–	–	1.2	V
	$V_{SENTtrig(H)}$	V_{OUT} rising, 3.3 V digital	2.8	–	–	V
SENT Output Saturation Voltage	$V_{SAT(LOW)}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.45	V
SENT Output Current Limit	I_{LIMIT}	Output FET on, T_A = 25°C	20	36	45	mA
SENT Output Load Resistance	$R_{L(PULLUP)}$	Output current ≥ –10 mA	1.2	–	–	kΩ
Trigger Delay Time [6]	t_{dSENT}	From end of trigger pulse to beginning of SENT message frame (TSENT and shared SENT)	7	–	–	ticks
SENT Output Impedance [3]	$R_{ON(SENT)}$	SENT driver impedance when pulled to logic low; T_A = 25°C	40	–	250	Ω
BUILT-IN SELF TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request	–	52	–	ms

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	900	G [7]
ANGLE CHARACTERISTICS						
Output [8]	RES_{ANGLE}	Both 12- and 15-bit angle values are available via SPI	–	12/15	–	bit
Angle Refresh Rate [9]	t_{ANG}	No averaging	–	2.0	–	µs
Response Time [3]	$t_{RESPONSE}$	Angular latency	–	17	–	µs
Effective Resolution [10]		B = 300 G [7], T_A = 25°C	–	12.5	–	bits

A33003LLUATR and A33003LLUBTR-DD PERFORMANCE CHARACTERISTICS:
Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions [11]	Min.	Typ.	Max.	Unit
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.2	±0.4	1.2	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.5	±0.5	1.5	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G	–1.75	–	1.75	degrees
		T_A = –40°C, B = 300 G	–	±1	–	degrees
Angle Noise [12]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3 sigma noise	–	±0.19	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, target rpm = 0, 3 sigma noise	–	±0.25	–	degrees
Angle Drift Over Lifetime [13]	$Angle_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.34	–	degrees

[1] During the power-on phase, the A33003 SPI transactions are valid within ≈ 300 µs of power on (with no self-tests). Angle reading requires full t_{PO} to stabilize.
[2] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during typical operation.
[3] Parameter is not guaranteed at final test. Determined by design.
[4] The minimum hold time for the Auxiliary interrupt, when the output is set for PWM, is double the PWM period. If the PWM frequency increases as a result of a diagnostic condition, the hold time is double the new PWM period at the diagnosis frequency.
[5] Tick times less than 0.5 µs are available, but not guaranteed.
[6] The synchronization pulse delay is a minimum of 7 ticks but can be extended to cover Slot Marking in SSENT.
[7] 1 G (gauss) = 0.1 mT (millitesla). Recommended minimum field is 300 G.
[8] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[9] The rate at which a new angle reading becomes ready.
[10] Effective Resolution is calculated using the formula below:

$$Effective\ Resolution = log_2(360) - log_2\left(\frac{1}{n} \times \sum_{i=1}^{n} \sigma_i\right)$$

where σ is the Standard Deviation based on thirty measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.

[11] 1 G (gauss) = 0.1 mT (millitesla).
[12] This value represents 3-sigma, or three times the standard deviation, of the measured samples.
[13] Maximum drift observed during AEC-Q100 testing was 1.076 degrees.

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TYPICAL PERFORMANCE CHARACTERISTICS

The figures below show performance data from 30 samples of A33003LLUBTR-DD devices.

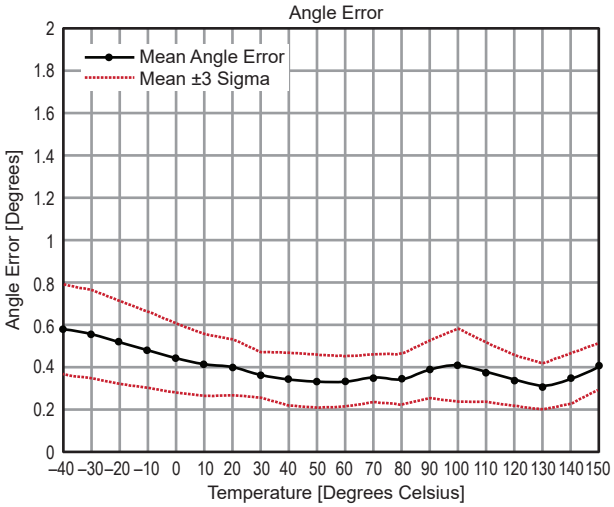

Figure 4: Peak Angle Error over Temperature (300 G)

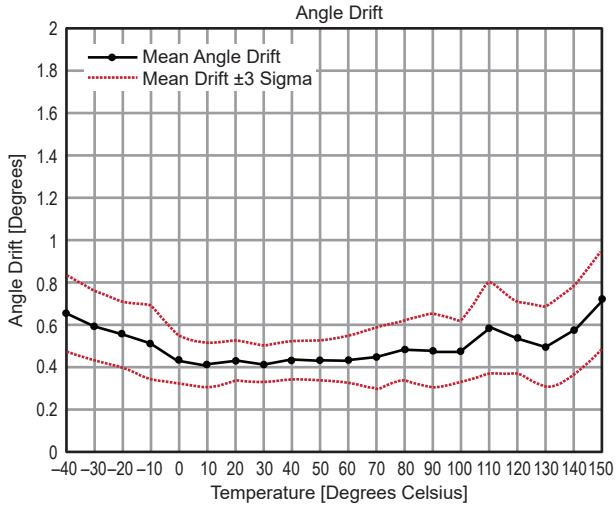

Figure 5: Maximum Absolute Drift over Temperature (300 G)

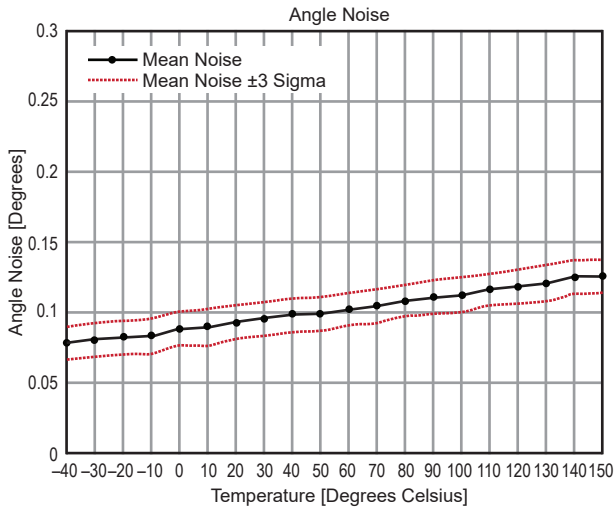

Figure 6: Noise Performance over Temperature (3-Sigma, 300 G)

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FUNCTIONAL DESCRIPTION

Overview

The A33003 is a rotary position Hall-sensor-based device in a surface-mount package, providing solid-state consistency and reliability, and supporting a wide variety of automotive applications. The Hall-sensor-based device measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). The integrated circuit includes a circular-vertical-Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter, digital filtering, and digital signal processing.

Advanced offset, gain, and linearization adjustment options are available in the A33003. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurement

The A33003 is capable of tracking magnet position at high speed. Performance up to 12,000 rpm has been verified by testing. Operation up to 30,000 rpm has been verified via design simulation. The A33003 has a typical output refresh rate of 2 µs.

Readout in SPI is possible with 12-bit resolution, with error flags included in the same word, or in 15-bit resolution without included error flags. Reading out the angle requires a minimum of 16 SPI clock cycles. A 20-bit SPI packet with 4 bits of CRC is also supported.

PWM output is always resolved to a 12-bit angle value.

When using SENT output, a 12-bit or 16-bit angle packet may be selected via the DATA_MODE field in EEPROM.

The sensor readout is processed and linearized in various steps. These are detailed in Figure 9.

System-Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from time of magnet sampling until generation of a processed angle value. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values presented to the user are latched to the output registers on the first SCLK edge of the SPI output frame. This means that, if the SPI clock is 10 MHz, the data are clocked out after 1.6 µs. Because the data are sampled-in at the first clock edge at an age of maximum $t_{RESPONSE}$, its age after the SPI transaction has finished is between 1.6 and 1.6 + $t_{RESPONSE}$ µs.

Similar to SPI, when using the PWM output, the output packet is not synchronized with the internal update rate of the sensor. The angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{response} + 1/f_{PWM}$.

The point within the SENT packet at which the angle value is latched varies with SENT configurations. However, in all configurations, the SENT transmission time is the dominant contributor to the delay. For a detailed description, see Appendix A: SENT Output Description.

Power-Up

Upon applying power to the A33003, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes time to complete, which is referred to as power-on time, t_{PO}. If diagnostics are enabled at power-up, additional time is required for the device to complete the programmed tests. Regardless of the state of the device before a power cycle, the device repowers with EEPROM shadow bits copied from the EEPROM and with serial registers in their default states. For example, on every power-up, the device powers up with the zero_offset that was stored in the EEPROM. The extended write access field, WRITE_ADR, is set back to its default value of zero.

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PWM Output

The A33003 provides a pulse-width-modulated (PWM) open-drain output, with the duty cycle proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% for diagnostic purposes. A 5% duty cycle corresponds to 0°; a 95% duty cycle corresponds to 360°.

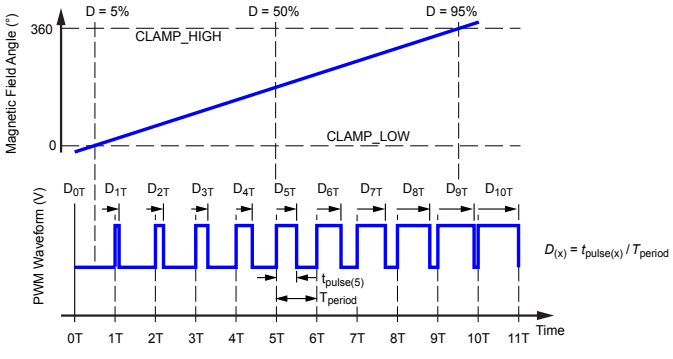

Figure 7: PWM Mode Outputs a Duty Cycle Proportional To Sensed Angle

Within each cycle, the output is high for the first 5% and low for the last 5% of each period. The middle 90% of the period is a linear interpolation of the angle as sampled at the start of the PWM period.

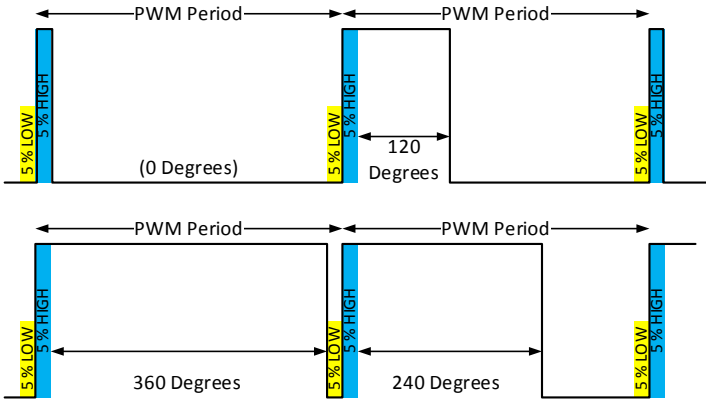

Figure 8: Pulse-Width Modulation (PWM) Examples

The angle is represented in 12-bit resolution and can never reach 360°. The maximum duty cycle high period is:

$$DutyCycleMax\ (\%) = (4095 / 4096) \times 90 + 5\ .$$

PWM CARRIER FREQUENCY

The PWM carrier frequency is controlled via two EEPROM fields, both of which are found in the PWS row.

- PWM_FREQ
- PWM_BAND

Together, these two fields allow 128 different PWM carrier frequencies to be selected.

Table 1: PWM Carrier Frequencies in Hz

		PWM_BAND							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PWM_FREQ	**0**	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

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ERROR REPORTING IN PWM

The PWM output can be configured to change state if certain errors occur. There are three options:

- No error reporting
- Tristate the PWM
- Halve the carrier frequency and represent the error via different duty cycles

Two EEPROM bits, PEO and PES, control how errors are reported in PWM mode. Both PEO and PES are in the PWS address row of EEPROM:

Table 2: PWM Error Output Enable Option (PEO)

Code	Description
0	PWM does not respond to errors.
1	PWM output responds to errors as selected with the PES field.

Table 3: PWM Error Select (PES)

Code	Description
0	PWM tristates on an error.
1	PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

The error priority and corresponding duty cycle are shown in Table 4, with the high-priority error dictating the PWM duty cycle.

Each error is individually enabled for PWM reporting, so that only events of interest interrupt the device output. These enable bits may be found within the PWE (0x18) EEPROM row.

Table 4: PWM Error Duty Cycle and Priority

Error	Priority	Duty Cycle %	Description / Persistence
WDE	1 (highest)	5	Watchdog error. Permanent.
EUE	2	10.625	EEPROM uncorrectable error.
STF	3	16.25	Self-test failure. Permanent.
PLK	4	21.875	PLL not locked. Persists until PLL locks.
ZIE	5	27.5	Zero-crossing integrity error. Persists until goes away.
AVG	6	33.125	Angle averaging error. Outputs once then clears.
UV	7	38.75	Undervoltage (UVA and/or UVCC dependent on serial error masks). Persists until no unmasked undervoltage.
MSL	8	44.375	Persists until field strength higher than low threshold.
ESE	9	50	EEPROM correctable error. Outputs once then clears.
SAT	10	55.625	Persists until no saturation warnings.
MSH	11	61.25	Persists until field strength lower than high threshold.
TR	12	66.875	Persists until temperature within range.
TOV	13	72.5	Persists until cleared via the serial CTRL register.

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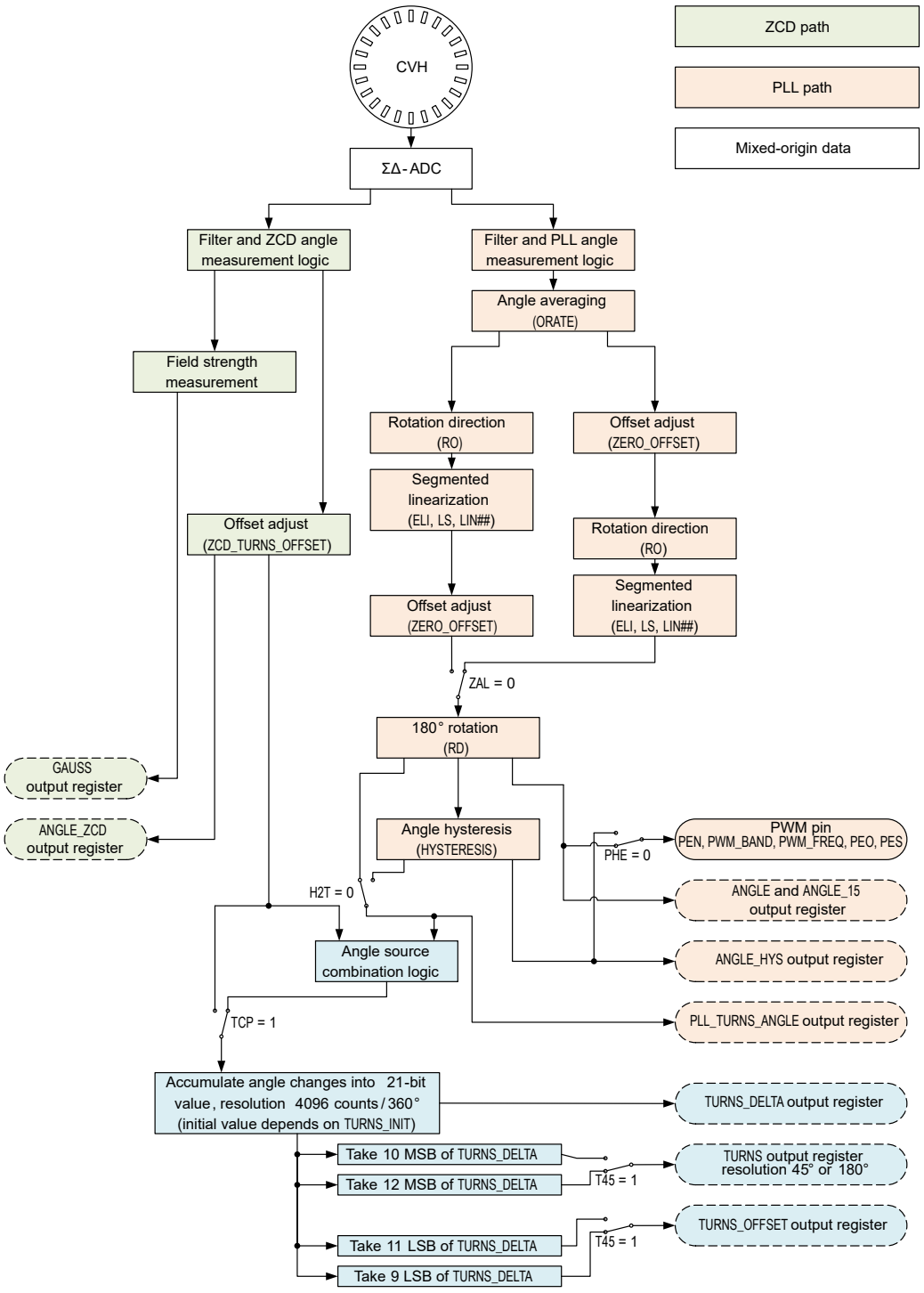

Figure 9: Angle Measurement—Sensor Readout Steps

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Linearization

The A33003 contains linearization functionality. Linearization allows for conversion of the initially sensor-measured magnetic field data into customer-desired linear output. This can be used to correct minor imperfections in the encoder signal, or to allow motor commutation in side-shaft measurement setups.

Linearization converts the electrical angles (the angle as measured by the sensor front end) into mechanical angles (the actual angle of the encoder signal).

To use the linearization feature, it is most convenient to use the Allegro A33003 Samples Programmer Graphical User Interface (GUI). [1] It allows the user to measure points along the mechanical rotation, calculate all parameters that need to be written into the sensor, and write these values into the sensor. To use this function, the user must be able to read and control the mechanical angle.

The sensor performs linearization by taking the measured electrical angles and, depending on the angle measured, subtracting a linearization coefficient stored in EEPROM. There are 32 of these linearization coefficients in the EEPROM. The angle value at a sensor angle reading of 0.00, 11.25, 22.50, … 348.75 electrical degrees become modified by the values in EEPROM fields LIN0, LIN1, LIN2, … LIN31. The EEPROM LIN values are subtracted from the electrical sensor angles, as shown in Table 5.

The LIN fields are 12-bit signed values. Each LIN coefficient has a range of –2048…+2047 LSB that corresponds to a correction of the electrical angle by +22.50…–22.49 degrees (EEPROM field LS = 0) or by +45.00…–44.98 degrees (EEPROM field LS = 1). When the electrical angle is between two of the linearization points, the sensor calculates the appropriate correction value for this angle by linear interpolation between the two coefficients next to the value. For example, if the sensor measures an angle of 5.625°, the output is 5.625 – (LIN0 + LIN1)/2.

An example of a nonlinear curve that is corrected by the sensor is shown in Figure 10. In this example, the values of LIN0 through LIN4 are positive numbers, while LIN5 and LIN6 are negative numbers. The straight-line interpolation between LIN points typically gives rise to some residual error because the device fits a line to a nonlinear error profile, as shown in Figure 11.

The output delay of the A33003 is not affected by enabling or disabling linearization. If linearization is disabled, the EEPROM LIN fields can be used for other customer purposes.

Table 5: Linearization Coefficients

Electrical Angle (°) Measured by Sensor	Correction Value Written in EEPROM	Output Angle Visible on Sensor Output
0.00	LIN0	Output = 0.00 – LIN0
11.25	LIN1	Output = 11.25 – LIN1
22.50	LIN2	Output = 22.50 – LIN2
33.75	LIN3	Output = 33.75 – LIN3
45.00	LIN4	Output = 45.00 – LIN4
56.25	LIN5	Output = 56.25 – LIN5
67.50	LIN6	Output = 67.50 – LIN6
78.75	LIN7	Output = 78.75 – LIN7
90.00	LIN8	Output = 90.00 – LIN8
101.25	LIN9	Output = 101.25 – LIN9
112.50	LIN10	Output = 112.50 – LIN10
123.75	LIN11	Output = 123.75 – LIN11
135.00	LIN12	Output = 135.00 – LIN12
146.25	LIN13	Output = 146.25 – LIN13
157.50	LIN14	Output = 157.50 – LIN14
168.75	LIN15	Output = 168.75 – LIN15
180.00	LIN16	Output = 180.00 – LIN16
191.25	LIN17	Output = 191.25 – LIN17
202.50	LIN18	Output = 202.50 – LIN18
213.75	LIN19	Output = 213.75 – LIN19
225.00	LIN20	Output = 225.00 – LIN20
236.25	LIN21	Output = 236.25 – LIN21
247.50	LIN22	Output = 247.50 – LIN22
258.75	LIN23	Output = 258.75 – LIN23
270.00	LIN24	Output = 270.00 – LIN24
281.25	LIN25	Output = 281.25 – LIN25
292.50	LIN26	Output = 292.50 – LIN26
303.75	LIN27	Output = 303.75 – LIN27
315.00	LIN28	Output = 315.00 – LIN28
326.25	LIN29	Output = 326.25 – LIN29
337.50	LIN30	Output = 337.50 – LIN30
348.75	LIN31	Output = 348.75 – LIN31

[1] Available for download via the Allegro Software Portal at https://registration.allegromicro.com/login

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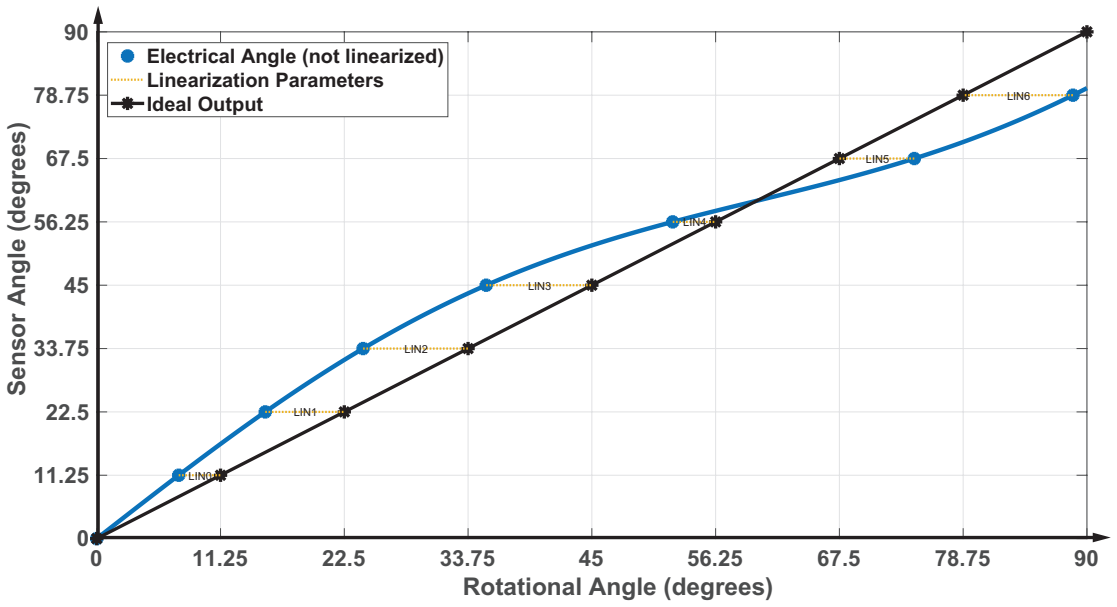

Figure 10: Linearization Example

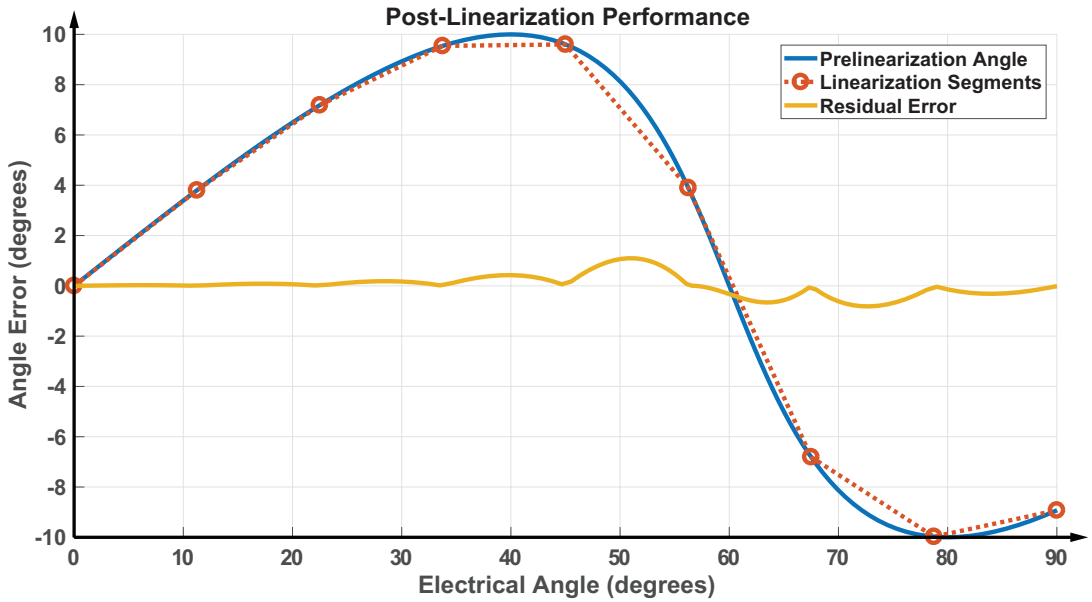

Figure 11: Post-Linearization Error

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Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the A33003, the hysteresis field (ANG.HYSTERESIS) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$ANG.HYSTERESIS \times (360/16384) \text{ degrees},$$

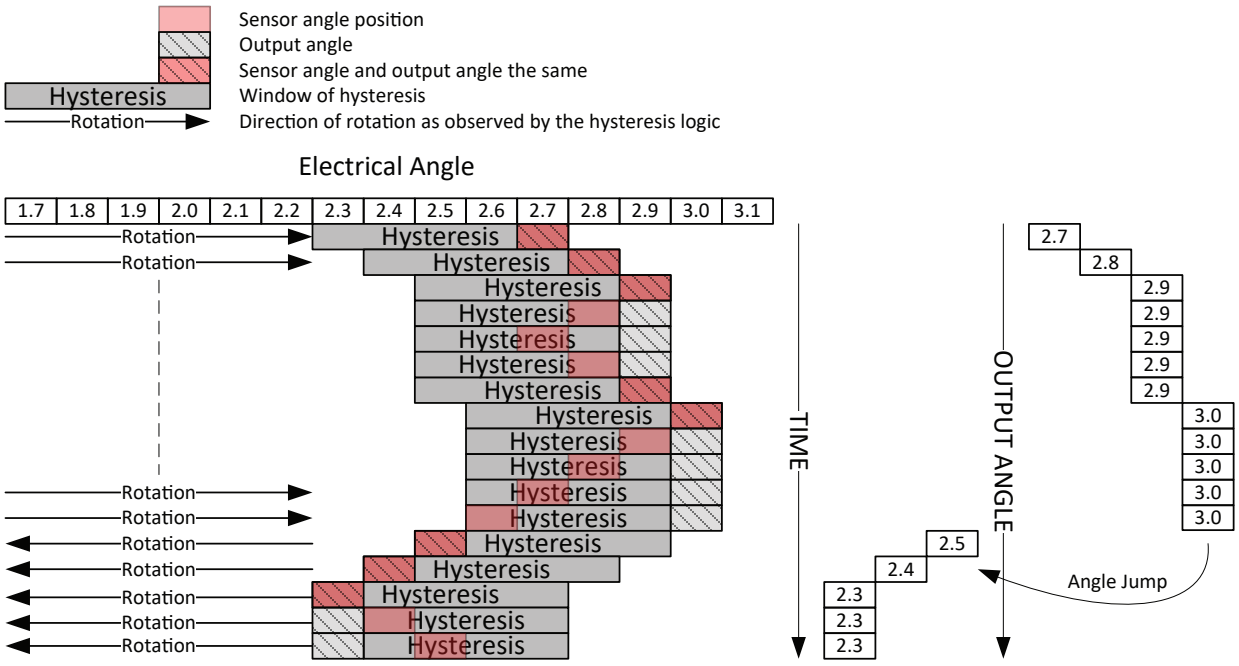
giving a range of 0 to 1.384 degrees.

On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.ANGLE_HYS) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 12. The current angle position as measured by the sensor is at the “head” of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle is the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the “head” was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or “head” for the purposes of hysteresis, is viewable via the STA.ROT bit, where 0 is in the increasing angle direction, and 1 is in the decreasing angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle skips consecutive resolution steps.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle tends to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., toward the current “head”), rather than to the average position of the jitter.



NOTE: The rotation direction resets to 0, or increasing angle direction. At power-up or after LBIST, the hysteresis window is always behind the initial angle position; so, if hysteresis is enabled, a decreasing angle direction of rotation does not register until the hysteresis window has passed.

Figure 12: Effect of Hysteresis

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Turns Counting

Certain automotive angle-sensing applications involve the magnetic target rotating multiple times. Thus, tracking the turns of the measured magnet becomes more important than knowing the specific angle at which the target sits. Examples of such applications include:

- Seat-belt passive safety systems
- EPS motor position

This implementation can also be used to measure exact angle in cases where the rotation is geared-up such that a slight angle rotation of the device of interest results in multiple rotations of a target magnet that the sensor is measuring. For this reason, the A33003 includes a circuit that counts the rotational turns of a magnet. This feature also includes the ability to start up with a preset value, allowing the turns counter to persist through powered-down periods, when combined with adequate system-level control. Traditionally, recovering the turns counter value was achieved by a combination of relatively complex mechanical and electrical components. The A33003 can help reduce system-level complexity and eliminate many system components by performing both the absolute angle measurement and the tracking of turns.

It is possible to use the zero-crossing diode (ZCD) signal path as the turns-counter source. This is performed by setting the TCP field in EEPROM to 0.

To read the total position of the magnetic encoder (angle in 12-bit resolution, as well as additional revolutions in 9 bits, sign-extended to 12 bits), a serial register TURNS_DELTA is provided. This 24-bit word accumulates the total changes in angle. The initial value of the register (zero, current angle, or current angle with TURNS_COUNT zeroed) can be controlled using the EEPROM field TURNS_INIT, as detailed in Figure 14.

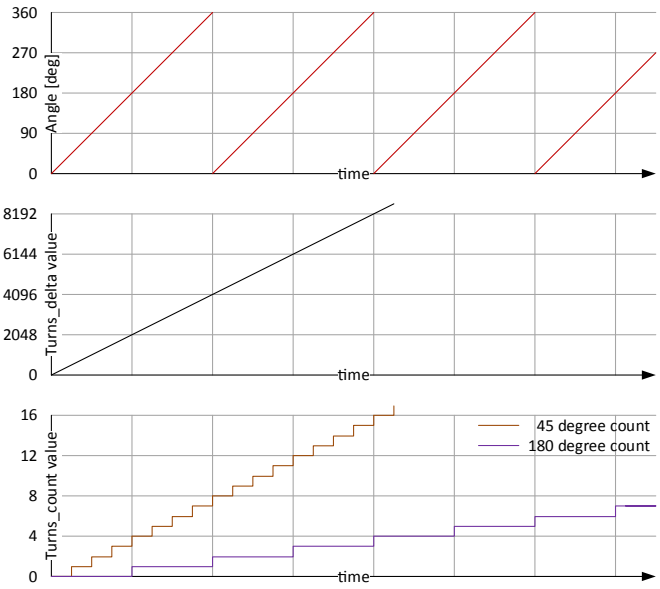

Figure 13: Turns Counting

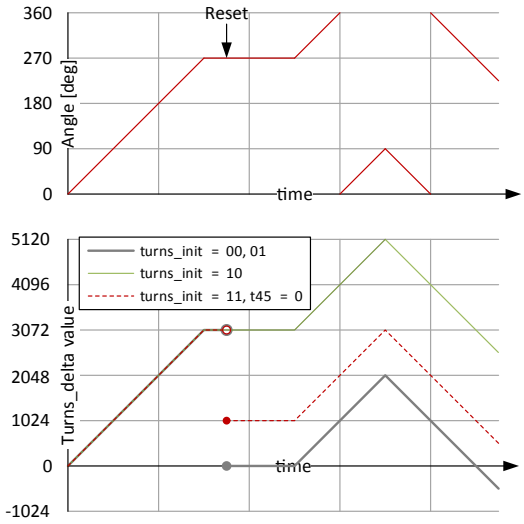

Figure 14: EEPROM field TURNS_INIT

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Turns Counting Behavior on Power-Up

Turns tracking, as measured by the IC, is derived from the TURNS_DELTA register. This is a 21-bit register that tracks absolute angle across multiple magnetic rotations by tracking change in angle from a reference position. The actual TURNS register (address 0x2C) is simply the upper bits from the TURNS_DELTA value. When configured in 180° turns mode (i.e., T45 = 0), the upper 10 bits are used; if in 45° mode (i.e., T45 = 1), the upper 12 bits are used to indicate the turns. The A33003 is capable of tracking up to –512/+511 turns in 180° mode and –2048/+2047 in 45° mode.

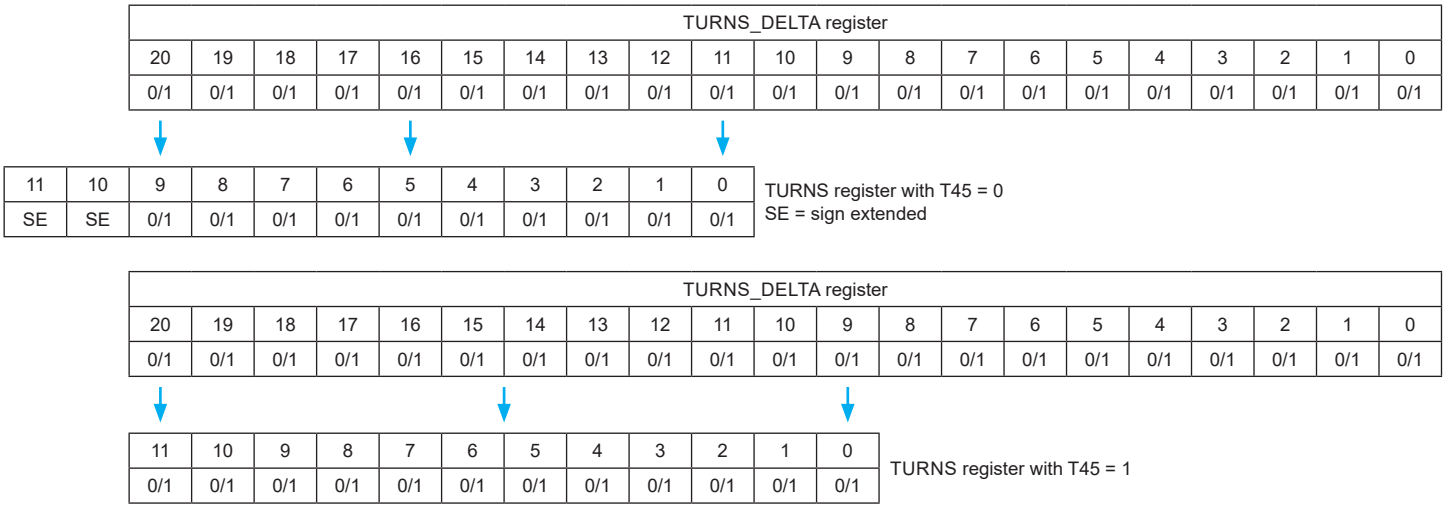

Figure 15: Turns Register

The reference position from which the turns_delta is measured impacts the initial turns count value. The TURNS_INIT field has the following options controlling this:

Table 6: turns_init (EEPROM 0x1D bits 19:18)

turns_init	Description
00	Turns counter is zeroed on power-up. Turns are tracked relative to the angle observed on power-up. TURNS_DELTA = 0 at power-up.
01	
10	Turns counter is set relative to the defined 0 position of the sensor, which may be a nonzero number. TURNS_DELTA is set to the angle observed on power-up.
11	Turns counter value initialized to zero, but increments on the 0°/180° or 45° boundaries as observed by the IC (set via the T45 field). TURNS_DELTA register is initialized with an offset based on the T45 register.

Control of the starting turns count value via the TURNS_INIT field is illustrated in Figure 14, where the angle constantly increases up to 270°, after which a sensor reset occurs.

For a TURNS_INIT value of 00_2 or 01_2, the TURNS_DELTA register measures the change in position relative to the observed angle on power-up. As such, the value of the turn is initialized to 0 on sensor reset.

When TURNS_INIT = 10_2, the turns_delta value represents the difference in position relative to the sensor's defined 0° position; put more simply, the TURNS_DELTA is initialized to the angle observed on power-up. As shown in Figure 14, once the reset occurs, the TURN_DELTA register is loaded with 3072 codes, which is 270° in 12-bit resolution. Depending on the T45 setting, this is reflected as a turn value of 1 (in 180° mode) or 6 (in 45° mode).

When TURNS_INIT = 11_2, the turns count is initialized to 0, and the increment/decrement points for turns counting are fixed to either the 0°/180° or the 0°/45°/90°/135°/180°/225°/270°/315° boundaries, based on the T45 field. The TURNS_DELTA register becomes loaded with the angular distance between two adjacent boundaries (0°/180° or a multiple of 45°). For example, in Figure 14, the T45 bit = 0, enabling 180° mode. The value of the turn, in this case, is 0. The angle on power-up is 270°, which is 50% between 180° and 360°; to reflect this, the TURNS_DELTA register is loaded with 1024 codes indicating it is halfway between one turn (i.e., 180° in 12-bit resolution, or 2048 codes).

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Setting the Turns Count Value

There are two ways to modify the value of the turns counter.

- Using the turns counter reset function
- Writing the TURNS_DELTA value to register EWD and loading it into TURNS_DELTA

INVOKING A TURNS COUNTER RESET

Resetting the turns counter is a command invoked using the SPECIAL field of the CTRL register.

CHANGING OR RESTORING TURNS_DELTA VALUE

It is possible to load a desired value into the turns counter register. This may be useful if a certain externally stored value should be set again following a power loss. The turns counter register itself cannot be written directly. Instead, the writing action is an indirect one using the following steps:

1. Before writing, ensure the system is stable, as indicated by the STA.AOK bit field.
2. Write the desired 21-bit value of TURNS_DELTA into the EWDH and EWDL serial registers in little-endian format. Example:
   A. To set the TURNS_DELTA to value 10441.32° (29 rotations and 1.32° current angle), write (10441.32 / 360) × 4096 = 118799 = 0x01D00F.
   B. Write the lower 16 bits into the EWDL register and the upper 5 bits into the EWDH register, with leading zeroes to make the 16-bit value to write. This results in writing 0x0001 to EWDH (0x04:0x05) and 0xD00F to EWDL (0x06:0x07).
3. Write the value 0x03 to the SPECIAL field, and write 0x46 to the INITIATE_SPECIAL field.
4. The sensor behavior to process the setting depends on the setting of the TURNS_INIT EEPROM field:
   A. When TURNS_INIT = 00_2 or 01_2, the value is copied to TURNS_DELTA, and subsequent angle changes accumulate on top of this value. Because small offset changes/noise errors accumulate every time such a write is performed, this method is not recommended for scenarios where the saved value must be restored.
   B. When TURNS_INIT = 10_2 or 11_2, the value is compared to the currently sensed angle. The TURNS_DELTA field "snaps" to the closest value matching the sensed angle. Errors in position of <180° are removed this way. This method is recommended if a saved turns count value must be restored, but the measured angle may have changed slightly in the meantime.

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DEVICE PROGRAMMING INTERFACE

The A33003 can be programmed in two ways:

- Using the *SPI interface* for input and output
- Using a *Manchester protocol* on the VOUT pin.

The A33003 features an internal charge pump and does not require high-voltage pulses to write to EEPROM.

All setting fields and all data fields of the sensor can be read and written using both protocols. Locking the EEPROM from changes locks EEPROM write access from both protocols.

A separate setting to completely disable the Manchester interface is available in the PWS.DM field of the EEPROM. Using this setting causes the sensor to ignore any commands entered using Manchester protocol. The SPI interface does not become disabled by disabling the Manchester interface.

For details regarding the programming procedures, contact your Allegro representative.

SWITCHING BETWEEN THE DIFFERENT OUTPUT PROTOCOLS

The A33003 supports four output protocols (SPI, Manchester, SENT, PWM), all of which overlap with the same pin. Below is the hierarchy of precedence for control of the MISO pin.

- SPI, when set with SPO bit within the serial register.
- Manchester communication (when the auxiliary interrupt pulse is sent).
- PWM, when set via the PWS.PEN bit in EEPROM.
- SENT, when enabled via the SENT_MODE field in EEPROM.
- Manchester, when neither PWM or SENT is enabled;
  SPI, when Manchester is disabled.

When the SPO bit is set, the SPI interface immediately overrides all other output protocols—this includes Manchester. If this bit is set via the Manchester interface, the device ends the Manchester interface and stops responding to Manchester communication until SPO is cleared.

INTERFACE STRUCTURE

The primary serial interface registers are used for direct writes and reads by the host controller for frequently required data. All forms of communication operate through these registers, whether it be via SPI or Manchester. These registers also provide a data and address location for accessing extended memory locations under control of the onboard processor.

EEPROM writing requires additional procedures. For more information, see the EEPROM and Shadow Memory Use section or contact your Allegro representative.

SPI Interface

The setup for programming using the SPI interface is given in Figure 16.

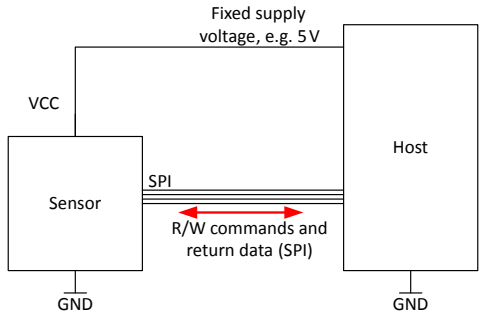

Figure 16: SPI Interface Programming Setup

SPI INTERFACE TIMING

The SPI interface operates in pure peripheral mode, with the controller controlling the SCLK, MOSI, and CS lines. The controller can maximize data throughput, up to $f_{SCLK(max)}$ of 10 MHz. The timing for read and write cycles is shown in Figure 17 and Figure 18.

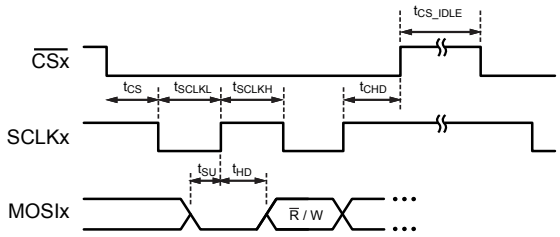

Figure 17: A33003 SPI Interface Timings Input

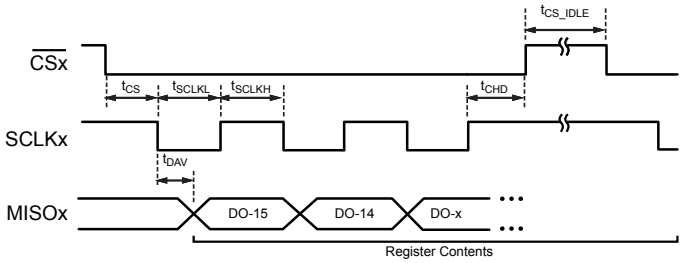

Figure 18: A33003 SPI Interface Timings Output

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SPI MESSAGE FRAME SIZE

The SPI interface requires either 16-, 17-, or 20-bit packet lengths. The extended 20-bit SPI packet allows 4-bit CRC to accompany every data packet. The 17-bit packet is only allowed when the EEPROM/shadow bit S17 = 1.

The purpose of the 17-bit SPI option is to allow a delayed reading of the MISO line on the host side. Some hosts allow data to be sampled from the peripheral on the falling edge of SCLK. This is typically performed in the case of long interface delays caused by large line capacitances or very long cables. Due to the sampling on the falling edge, an additional 17th clock is required for the 16 bits of data.

If more or less clock pulses than expected are detected by the sensor during a SPI transaction, the interface warning, WARN.IER, becomes set. This occurs for anything other than 16 or 20 when S17 = 0, or anything other than 17 when S17 = 1.

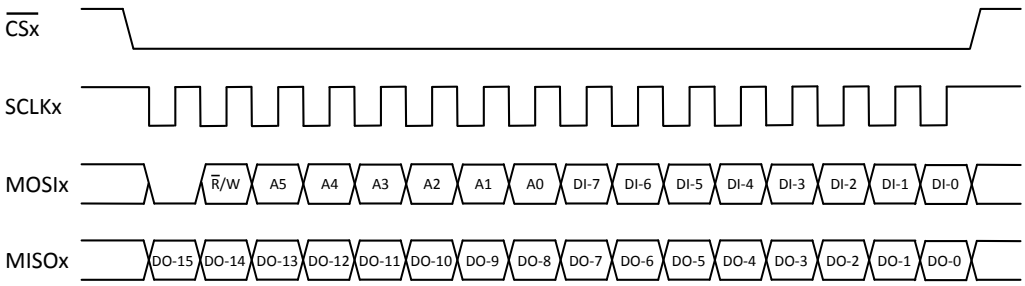

Figure 19: Sixteen-Bit SPI Transaction

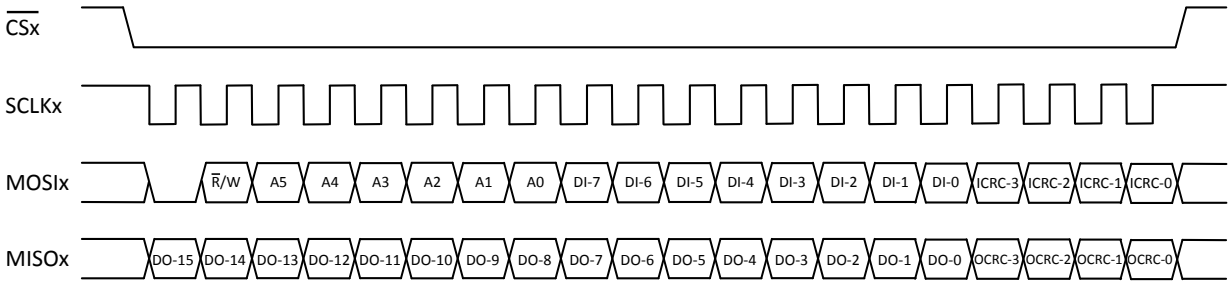

Figure 20: Twenty-Bit SPI Transaction

SPI OUTPUT VOLTAGE LEVELS

The A33003 can operate in either 3.3 or 5 V SPI mode. Contact Allegro MicroSystems for more information.

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WRITE CYCLE OVERVIEW

Write cycles consist of a 1-bit low, a 1-bit R/W asserted high, 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16-bit serial register, two write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the controller-generated SCLK signal. The complete SPI packet is latched on the rising edge of the controller-generated ($\overline{CS}$) signal.

The simultaneous MISO signal output represents the contents of the corresponding die SPI read packet, including 16 data bits and 4 optional CRC bits—automatically included if a 17th SCLK edge is detected. The data bits correspond to the register contents selected during the previous read command. If the previous command was a write command, the device, by default, outputs the angle register (0x20). If no previous command was sent, i.e., the first SPI packet after POR, the data sent by the device is indeterminate.

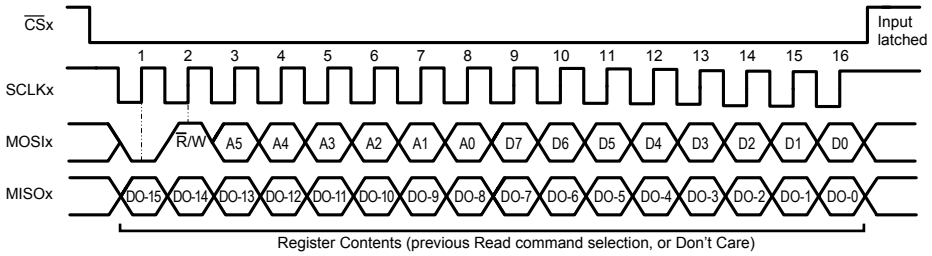

Figure 21: SPI Write Example

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READ CYCLE OVERVIEW

Read cycles have two stages: a read command to select a serial register address, followed by another read command to transmit the data from the selected register. Both commands consist of a 1-bit low, a 1-bit R/W asserted low, 6 address bits identifying the target register, and 8 data bits (all zeroes because no data is being written).

In the first stage, as with the write command, read command MOSI bits are clocked-in on the rising edge of the controller-generated SCLK signal and data-latched on the rising edge of the ($\overline{CS}$) signal. During the first read stage, the simultaneous MISO signal output is the content of the SPI read data from the previous read command.

In the second stage, the read command continues on the next falling edge of the controller-generated ($\overline{CS}$) signal. The MISO bits are the contents of the register selected during the first stage, read 16 bits at a time. The MISO bits transmit on the falling edge of the SCLK signal, such that the controller can sample them on the SCLK rising edges.

Because a SPI read can transmit 16 data bits at one time and the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register may be transmitted with one SPI frame. This is accomplished by providing an even serial address value. If an odd value address is sent, only the contents of the single byte are returned, with the 8 MSBs within the SPI packet set to zero.

Example: To read all 16 bits of the error register (0x24:0x25), send a SPI read request with the address bits set to 0x24. If only the 8 LSBs are desired, use the address 0x25.

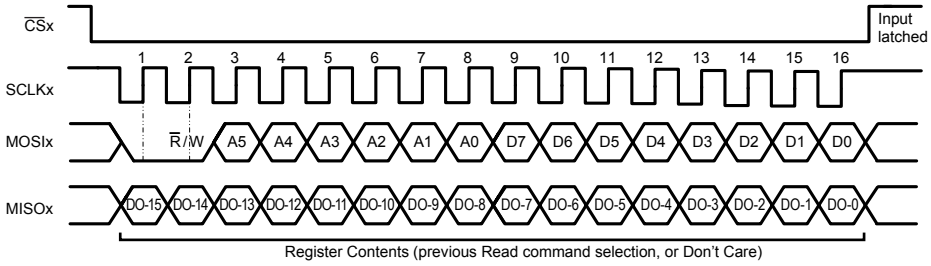

Figure 22: SPI Read Example, Register Selection

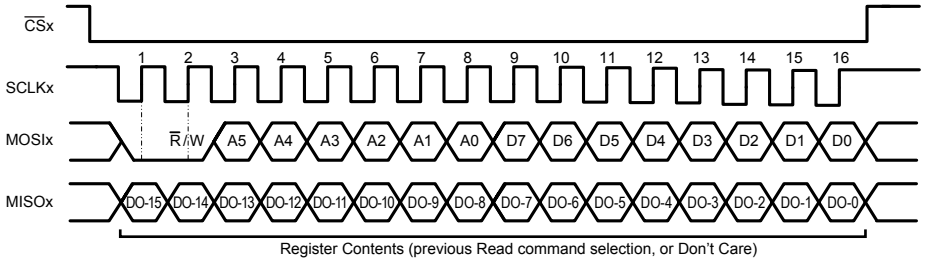

Figure 23: SPI Read Example, Data Output From Selected Register

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CRC

To check the data coming from the sensor, 20-bit SPI frames can be used. Without additional setting required, a 4-bit CRC is automatically generated and placed on the MISO line if more than 16 bits are read from the sensor.

The four additional CRC bits on the MOSI line coming from the host are ignored by the sensor, unless the PWS.SC bit is set within EEPROM (0x1B, bit 0). When the incoming CRC check is enabled, an incoming SPI packet with an incorrect CRC is discarded, and the CRC error flag is set in the WARN.CRC serial register.

The CRC is based on the polynomial $x^4 + x + 1$ with the linear feedback shift register preset to all ones. The 16-bit packet is shifted through from bit 15 (MSB) to bit 0 (LSB). The CRC logic is shown in Figure 24. Data are fed into the CRC logic with MSB first. Output is sent as C3-C2-C1-C0.

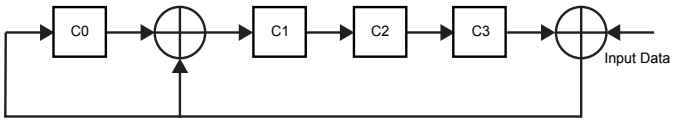

Figure 24: SPI CRC

The CRC output by the sensor on the MISO pin is always correct. The CRC from the host on the MOSI pin must be correct if the CRC enable bit PWS.SC in the EEPROM was set.

NOTE: If the extended read data (ERD) register is read before the ERCS.ERD bit indicates a read has completed, there is a possibility of a CRC error, because the data could change during the read. Do not read the ERD register until it is known to be stable, as evidenced by either an indication that the read is complete or sufficient passage of time.

The CRC can be calculated with the following C code:

```
/*
* CalculateCRC
*
* Take the 16-bit input and generate a 4-bit CRC
* Polynomial = x^4 + x + 1
* LFSR preset to all 1's
*/
uint8_t CalculateCRC(uint16_t input)
{
    bool CRC0 = true;
    bool CRC1 = true;
    bool CRC2 = true;
    bool CRC3 = true;
    int  i;
    bool DoInvert;
    uint16_t mask = 0x8000;

    for (i = 0; i < 16; ++i)
    {
        DoInvert = ((input & mask) != 0) ^ CRC3;
        CRC3 = CRC2;
        CRC2 = CRC1;
        CRC1 = CRC0 ^ DoInvert;
        CRC0 = DoInvert;
        mask >>= 1;
    }

    return (CRC3 ? 8U : 0U) + (CRC2 ? 4U : 0U) + (CRC1 ? 2U
: 0U) + (CRC0 ? 1U : 0U);
}
```


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Manchester Serial Interface

The A33003 incorporates a serial interface shared with the standard output line (VOUT). (Note: The A33003 may be programmed via SPI, with additional wiring connections). This interface allows an external controller to read and write to registers in the A33003 EEPROM and volatile memory without the need for the host controller to control V_{CC} or to share the same V_{CC} line. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0, and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0/SA1 pins to set address values for each die. In this way, individual communication with up to four A33003 die is possible per line.

To prevent any undesired programming of the A33003, the serial interface can be disabled by setting the disable Manchester bit (PWS.DM EEPROM address 0x1B, bit 3) to 1. With this bit set, the A33003 ignores any Manchester input commands.

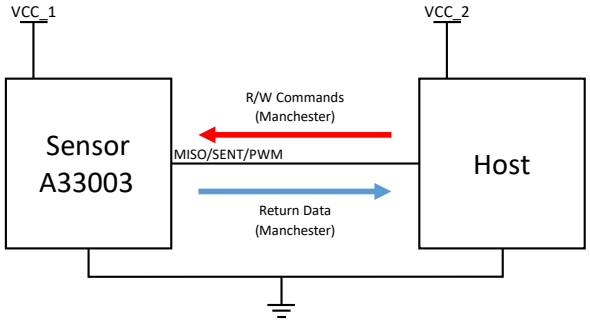

Figure 25: Manchester Interface Programming Setup

ENTERING MANCHESTER COMMUNICATION MODE

Provided the disable Manchester bit is not set in EEPROM, there are two ways to begin Manchester communication:

1. If PWM, SENT, and SPO are disabled, and if Manchester is the active communication protocol, only the Manchester entry code on the VOUT pin is required to begin Manchester communication.
2. If PWM or SENT protocols are enabled, the Manchester auxiliary interrupt pulse or auxiliary function (F_AUX) pulses must be used, followed by the Manchester entry code. Once this has been completed, Manchester communication is enabled. If no entry code is received after an auxiliary interrupt pulse or F_AUX pulse for t_{msgRX}, the Manchester interface times out, and the device returns to its previous operating state.

   NOTE: If the MEPE bit = 0, the auxiliary interrupt pulse and F_AUX pulses are disabled. Because of this, Manchester communication is not possible when PWM or SENT are active.

Once the Manchester communication mode is entered, the VOUT pin ceases to provide angle data, interrupting any data transmission in progress. After this, the Manchester interface only responds to two specific codes: the access and exit codes. If the access code is sent, the Manchester interface becomes fully active and responds to all commands. If the exit code is sent, the Manchester interface closes all access and the previous protocol resumes control of the PWM pin or SENT pin, as determined by EEPROM. Both the access and exit codes must be written to address 0x3F (address field composed of all ones).

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MANCHESTER AUXILIARY INTERRUPT PULSE FOR PWM OUTPUT MODE

To initialize communication using the Manchester auxiliary command when the A33003 is configured with PWM output, the auxiliary interrupt pulse can be applied at any time. The auxiliary pulse must have a minimum width of t_{HOLD}, after which the pulse is released for t_{GATE} plus the rise time to allow the line to pull high and the device to register a rising edge. After this, the controller must pull low for t_{GATE} before beginning to send the Manchester access code. If the first rising edge of the Manchester access code is not observed by the device before t_{msgRX} after the hold time, the device times out, aborts Manchester initialization, and returns to PWM functionality. The Manchester auxiliary command for PWM output is shown Figure 26.

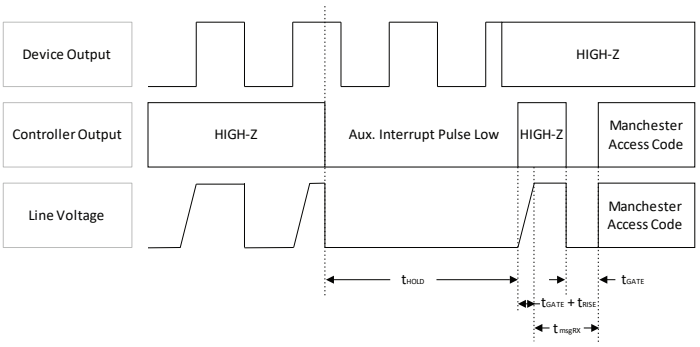

Figure 26: Auxiliary Interrupt Pulse Waveform

MANCHESTER AUXILIARY COMMAND FOR SENT AND TSENT OUTPUT MODE

To initialize communication using the Manchester auxiliary command when the A33003 is configured with SENT or TSENT output, the auxiliary interrupt pulse can begin at any time between the start of the synchronization (sync) pulse and the end of the last data nibble pulse. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to pull high, followed by a low period of t_{GATE} before sending the Manchester access code. Again, if the first rising edge of the Manchester access code is not observed before t_{msgRX}, the device times out, Manchester initialization aborts, and the device returns to typical functionality. The Manchester auxiliary command for SENT and TSENT output is shown Figure 27.

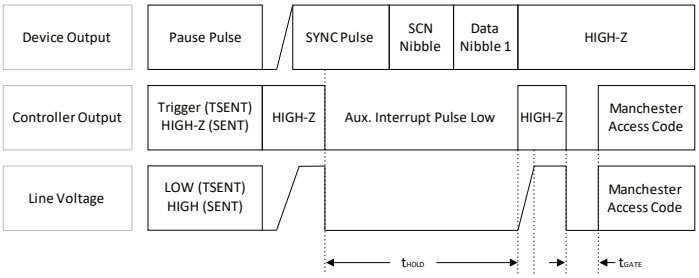

Figure 27: Interrupt Waveform for SENT and TSENT Output

OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Access Code Timeout	t_{msgRX}			–	–	300	µs
Interrupt Pulse Hold Time	t_{HOLD}	SSENT—Short	F_AUX	50	–	83	ticks
		SSENT—Long	F_AUX	196	–	297	ticks
		ASENT	F_AUX	50	–	80	ticks
		SENT	Aux. interrupt pulse	30	–	–	ticks
		TSENT	Aux. interrupt pulse	30	–	–	ticks
		PWM	Aux. interrupt pulse	2 × PWM period [1]	–	–	µs
Deglitch Gate Time	t_{GATE}			1.0	–	–	µs

[1] The minimum hold time for the auxiliary interrupt, when the output is set for PWM, is double the PWM period. If the PWM frequency increases as a result of a diagnostic condition, the hold time is double the new PWM period at the diagnosis frequency.

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Manchester Message Structure

The general format of a command message frame is shown in Figure 28. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of 0 is indicated by a rising edge within the bit boundary.

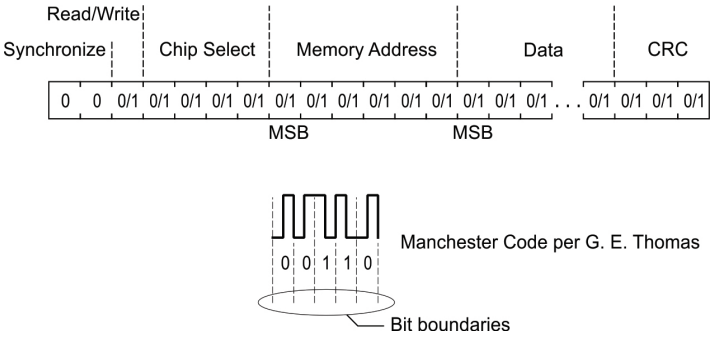

Figure 28: General Format for Serial Interface Commands

A brief description of each bit is provided in Table 7.

Table 7: Manchester Command General Format

Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
4	Chip Select	0/1	Used to select a set of target chips/die, based on ID value.
6	Address	0/1	[Read/Write] Serial address
16	Data	0/1	Requested serial register contents (write operation only)
3	CRC	0/1	Incorrect value indicates errors

When the A33003 is operating in I²C Mode (ISEL pin set to a logic low), the die ID value is determined by the state of the SA0 and SA1 pins.

Table 8: Pin Values

SA1	SA0	ID Value
0	0	ID0
0	1	ID1
1	0	ID2
1	1	ID3

Using the 4 bits of the chip select field, die can be selected via their ID value, allowing up to four die to be individually addressed and providing for different group addressing schemes. If the chip select field is composed of all zeroes, or if the A33003 is operating in SPI mode (ISEL pin set to a logic high), no ID comparison is made, allowing all A33003 devices to be addressed at once.

Example: If the chip select field is 1010, all die with ID3 or ID1 are selected.

Note: If sharing a SENT line with multiple chips/dies, reading must be performed one die at a time.

Table 9: Chip Select

Chip Select			
ID3	ID2	ID1	ID0

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MANCHESTER AUXILIARY COMMAND FOR SSENT AND ASENT OUTPUT MODE

To initialize communication using the Manchester auxiliary command when the A33003 is configured with SSENT or ASENT output, the auxiliary function (F_AUX) pulse is applied as the frame request pulse. The auxiliary function pulse must have a minimum width of t_{HOLD}. After the pulse is released, the output line is required to go HIGH-Z for t_{GATE} plus the rise time. The controller must then pull the output line low for t_{GATE} before sending the Manchester access code. If the first rising edge of the access code is not recognized before t_{msgRX}, a timeout occurs, the Manchester initialization aborts, and the output returns to typical functionality.

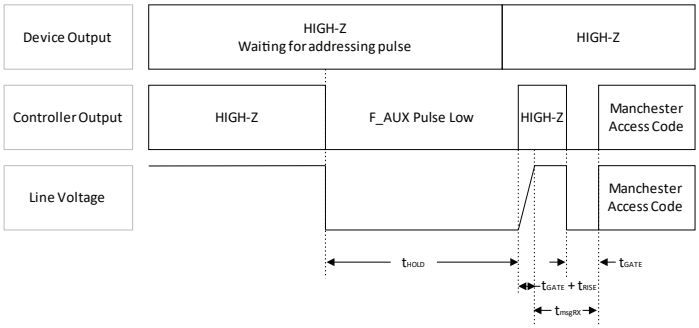

Figure 29: Interrupt waveform for SSENT and ASENT output

ACCESS CODES

Once the device is set up to recognize Manchester communication, there are two special Manchester codes used to activate or deactivate the serial interface:

1. Manchester access code: This code (equivalent to performing a write to register: 0x3F with data: 0x62D2) must be sent to fully begin Manchester communication. Once this is performed, the Manchester interface responds to all available Manchester commands.
2. Manchester exit code: This code (equivalent to writing to register: 0x3F with data: 0x0000), when sent, exits Manchester communication and returns the device to its previous state.

Once the Manchester communication mode is exited, the output pin returns to outputting angle data (provided no flag is asserted). This output data is taken directly from the transmission in progress. The recommendation when exiting Manchester communication is to disregard the first angle reading and to wait for the start of the next PWM duty cycle or SENT packet, as applicable.

TRANSACTION TYPES

The A33003 never initiates communication. Four transactions are recognized: write access, write to EEPROM, write to volatile, and read. Only the read transaction prompts the A33003 to respond with data. When responding to a read command, the A33003 does not check for line contention; it is the responsibility of the controller to release the line in time and be ready to read the data sent by the A33003.

After a read command is received, there is a delay time between when the last bit of the command is sent to the device and when the device begins to respond on the line. This delay is divided into two times.

- The first (t_d) is the delay between the last bit of the read command and when the device begins to pull the line low in preparation to send data.
- The second (t_b) is the delay between the time when the device pulls the line low to when it begins outputting the data. While the output is fully readable as long as the controller releases control before $t_d + t_b$, release of the line is recommended before t_d.

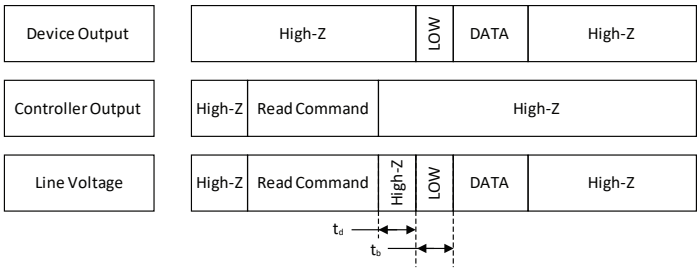

Figure 30: Transaction Types

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READING DATA USING MANCHESTER ENCODING

A read command with the desired register number is sent from the controller to the A33003. The device responds with a read response frame using the Manchester protocol.

In addition to the contents of the requested memory location, a return status field is included with every read response. This field provides the ID used to communicate with the part and any errors that may have occurred during the transaction. These bits are:

- **ID**: ID (SA1, SA0) unless BC = 1 (ID is 00).
- **BC**: Broadcast; ID field was zero.
- **AE**: Abort error; edge detection failure after sync detect.
- **OR**: Overrun error; a new Manchester command has been received before the previous request could be completed.
- **CS**: Checksum error; a prior command had a checksum error.

Table 10: Return Status Bits

Return Status Bits (6 bits)					
5	**4**	**3**	**2**	**1**	**0**
ID		BC	AE	OR	CS

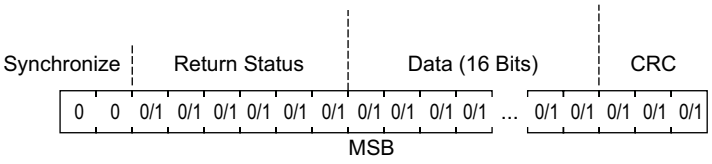

Figure 31: Manchester Read Response

The following command messages can be exchanged between the device and the external controller:

- Manchester access code
- Manchester exit code
- Read
- Read response
- Write

For EEPROM address information, refer to the EEPROM Reference section. For serial address locations, refer to the Primary Serial Interface Registers Reference section.

ERROR CHECKING

The serial Manchester interface uses a cyclic redundancy check (CRC) for data bit error checking (synchronization bits are ignored during the check).

The CRC algorithm is based on the polynomial:

$$g(x) = x^3 + x + 1,$$

and the calculation is represented graphically in Figure 32.

The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

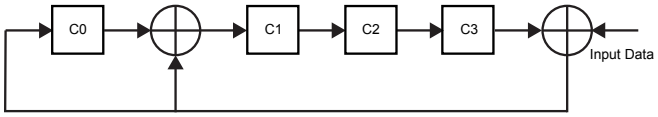

Figure 32: Manchester CRC Calculation

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Table 11: Manchester Access Code

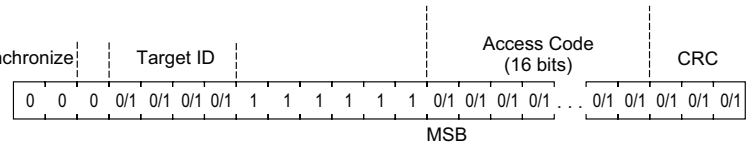
Function	Transmits the access code to the A33003. Enters serial communication mode with the desired output protocol.
Syntax	Sent by the external controller on the A33003 output pin.
Related Commands	Related command: Serial exit code
Pulse Sequence	
Options	Access Codes: Manchester access code = 0x62D2 Selects Manchester output on the PWM pin.
Examples	The Manchester access code operates as a broadcast pulse, meaning the target ID field is inconsequential. For example, if two A33003s configured with ID0 and ID2 respectively are sharing a common SENT line, a Manchester access code with a target ID value of 0x1 results in both sensors entering Manchester serial communication mode.

Table 12: Manchester Exit Code

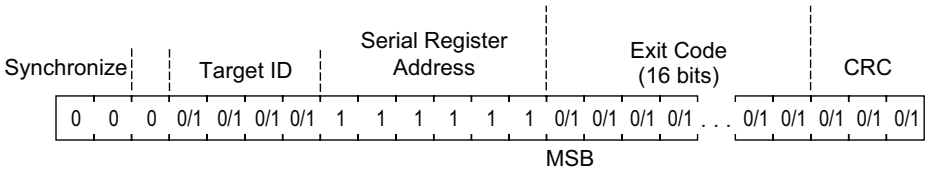
Function	Returns the A33003 to typical operation.
Syntax	Sent by the external controller on the A33003 output pin. Manchester exit code = Any value other than 0x62d2
Related Commands	Manchester access codes
Pulse Sequence	
Options	None
Examples	Similiar to the Manchester access code, the Manchester exit code acts as a broadcast pulse. To exit the serial communication mode, the exit code can be any value besides the access code (such as 0x0000).

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Table 13: Manchester Read

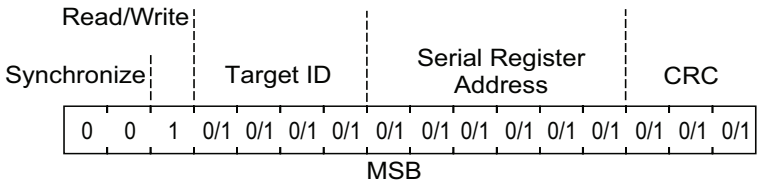
Function	Determines the serial address within the A33003, from which the next read response transmits data. The A33003 must first receive a Manchester access code before responding to a read command.
Syntax	Sent by the external controller on the A33003 output pin.
Related Commands	Read response
Pulse Sequence	
Options	None
Examples	

Table 14: Manchester Read Response

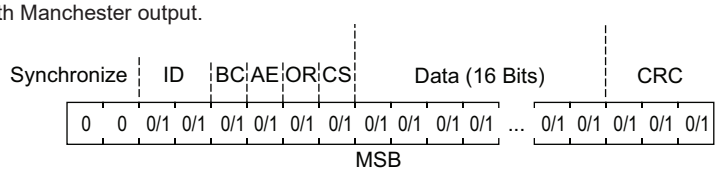
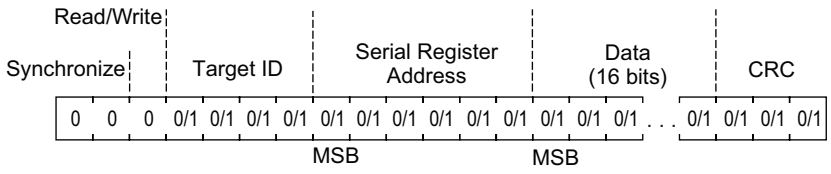
Function	Transmits to the external controller data retrieved from the A33003 serial register in response to the most recent read command.
Syntax	Sent by the A33003 on the output pin. Sent after a read command.
Related Commands	Read
Pulse Sequence	Read response with Manchester output. 
Options	Read from an even address, returns even byte [15:8] and odd byte [7:0]. Read from an odd address, returns odd byte [7:0] only. Data bits [15:8] are zeroes.
Examples	–

Table 15: Manchester Write

Function	Transmits to the A33003 data prepared by the external controller.
Syntax	Sent by the external controller on the A33003 output pin.
Related Commands	
Pulse Sequence	
Options	If the address is even, the 16 bits of the data field are written to the addressed byte and the addressed byte + 1. If the address is odd, only 8 bits are written (LSB of 16-bit data field).
Examples	

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EEPROM AND SHADOW MEMORY USE

The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and return 0 when read. Shadow registers do not contain the ECC bits. All EEPROM and shadow locations may be read without unlocking. The mapping of bits from register addresses in EEPROM to their corresponding register addresses in shadow is shown in the EEPROM table (See EEPROM Table section).

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM, shadow registers, and registers for additional status and diagnostics. All extended registers are up to 32 bits wide.

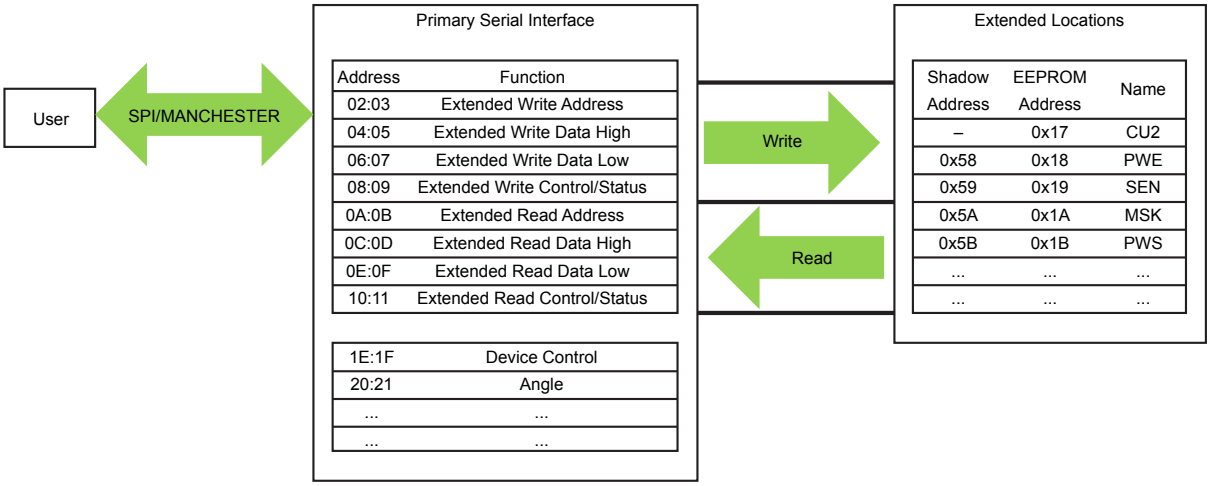

Figure 33: Serial Interface to Extended Memory (EEPROM and Shadow)

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Enabling EEPROM Access

To enable EEPROM write access after a power-on reset, an unlock code needs to be written to the KEYCODE serial register. This involves five write commands, executed as follows:

1. Write 0x00 to register 0x3C[15:8]
2. Write 0x27 to register 0x3C[15:8]
3. Write 0x81 to register 0x3C[15:8]
4. Write 0x1F to register 0x3C[15:8]
5. Write 0x77 to register 0x3C[15:8]

This needs to be performed once after power-on reset to enable writing to the EEPROM.

Writing to serial registers and reading from serial registers does not require special treatment after power-up.

Reading all EEPROM cells is always possible.

The device must be unlocked when performing EEPROM margin checking.

EEPROM Write Lock

It is possible to protect the EEPROM against accidental writes:

- Setting the LOCK field in the EEPROM to the value 0xC (1100 in binary) blocks any writes to the EEPROM, so that permanent changes are not possible anymore. Temporary changes to the setting are still possible by writing to the shadow memory, but these changes are lost after a power cycle.

This lock is permanent and cannot be reversed. Reading of the settings is still possible.

Setting the LOCK field in the EEPROM to the value 0x3 (0011 in binary) locks both EEPROM writes and shadow memory writes. This means none of the sensor settings can be changed anymore. This lock is permanent and cannot be reversed. Reading of the settings is still possible.

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Read Transaction from EEPROM (or Shadow Memory)

Invoking an extended read access is a three-step process:

1. Load the ERA register (using SPI or Manchester direct access) with the target extended address. ERA is the 8-bit extended address that determines which extended memory address is to be accessed.
2. Invoke the extended access by writing the direct ERCS register EXR bit with a 1. The ERA address is then read and the data are loaded into the ERD registers.
3. Read the ERD registers (using SPI or Manchester direct access) to get the extended data. Multiple packets are required to obtain all 32 bits.

EEPROM read accesses may take up to 2 µs to complete. The RDN bit in the ERCS register can be polled to determine if the read access is complete before reading the data. Shadow and AUX register reads complete in one system clock cycle after synchronization. Do not attempt to read the ERD registers if the read access is potentially in process, because it could change during the serial access and the data would be inconsistent. It is also possible that a SPI CRC error would be detected if the data were to change during the serial read via the SPI interface.

For example, to read location 0x1F in the EEPROM:

- Write 0x1F to the lower 8 bits of ERA (0x1F to ERA+1, address 0x0B)
- Write 0x80 to ERCS
- Read ERCS+1 until bit 0 (RDN) is set (or wait enough time)
- Read ERD (upper 16 bits of read data)
- Read ERD+2 (lower 16 bits of read data)

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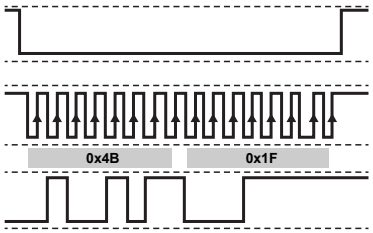
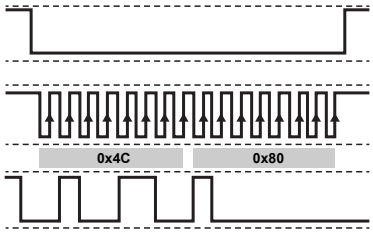
For example, to read location 0x1F in the EEPROM:

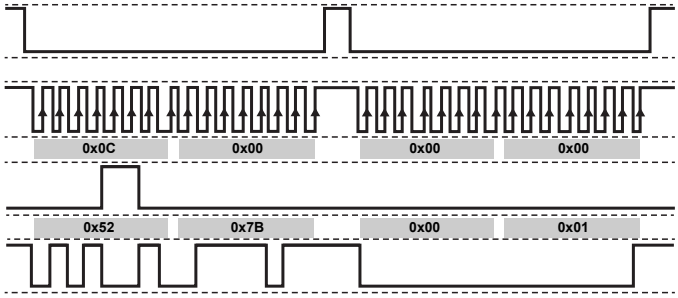
1. Write 0x1F to lower 8 bits of ERA (0x1F to “ERA+1”, address 0x0B).



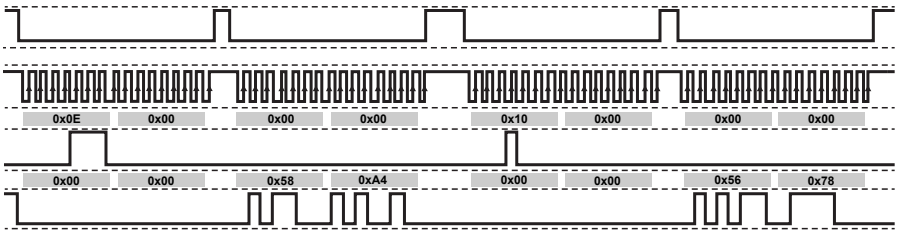
2. Write 0x80 to ERCS.



3. Read ERCS+1 until bit 0 (RDN) is set, or wait enough time.
   In the example, register 0x0C is read, so that the last bit of the second output byte contains the RDN bit.



4. Read ERDH (upper 16 bits of read data).
5. Read ERDL (lower 16 bits of read data).
   In the example below, the result for the data at address 0x1F is 0x58A45678. In this value:
   - Bits [31:26] are the EEPROM CRC.
   - Bits [25:24] are unused and zero.
   - Bits [23:0] are the EEPROM values that can be used. These are the 24 bits containing the data 0xA45678 that was written in the EEPROM write example.



NOTE: It is possible to pipeline transactions in this example, i.e., to send a new command while reading return data from the old command. If pipelined, the example transaction would be performed in eight SPI frames instead of the five shown.

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Write Transaction to EEPROM (or Shadow Memory)

Invoking an extended write access is a three-step process:

1. Load the EWA register (using SPI or Manchester direct access) with the target extended address.
2. Load the EWD registers (using SPI or Manchester direct access) with the data to be written to the target. Four SPI writes or two Manchester packets are needed to load all 32 bits of data.
3. Invoke the extended access by writing the direct EWCS register EXW bit with the value 1.

The EWA address is then written with the 32-bit EWD data.

The WDN bit in the EWCS register can be polled to determine when the write completes. This is only necessary for EEPROM writes, which can take up to 24 ms to complete. Shadow and AUX register writes complete immediately in one system clock cycle after synchronization.

For example, to write location 0x1F in the EEPROM with 0x00A45678:

1. Write 0x1F to the lower 8 bits of the EWA register (0x1F to EWA+1 address 0x03).
2. Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD+1, 0x56 to EWD+2, and 0x78 to EWD+3).
3. Write 0x80 to EWCS.
4. Read EWCS+1 until bit 0 (WDN) is set (or wait enough time).

If an access violation occurs (address not unlocked), the transaction terminates, the corresponding RDN or WDN bit becomes set, and the XEE warning bit asserts. The XEE bit in the ERR register also sets if the EEPROM write aborts.

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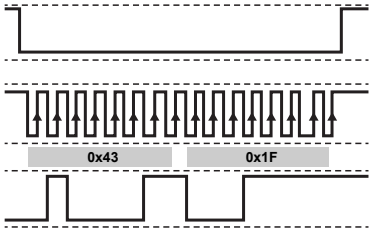
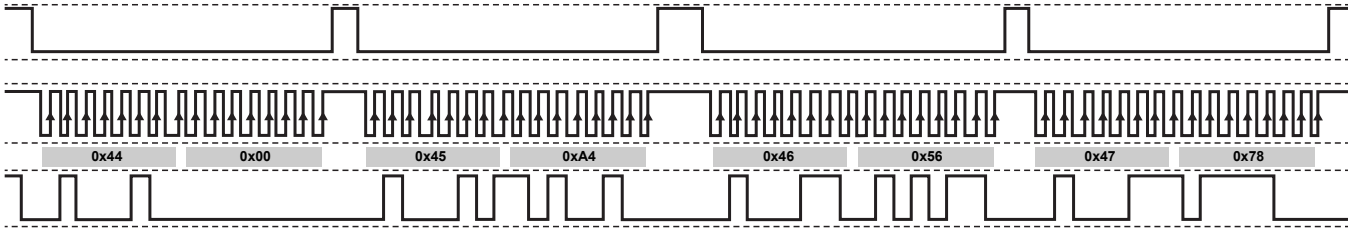
For example, to write location 0x1F in the EEPROM with 0x00A45678:

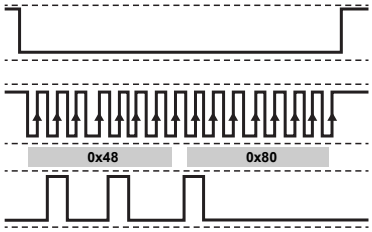
1. Write 0x1F to the lower 8 bits of the EWA register (0x1F to EWA+1, address 0x03).



2. Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD+1, 0x56 to EWD+2, and 0x78 to EWD+3).

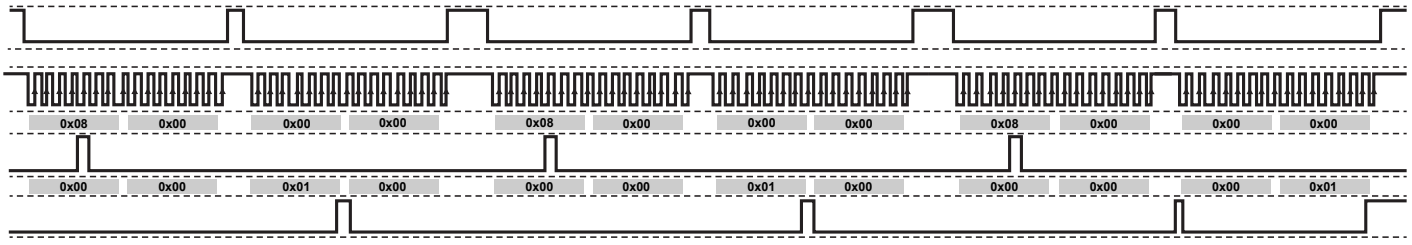


3. Write 0x80 to EWCS.



4. Read EWCS+1 until bit 0 (WDN) is set, or wait enough time.

   In the example, register 0x08 is read, so that the second output byte is from register 0x09, and a wait occurs for bit 0 to become 1, which happens in the last read.



If an access violation occurs (address not unlocked), the transaction terminates and the corresponding RDN or WDN bit becomes set, and the XEE warning bit asserts. The XEE bit in the ERR register also becomes set if the EEPROM write aborts.

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After writing to the EEPROM, verify that the write was successful by performing an EEPROM margin check.

EEPROM Margin Check

Due to nonidealities in transistors, current slowly leaks into or out of EEPROM cells and can, over time, cause small changes in the stored voltage level. Variances in voltage levels of the charge pump can result in a variety of stored EEPROM cell voltages when programming. If this value is marginally close to the threshold, the small drift over lifetime can cause this value to move across the threshold. This results in a corrupted EEPROM value. Because this drift happens slowly over time, if there is an issue, it may not become apparent for years. For this reason, it is important to perform margin testing (margining) to verify the internal voltage levels of EEPROM cells after programming, to ensure issues do not present in the future.

Margining is performed by Allegro on all registers at final test. Because EEPROM cell voltages are only modified when writing to the cell, margining is not required on registers that have not been modified.

Margining is performed in two steps: the first checks the validity of the voltage stored on digital “1” cells, and the second checks the voltage stored on digital “0” cells. It is important to perform both steps to ensure there are no issues.

To perform margining, write the value 0b0001 to the SPECIAL field of the CTRL register. This reduces the internal threshold value. Once this value is written, an EEPROM read uses this lower threshold when reading EEPROM values. Perform a read on all EEPROM registers that are being tested, and confirm they read correctly. If a stored voltage is marginal to the typical operating threshold, it appears as a one when it should be a zero.

To raise the threshold value above typical operation, repeat this test with the value 0b0010 in the SPECIAL register. Again, read all EEPROM registers being tested. In this test, any stored high voltage that is marginal to the typical threshold appears as a zero when it should be a one.

During either test, if a bit is read incorrectly, perform another EEPROM write of the desired values to the register, and retest the margins.

Unlike other values in the SPECIAL field, these values persist and can be read to confirm the write was successful. As a result, the SPECIAL register must be cleared (or power cycled) to return the threshold value to its typical level.

In the figure below, $V_{NOM(H)}$ represents the nominal voltage programmed into EEPROM cells containing a one, and $V_{NOM(L)}$ represents the nominal voltage programmed into EEPROM cells containing a zero. The red and blue lines represent the actual voltage levels in the programmed cells for “1” and “0” values, respectively. As can be observed, at time 0 when the margin test is run, both high and low levels still appear to be the correct value when the threshold is moved to the margin testing levels.

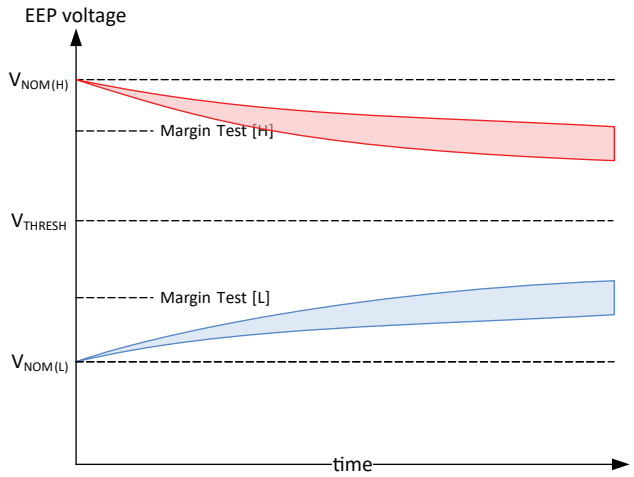

Figure 34: Example of Passing Programming Voltages

In the figure below, the high and low voltage levels at the time of programming are farther from their target. The drift over time results in these values crossing V_{THRESH} and becoming corrupted. At time 0 when the margin test is run, these values fail and are reported as errors to be reprogrammed.

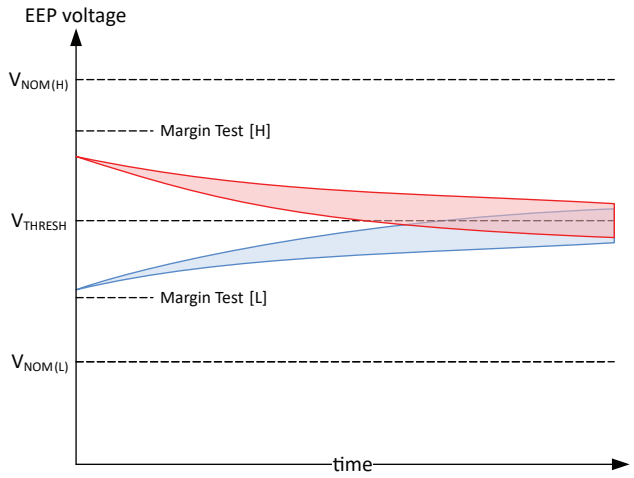

Figure 35: Example of Failing Programming Voltages

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Margining is shown below as a list of high-level steps. For details about performing individual steps, see the associated sections.

1. Clear the ERR and WARN registers.
   A. Set the CTRL.CLW and CTRL.CLE bits.
2. Enable EEPROM access.
3. Write new data to the EEPROM as desired.
4. Check the following flags for EEPROM errors: ESE, EUE, XEE,IER, CRC, and BSY.
   A. If any are asserted, the EEPROM write may have failed.
   B. A second write attempt is recommended.
5. Set CTRL.SPECIAL to 0001b to enable low-voltage margining.
6. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
7. Set CTRL.SPECIAL to 0010b to enable high-voltage margining.
8. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
9. If any EEPROM value read with a low or high threshold differs from the desired EEPROM or if either the ESE or EUE bits are set, EEPROM margining has failed.
   A. One additional write attempt and margin check should be accomplished. If margin failures persist following a second EEPROM write, the device should be discarded.

Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, the shadow extended addresses must be addressed, which are located at an offset of 0x40 above the EEPROM. For all addresses, refer to the EEPROM Table section.

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SERIAL INTERFACE TABLE

Table 16: Primary Serial Interface Registers Bits Map

Address [1] (0x00)	Register Symbol	Read/ Write	Addressed Byte (MSB)								Addressed Byte + 1 (LSB)								LSB Address
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x00	NOP	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x01
0x02	EWA	RW	0	0	0	0	0	0	0	0	WRITE_ADR								0x03
0x04	EWDH	RW	WRITE_DATA_HI																0x05
0x06	EWDL	RW	WRITE_DATA_LO																0x07
0x08	EWCS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN	0x09
0x0A	ERA	RW	0	0	0	0	0	0	0	0	READ_ADR								0x0B
0x0C	ERCS	WO/RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN	0x0D
0x0E	ERDH	RO	READ_DATA_HI																0x0F
0x10	ERDL	RO	READ_DATA_LO																0x11
0x12 0x14 0x16 0x18 0x1A 0x1C	UNUSED	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x13 0x15 0x17 0x19 0x1B 0x1D
0x1E	CTRL	RW/WO	SPECIAL				SPO	CLS	CLW	CLE	INITIATE_SPECIAL								0x1F
0x20	ANG	RO	0	EF	UV	P	ANGLE												0x21
0x22	STA	RO	1	0	0	0	EPTR	0	DIEID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK	0x23
0x24	ERR	RO	1	0	1	0	WAR	STF	AVG	0	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST	0x25
0x26	WARN	RO	1	0	1	1	IER	CRC	SEN	0	XEE	TR	ESE	SAT	TCW	BSY	MSH	TOV	0x27
0x28	TSEN	RO	1	1	1	1	TEMPERATURE												0x29
0x2A	SFIELD	RO	1	1	1	0	GAUSS												0x2B
0x2C	TURNS	RO	1	1	TSRC	P	TURNS												0x2D
0x2E	TOFF	RO	1	LAT	0	P	0	TURNS_OFFSET											0x2F
0x30	HANG	RO	0	EF	UV	P	ANGLE_HYS												0x31
0x32	ANG15	RO	0	ANGLE_15															0x33
0x34	ZANG	RO	0	EF	UV	P	ANGLE_ZCD												0x35
0x36	TD_HIGH	RO	0	EF	TSRC	P	TURNS_DELTA[23:12]												0x37
0x38	TD_LOW	RO	0	EF	LAT	P	TURNS_DELTA[11:0]												0x39
0x3A	PTANG	RO	0	EF	UV	P	PLL_TURNS_ANGLE												0x3B
0x3C	IKEY	WO/RO	KEYCODE								0	0	0	0	0	0	0	CUL	0x3D
0x3E	UNUSED	RO	UNUSED																0x3F

[1] Addresses that span multiple bytes are addressed by the most significant byte.

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PRIMARY SERIAL INTERFACE REGISTERS REFERENCE

Location 0x02:0x03 (EWA)

EWA.WRITE_ADR

The field WRITE_ADR is a bit field located at address 0x02[7:0]. This bit field is part of the location EWA.

8-bit address for extended writes. Writes require unlock.

0x00:0x1F—EEPROM (takes approximately 24 ms)
0x40:0x5F—Shadow memory

Location 0x04:0x05 (EWDH)

EWDH.WRITE_DATA_HI

The field WRITE_DATA_HI is a bit field located at address 0x04[15:0]. This bit field is part of the location EWDH.

Upper 16 bits of data for an extended write operation.

Location 0x06:0x07 (EWDL)

EWDL.WRITE_DATA_LO

The field WRITE_DATA_LO is a bit field located at address 0x06[15:0]. This bit field is part of the location EWDL.

Lower 16 bits of data for an extended write operation.

Location 0x08:0x09 (EWCS)

EWCS.WDN

The field WDN is a bit located at address 0x08[0]. This bit is part of the location EWCS.

Write is complete when wdn = 1; WDN clears when EXW is set to 1.

EWCS.WIP

The field WIP is a bit located at address 0x08[8]. This bit is part of the location EWCS.

Write in progress when 1.

EWCS.EXW

The field EXW is a bit located at address 0x08[15]. This bit is part of the location EWCS.

Initiate extended write by writing with 1. Sets WIP and clears WDN. Write-only, always reads back 0.

Location 0x0A:0x0B (ERA)

ERA.READ_ADR

The field READ_ADR is a bit field located at address 0x0A[7:0]. This bit field is part of the location ERA.

8-bit address for extended reads.

0x00:0x1F—EEPROM (takes approximately 2 µs)
0x40:0x5F—Shadow memory

NOTE: After LBIST or a reload of EEPROM values, the value of READ_ADR changes.

Location 0x0C:0x0D (ERCS)

ERCS.RDN

The field RDN is a bit located at address 0x0C[0]. This bit is part of the location ERCS.

Read is complete when value is 1, clears when EXR is set to 1.

ERCS.RIP

The field RIP is a bit located at address 0x0C[8]. This bit is part of the location ERCS.

Read in progress when value is 1.

ERCS.EXR

The field EXR is a bit located at address 0x0C[15]. This bit is part of the location ERCS.

Initiate extended read by writing with the value 1. Sets RIP and clears RDN. Write-only, always reads back the value 0.

Location 0x0E:0x0F (ERDH)

ERDH.READ_DATA_HI

The field READ_DATA_HI is a bit field located at address 0x0E[15:0]. This bit field is part of the location ERDH.

Upper 16 bits of data from extended read operation, valid when RDN is set to 1.

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Location 0x10:0x11 (ERDL)

ERDL.READ_DATA_LO

The field READ_DATA_LO is a bit field located at address 0x10[15:0]. This bit field is part of the location ERDL.

Lower 16 bits of data from extended read operation, valid when RDN is set to 1.

Location 0x1E:0x1F (CTRL)

CTRL.INITIATE_SPECIAL

The field INITIATE_SPECIAL is a bit field located at address 0x1E[7:0]. This bit field is part of the location CTRL.

For certain actions from the SPECIAL bit field, a code must be sent to INITIATE_SPECIAL. The following actions may be triggered by writing this field (the code must be written after the CTRL.SPECIAL field is written):

0x46 Initiates turns counter reset.
0x5A Initiates hard reset.
0xA5 Initiates EEPROM reload.
0xB9 Initiates CVH self-test or functional BIST.

Read always returns 0x00.

CTRL.SPO

The SPO bit is bit 11 of the CTRL row. It is the SPI override bit.

If set to 1, MISO is forced to be SPI output. This overrides PWM and SENT.

CTRL.CLE

The field CLE is a bit located at address 0x1E[8]. This bit is part of the location CTRL.

Clears error register ERR when written with the value 1. Clears bits that were previously read from ERR. Bits that have not been read are not cleared, so ERR should be read first. Write-only, always returns 0.

CTRL.CLW

The field CLW is a bit located at address 0x1E[9]. This bit is part of the location CTRL.

Clears warning (WARN) register when set to 1. Bits that have not been read are not cleared, so WARN should be read first. Write-only, always returns 0.

CTRL.CLS

The field CLS is a bit located at address 0x1E[10]. This bit is part of the location CTRL.

Clears bits SDN and BDN from STATUS register when set to 1. Write-only, returns 0 when read.

CTRL.SPECIAL

The field SPECIAL is a bit field located at address 0x1E[15:12]. This bit field is part of the location CTRL.

Special actions. Some of the actions are only invoked after the INITIATE_SPECIAL field is written with the correct value. This field returns 0x00 on completion.

0000	No action.
0001	Enable EEPROM low-voltage margin. IC must be unlocked.
0010	Enable EEPROM high-voltage margin. IC must be unlocked.
0011	Turns counter load from EWD. Starts after writing 0x46 to INITIATE_SPECIAL.
0100	Turns counter reset. Starts after writing 0x46 to INITIATE_SPECIAL.
0101	Reload EEPROM. Requires unlock of part. Starts after writing 0xA5 to INITIATE_SPECIAL.
0111	Hard reset. Requires unlock of part. Starts after writing 0x5A to INITIATE_SPECIAL.
1001	Run CVH self-test. Starts after writing 0xB9 to INITIATE_SPECIAL.
1010	Run logic BIST (on PLL logic). Starts after writing 0xB9 to INITIATE_SPECIAL.
1011	Run both the CVH self-test and Logic BIST in parallel. Starts after writing 0xB9 to the CTRL.INITIATE_SPECIAL field.
1101	Resample PWM errors (errors must have cleared for this to have an effect).
1110	Clear fatal PWM errors (EUE, WDE, STE).
1111	Clear fatal and resample all PWM errors.

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Location 0x20:0x21 (ANG)

ANG.ANGLE

The field ANGLE is a bit field located at address 0x20[11:0]. This bit field is part of the location ANG.

Angle from PLL after processing. Angle in degrees = unsigned 12-bit value × (360/4096).

ANG.P

The field P is a bit located at address 0x20[12]. This bit is part of the location ANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

ANG.UV

The field UV is a bit located at address 0x20[13]. This bit is part of the location ANG.

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are real time, but are masked by the shadow mask bits.

ANG.EF

The field EF is a bit located at address 0x20[14]. This bit is part of the location ANG.

Error flag. If 1, at least one unmasked bit is set in ERR or WARN.

Location 0x22:0x23 (STA)

STA.AOK

The field AOK is a bit located at address 0x22[0]. This bit is part of the location STA.

Angle output OK. PLL is in lock.

STA.BIP

The field BIP is a bit located at address 0x22[1]. This bit is part of the location STA.

Boot in progress.

STA.CSTR

The field CSTR is a bit located at address 0x22[2]. This bit is part of the location STA.

CVH self-test running.

STA.LBR

The field LBR is a bit located at address 0x22[3]. This bit is part of the location STA.

LBIST running.

STA.BDN

The field BDN is a bit located at address 0x22[4]. This bit is part of the location STA.

Boot complete. EEPROM loaded and any startup self-tests are complete.

STA.SDN

The field SDN is a bit located at address 0x22[5]. This bit is part of the location STA.

Special access (from ctrl register) done. Clears to 0 when SPECIAL triggered, set to 1 when complete.

STA.ROT

The field ROT is a bit located at address 0x22[7]. This bit is part of the location STA.

Rotation direction based on hysteresis (0 = increasing angles, 1 = decreasing angles).

STA.DIEID

The field DIEID is a bit field located at address 0x22[9:8]. This bit field is part of the location STA.

Die ID from EEPROM. Programmed by Allegro at factory.

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Location 0x24:0x25 (ERR)

This is the error register. All errors are latched, meaning they remain high after they have occurred just once. Errors need to be read, then cleared to remove them. It is important to clear errors during operation, so that subsequent errors become visible. This is especially important for the RST error flag (reset), which is always enabled after power-up. Failure to remove an error flag prevents discovery of any later unexpected reset.

ERR.RST

The field RST is a bit located at address 0x24[0]. This bit is part of the location ERR.

Reset condition. Sets on power-on reset or on hard reset. Does not set on LBIST.

ERR.MSL

The field MSL is a bit located at address 0x24[1]. This bit is part of the location ERR.

Magnetic sense low fault. Magnetic sense was below the low limit (MagSenseLow).

ERR.UVA

The field UVA is a bit located at address 0x24[2]. This bit is part of the location ERR.

Undervoltage detector tripped. Becomes set again after clearing if the undervoltage situation persists. Based on analog regulator.

ERR.UVD

The field UVD is a bit located at address 0x24[3]. This bit is part of the location ERR.

Undervoltage detector tripped. Becomes set again after clearing if the undervoltage situation persists. Based on digital regulator.

ERR.WDE

The field WDE is a bit located at address 0x24[4]. This bit is part of the location ERR.

Oscillator watchdog tripped.

ERR.EUE

The field EUE is a bit located at address 0x24[5]. This bit is part of the location ERR.

EEPROM uncorrectable error. A multi-bit EEPROM read occurred.

ERR.ZIE

The field ZIE is a bit located at address 0x24[6]. This bit is part of the location ERR.

Zero-crossing integrity error. A zero-crossing did not occur within the maximum time expected, likely indicating a missing magnet or extreme rotation speed.

ERR.PLK

The field PLK is a bit located at address 0x24[7]. This bit is part of the location ERR.

PLL lost lock.

ERR.AVG

The field AVG is a bit located at address 0x24[9]. This bit is part of the location ERR.

Angle averaging error. The ORATE is too high for the velocity and the averaging is corrupted.

ERR.STF

The field STF is a bit located at address 0x24[10]. This bit is part of the location ERR.

Self-test failure.

ERR.WAR

The field WAR is a bit located at address 0x24[11]. This bit is part of the location ERR.

Warning. Some unmasked error bits are set in the WARN register. If WAR in mask register MSK is set, ERR.WAR is forced to 0.

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Location 0x26:0x27 (WARN)

WARN.TOV

The field TOV is a bit located at address 0x26[0]. This bit is part of the location WARN.

Turns counter overflow error. The turns counter surpassed its maximum value of ±256 full rotation. This is not dependent on the resolution of TURNS (45 or 180 degrees).

WARN.MSH

The field MSH is a bit located at address 0x26[1]. This bit is part of the location WARN.

Magnetic sense high fault. Magnetic sense has exceeded the high limit (MagSenseHigh).

WARN.BSY

The field BSY is a bit located at address 0x26[2]. This bit is part of the location WARN.

Extended access overflow. An EXW or EXR was initiated while previous extended read or write was in progress.

WARN.TCW

The field TCW is a bit located at address 0x26[3]. This bit is part of the location WARN.

Turns counter warning (over ±135 degrees delta).

WARN.SAT

The field SAT is a bit located at address 0x26[4]. This bit is part of the location WARN.

Aggregate saturation flag. Shows that any internal signals have saturated, likely to have been cause by extremely strong or weak fields.

WARN.ESE

The field ESE is a bit located at address 0x26[5]. This bit is part of the location WARN.

EEPROM soft error. A correctable (single-bit) EEPROM read occurred.

WARN.TR

The field TR is a bit located at address 0x26[6]. This bit is part of the location WARN.

Temperature out of range. The temperature sensor calculated a temperature below –60°C or above 180°C. Temperature saturates at those limits.

WARN.XEE

The field XEE is a bit located at address 0x26[7]. This bit is part of the location WARN.

Extended execute error. A command intiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

WARN.SEN

The field SEN is a bit located at address 0x26[9]. This bit is part of the location WARN.

SENT contention error.

WARN.CRC

The field CRC is a bit located at address 0x26[10]. This bit is part of the location WARN.

Incoming SPI CRC error. Packet was discarded.

WARN.IER

The field IER is a bit located at address 0x26[11]. This bit is part of the location WARN.

Interface error. Invalid number of bits in SPI packet, or bit 15 of MOSI data = 1. Packet was discarded.

Also Manchester error or SENT contention.

Location 0x28:0x29 (TSEN)

TSEN.TEMPERATURE

The field TEMPERATURE is a bit field located at address 0x28[11:0]. This bit field is part of the location TSEN.

Current junction temperature from internal temperature sensor relative to room temperature (signed value). Value is in 1/8 of a degree. Temperature °C ≈ (TSEN.TEMPERATURE / 8) + 25.

Location 0x2A:0x2B (FIELD)

FIELD.GAUSS

The field GAUSS is a bit field located at address 0x2A[11:0]. This bit field is part of the location FIELD.

Field strength in gauss. Field level is used for gross correction, and should not be used for accurate field readings. Value is typically ~10% low.

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Location 0x2C:0x2D (TRNS)

TRNS.TURNS

The field TURNS is a bit field located at address 0x2C[11:0]. This bit field is part of the location TRNS.

Turns counter. Signed 45- or 180-degree increments.

Reading this field automatically latches the TOFF.TURNS_OFFSET value and sets TOFF.LAT. Allows all 21 bits of the TURNS_DELTA field to be read with the same timestamp.

TRNS.P

The field P is a bit located at address 0x2C[12]. This bit is part of the location TRNS.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

TRNS.TSRE

The field TSRE is a bit located at address 0x2C[13]. This bit is part of the location TRNS.

Turns source. Set to 1 to use the more accurate PLL as the turns counter source (recommended). Set to 0 to use ZCD angle as turns counter (not recommended).

Location 0x2E:0x2F (TOFF)

TOFF.TURNS_OFFSET

The field TURNS_OFFSET is a bit field located at address 0x2E[10:0]. This bit field is part of the location TOFF.

This is either the 11 or 9 LSBs of the TURNS_DELTA register, depending on a 180- or 45-degree turns configuration. This field is latched whenever the turns address is read.

TOFF.P

The field P is a bit located at address 0x2E[12]. This bit is part of the location TOFF.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

TOFF.LAT

The field LAT is a bit located at address 0x2E[14]. This bit is part of the location TOFF.

Indicates that the TURNS_OFFSET field is latched. If 1, indicates that the word TOFF was latched on a prior read of the TURNS register and is consistent with that reading. Returns to 0 after reading.

Location 0x30:0x31 (HANG)

HANG.ANGLE_HYS

The field ANGLE_HYS is a bit field located at address 0x30[11:0]. This bit field is part of the location HANG.

Angle from PLL after processing and application of hysteresis. Angle in degrees = unsigned 12-bit value × (360 / 4096).

HANG.P

The field P is a bit located at address 0x30[12]. This bit is part of the location HANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

HANG.UV

The field UV is a bit located at address 0x30[13]. This bit is part of the location HANG.

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are real time, but are masked by the shadow mask bits.

HANG.EF

The field EF is a bit located at address 0x30[14]. This bit is part of the location HANG.

Error flag. Becomes 1 if any unmasked bit in ERR or WARN is set.

Location 0x32:0x33 (ANG15)

ANG15.ANGLE_15

The field ANGLE_15 is a bit field located at address 0x32[14:0]. This bit field is part of the location ANG15.

15-bit compensated angle (not rounded).

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Location 0x34:0x35 (ZANG)

ZANG.ANGLE_ZCD

The field ANGLE_ZCD is a bit field located at address 0x34[11:0]. This bit field is part of the location ZANG.

Angle from ZCD.
Angle in degrees = unsigned 12-bit value × (360 / 4096).

ZANG.P

The field P is a bit located at address 0x34[12]. This bit is part of the location ZANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

ZANG.UV

The field UV is a bit located at address 0x34[13]. This bit is part of the location ZANG.

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are real time, but are masked by the shadow mask bits.

ZANG.EF

The field EF is a bit located at address 0x34[14]. This bit is part of the location ZANG.

Error flag. Becomes 1 if any unmasked bit in ERR or WARN is set.

Location 0x36:0x37 (TD_HIGH)

TD_HIGH.TURNS_DELTA_HIGH

The field TURNS_DELTA_HIGH is a bit field located at address 0x36[11:0]. This bit field is part of the location TD_HIGH.

Upper 9 bits (sign extended to 12) of the turns delta counter.

When read, the contents of TD_LOW (address 0x38:0x39) are latched and the TD_LOW.LAT bit is set. This allows all 25 bits (sign extended) of the TURNS_DELTA value to be read at the same timestamp.

TD_HIGH.P

The field P is a bit located at address 0x36[12]. This bit is part of the location TD_HIGH.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

TD_HIGH.TSRC

The field TSRC is a bit located at address 0x36[14]. This bit is a part of the location TD_HIGH.

Turns source. When 1, indicates the PLL is the turns counter source. When 0, the ZCD signal path (uncompensated) is the source.

TD_HIGH.EF

The field EF is a bit located at address 0x36[14]. This bit is part of the location TD_HIGH.

Error flag. Becomes 1 if any unmasked bit in ERR or WARN is set.

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Location 0x38:0x39 (TD_LOW)

TD_LOW.TURNS_DELTA_LOW

The field TURNS_DELTA_LOW is a bit field located at address 0x38[11:0]. This bit field is part of the location TD_LOW.

Lower 12 bits of the turns delta. This is the angle offset at 12-bit resolution.

This value is latched when reading the td_high register, allowing the entirety of TURNS_DELTA to be read with the same timestamp.

TD_LOW.P

The field P is a bit located at address 0x38[12]. This bit is part of the location TD_LOW.

Odd parity computed across all bits in this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

TD_LOW.LAT

The filed LAT is a bit located at address 0x38[13]. This bit is part of the location TD_LOW.

Inidicates that the TD_LOW field is latched. If 1, indicates that TD_LOW was latched on a prior read of the TD_HIGH register and is consistent with that reading. Returns to 0 after reading.

TD_LOW.EF

The field EF is a bit located at address 0x38[14]. This bit is part of the location TD_LOW.

Error flag. Becomes 1 if any unmasked bit in ERR or WARN is set.

Location 0x3A:0x3B (PTANG)

PTANG.PLL_TURNS_ANGLE

The field PLL_TURNS_ANGLE is a bit field located at address 0x3A[11:0]. This bit field is part of the location PTANG.

Angle from PLL after processing, as used for the turns counter.

May have hysteresis based on H2A configuration in EEPROM.

Angle in degrees = unsigned 12-bit value × (360 / 4096).

PTANG.P

The field P is a bit located at address 0x3A[12]. This bit is part of the location PTANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

PTANG.UV

The field UV is a bit located at address 0x3A[13]. This bit is part of the location PTANG.

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are real time, but are masked by the shadow mask bits.

PTANG.EF

The field EF is a bit located at address 0x3A[14]. This bit is part of the location PTANG.

Error flag. Becomes 1 if any unmasked bit in ERR or WARN is set.

Location 0x3C:0x3D (KEY)

KEY.CUL

The field CUL is a bit located at address 0x3C[0]. This bit is part of the location KEY.

Customer unlocked if 1.

KEY.KEYCODE

The field KEYCODE is a bit field located at address 0x3C[15:8]. This bit field is part of the location KEY.

Customer access keycode is entered here; value is 0x27_81_1F_77.

Always reads back 0.

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EEPROM TABLE

The EEPROM register bitmap is shown below.

All EEPROM content can be read by the user. The EEPROM ECC field in bits [31:26] of each word are not shown here.

Table 17: EEPROM / Shadow Memory Map

EEPROM Address	Shadow Memory Address	Register Name	Bits																									
			25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x17	0x57	CU2	-X-	-X-	CUSTOMER 2																							
0x18	0x58	PWE	-X-	-X-	ZCD_TURNS_OFFSET											TOV	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	WDE
0x19	0x59	SEN	MAXID		SS	SENT_TICK							SM	SENT_MODE			DATA_MODE				CIS	SCN_MODE			NS	ZS	XA	FA
0x1A	0x5A	MSK	-X-	-X-	IERM	CRCM	SENM	-X-	XEEM	TRM	ESEM	SATM	TCWM	BSYM	MSHM	TOVM	WARM	STFM	AVGM	-X-	PLKM	ZIEM	EUEM	WDEM	UVCCM	UVAM	MSLM	RSTM
0x1B	0x5B	PWS	FP_ADJ		PEN	PWM_BAND			PWM_FREQ				MEPE	PHE	PEO	PES	ELI	LS	ZAL	IS	PO	SPDRV			DM	H2T	S17	SC
0x1C	0x5C	ANG	-X-	-X-	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
0x1D	0x5D	LPC	-X-	-X-	T45	TCP	-X-	-X-	TURNS_INIT	-X-							-X-	-X-										
0x1E	0x5E	COM	-X-	-X-	LOCK				LBE	CSE	DUR	DEL	-X-	CUD	DST	DHR	MAG_THRES_HI				MAG_THRES_LO							
0x1F	0x5F	CUS	-X-	-X-	CUSTOMER																							
0x20	0x60	LIN	-X-	-X-	LINEARIZATION ERROR SEGMENT 1												LINEARIZATION ERROR SEGMENT 0											
0x21	0x61	LIN	-X-	-X-	LINEARIZATION ERROR SEGMENT 3												LINEARIZATION ERROR SEGMENT 2											
…	…	…	-X-	-X-	…												---											
0x2E	0x6E	LIN	-X-	-X-	LINEARIZATION ERROR SEGMENT 29												LINEARIZATION ERROR SEGMENT 28											
0x2F	0x6F	LIN	-X-	-X-	LINEARIZATION ERROR SEGMENT 31												LINEARIZATION ERROR SEGMENT 30											

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EEPROM REFERENCE

Location 0x17 (CU2)

Customer-usable field, intended for storing data or turns counter.

This word can be written even if EEPROM is locked. Write may be allowed without the unlock code based on COM.DUR and COM.DEL settings (see word 0x1E).

CU2.CUSTOMER 2

The field CUSTOMER 2 is a bit field located at address 0x17 [23:0]. This bit field is part of the location CU2.

Location 0x18 (PWE)

PWE.WDE

The field WDE is a bit located at address 0x18[0]. This bit is part of the location PWE.

PWM watchdog error enable. Duty cycle output 5% at half the selected PWM frequency.

PWE.EUE

The field EUE is a bit located at address 0x18[1]. This bit is part of the location PWE.

PWM EEPROM uncorrectable error enable. Duty cycle 10.625% at half the selected PWM frequency.

PWE.STF

The field STF is a bit located at address 0x18[2]. This bit is part of the location PWE.

PWM self-test failure error enable. Duty cycle 16.25% at half the selected PWM frequency.

PWE.PLK

The field PLK is a bit located at address 0x18[3]. This bit is part of the location PWE.

PWM PLL lost lock error enable. Duty cycle 21.875% at half the selected PWM frequency.

PWE.ZIE

The field ZIE is a bit located at address 0x18[4]. This bit is part of the location PWE.

PWM zero-crossing integrity error enable. Duty cycle 27.5% at half the selected PWM frequency.

PWE.AVG

The field AVG is a bit located at address 0x18[5]. This bit is part of the location PWE.

PWM angle averaging error enable. Duty cycle is 33.125% at half the selected PWM frequency.

PWE.UV

The field UV is a bit located at address 0x18[6]. This bit is part of the location PWE.

PWM undervoltage fault enable (analog or digital). Duty cycle 38.75% at half the selected PWM frequency.

PWE.MSL

The field MSL is a bit located at address 0x18[7]. This bit is part of the location PWE.

PWM magnetic sense low fault enable. Duty cycle 44.375% at half the selected PWM frequency.

PWE.ESE

The field ESE is a bit located at address 0x18[8]. This bit is part of the location PWE.

PWM EEPROM soft error enable. Duty cycle 50% at half the selected PWM frequency.

PWE.SAT

The field SAT is a bit located at address 0x18[9]. This bit is part of the location PWE.

PWM saturation warning enable. Duty cycle 55.625% at half the selected PWM frequency.

PWE.MSH

The field MSH is a bit located at address 0x18[10]. This bit is part of the location PWE.

PWM magnetic sense high fault enable. Duty cycle 61.25% at half the selected PWM frequency.

PWE.TR

The field TR is a bit located at address 0x18[11]. This bit is part of the location PWE.

PWM temperature sensor out of range error enable. Duty cycle 66.875% at half the selected PWM frequency.

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PWE.TOV

The field TOV is a bit located at address 0x18[12]. This bit is part of the location PWE.

PWM turns counter overflow error enable. Duty cycle 72.5% at half the selected PWM frequency.

PWE.ZCD_TURNS_OFFSET

The field ZCD_TURNS_OFFSET is a bit field located at address 0x18[23:13]. This bit field is part of the location PWE.

Offset to ZCD angle for purposes of aligning for turns counting. This is 11-bit angle resolution and is added to the ZCD angle for turns purposes. If turns is configured to use the PLL (TCP = 1), it is important to use this to align the ZCD close to the PLL angle.

Location 0x19 (SEN)

For further details, see Appendix A: SENT Output Description.

SEN.FA

The field FA is a bit located at address 0x19 [0]. This bit field is part of the location SEN.

F_SAMPLE is an addressing pulse. If 0, it is a broadcast pulse.

SEN.XA

The field XA is a bit field located at address 0x19 [1]. This bit field is part of the location SEN.

Allows the F_AUX pulse to be treated as an addressing pulse. If 0, F_AUX is a broadcast pulse.

SEN.ZS

The field ZS is a bit located at address 0x19 [2]. This bit field is part of the location SEN.

Sample-and-hold is to be performed in slot 0.

SEN.NS

The field NS is a bit located at address 0x19 [3]. This bit field is part of the location SEN.

No sample. If 1, the F_SAMPLE pulse does not perform a sample-and-hold.

SEN.SCN_MODE

The field SCN_MODE is a bit field located at address 0x19 [6:4]. This bit field is part of the location SEN.

SCN contents by mode:

0 {0, 0, SOFT_FLAG, HARD_FLAG}
1 {SERIAL MSG SYNC, SERIAL MSG DATA, SOFT_FLAG, HARD_FLAG}
2 {ID[1], ID[0], SOFT_FLAG, HARD_FLAG}
3 {0, 0, 0, SOFT_FLAG | HARD_FLAG}
4 {0, 0, ID[1], ID[0]}
5 {SERIAL MSG SYNC, SERIAL MSG DATA, ID[1], ID[0]}
6 {SOFT_FLAG, HARD_FLAG, ID[1], ID[0]}
7 {SERIAL MSG SYNC, SERIAL MSG DATA, 0, SOFT_FLAG | HARD_FLAG}

SEN.CIS

The field CIS is a bit located at address 0x19 [7]. This bit field is part of the location SEN.

If 1, CRC includes the status and communication nibble.

SEN.DATA_MODE

The field DATA_MODE is a bit field located at address 0x19 [11:8]. This bit field is part of the location SEN.

SENT data nibble content mode:

0 Angle only (3 nibbles)
1 Angle (3) + rotating status (2)
2 Angle (3) + rotating data (3)
3 Unused
4 Angle (3) + rotating status (2) + alive (1)
5 Angle (3) + alive (2) + ~first nibble (1) (secure sensor format)
6 Angle16 (4)
7 Angle16 (4) + rotating status (1) + alive (1)
8 Angle only (3 nibbles) + ID (1)
9 Angle (3) + rotating status (2) + ID (1)
10 Angle (3) + rotating data (2) + ID (1)
11 Unused
12 Angle (3) + rotating status (1) + alive (1) + ID (1)
13 Angle (3) + alive(1) + ~first nibble (1) + ID (1)
14 Angle16 (4) + ID (1)
15 Angle16 (4) + alive (1) + ID (1)

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SEN.SENT_MODE

The field SENT_MODE is a bit field located at address 0x19 [14:12]. This bit field is part of the location SEN.

0	Disabled
1	Streaming (no pause pulses)
2	Streaming but aligned to angle update (pause pulses)
3	TSENT, data sampled just before data nibbles
4	TSENT, data sampled at falling edge of trigger (after minimum width)
5	ASENT
6	SSENT
7	Long SSENT

NOTE: If PEN = 1, then PWM has precedence, and SENT becomes disabled.

NOTE: If both PWM and SENT are disabled, Manchester is active (unless it is disabled or CTRL.SPO is 1).

SEN.SM

The field SM is a bit located at address 0x19 [15]. This bit field is part of the location SEN.

Slot marking. SSENT only. If 1, SSENT outputs a bus high delay after an addressing pulse based on slot ID.

SEN.SENT_TICK

The field SENT_TICK is a bit field located at address 0x19 [22:16]. This bit field is part of the location SEN.

SENT tick time, N × period of 16 MHz clock (forced to minimum of 2 clocks internally).

SEN.SS

The field SS is a bit located at address 0x19 [23]. This bit field is part of the location SEN.

Slot sync. SSENT only. If 1, then SSENT synchronizes to the bus after a reset based on the slot marking of the other sensor. Only valid if SM = 1.

SEN.MAXID

The field MAXID is a bit field located at address 0x19 [25:24]. This bit field is part of the location SEN.

Max sensor ID on bus, for SSENT. Defines highest sensor ID on bus, after which the slot counting wraps back to 0.

Location 0x1A (“MSK”)

MSK.RSTM

The field RSTM is a bit located at address 0x1A[0]. This bit is part of the location MSK.

Reset mask. Set to 1 to hide the error bit.

MSK.MSLM

The field MSLM is a bit located at address 0x1A[1]. This bit is part of the location MSK.

Magnetic sense low fault mask. Set to 1 to hide the error bit.

MSK.UVAM

The field UVAM is a bit located at address 0x1A[2]. This bit is part of the location MSK.

Analog undervoltage fault mask. Set to 1 to hide the error bit.

MSK.UVDM

The field UVDM is a bit located at address 0x1A[3]. This bit is part of the location MSK.

Digital undervoltage fault mask. Set to 1 to hide the error bit.

MSK.WDEM

The field WDEM is a bit located at address 0x1A[4]. This bit is part of the location MSK.

Watchdog error mask. Set to 1 to hide the error bit.

MSK.EUEM

The field EUEM is a bit located at address 0x1A[5]. This bit is part of the location MSK.

EEPROM uncorrectable error mask. Set to 1 to hide the error bit.

MSK.ZIEM

The field ZIEM is a bit located at address 0x1A[6]. This bit is part of the location MSK.

Zero-crossing integrity error mask. Set to 1 to hide the error bit.

MSK.PLKM

The field PLKM is a bit located at address 0x1A[7]. This bit is part of the location MSK.

PLL lost lock error mask. Set to 1 to hide the error bit.

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MSK.AVGM

The field AVGM is a bit located at address 0x1A[9]. This bit is part of the location MSK.

Angle averaging fault mask. Set to 1 to hide the error bit.

MSK.STFM

The field STFM is a bit located at address 0x1A[10]. This bit is part of the location MSK.

Self-test failure error mask. Set to 1 to hide the error bit.

MSK.WARM

The field WARM is a bit located at address 0x1A[11]. This bit is part of the location MSK.

If set to 1, the WAR bit in the ERR register does not become set when unmasked warnings are present.

MSK.TOVM

The field TOVM is a bit located at address 0x1A[12]. This is part of the location MSK.

Turns counter overflow error mask. Set to 1 to hide the error bit.

MSK.MSHM

The field MSHM is a bit located at address 0x1A[13]. This bit is part of the location MSK.

Magnetic sense high fault mask. Set to 1 to hide the error bit.

MSK.BSYM

The field BSYM is a bit located at address 0x1A[14]. This bit is part of the location MSK.

Indirect access busy error mask. Set to 1 to hide the error bit.

MSK.TCWM

The field TCWM is a bit located at address 0x1A[15]. This bit is part of the location MSK.

Turns counter warning mask. Set to 1 to hide the error bit.

MSK.SATM

The field SATM is a bit located at address 0x1A[16]. This bit is part of the location MSK.

Aggregate saturation flag mask. Set to 1 to hide the error bit.

MSK.ESEM

The field ESEM is a bit located at address 0x1A[17]. This bit is part of the location MSK.

EEPROM soft error mask. Set to 1 to hide the error bit.

MSK.TRM

The field TRM is a bit located at address 0x1A[18]. This bit is part of the location MSK.

Temperature sensor out of range error mask. Set to 1 to hide the error bit.

MSK.XEEM

The field XEEM is a bit located at address 0x1A[19]. This bit is part of the location MSK.

Execute error mask. Set to 1 to hide the error bit.

MSK.SEN

MSK.SEN is located at address 0x1A[21].

SENT error mask. Set to 1 to prevent a SENT contention error from asserting the EF flag within serial space and the soft error flag within the SCN of the SENT frame.

MSK.CRCM

The field CRCM is a bit located at address 0x1A[22]. This bit is part of the location MSK.

CRC error mask (SPI). Set to 1 to hide the error bit.

MSK.IERM

The field IERM is a bit located at address 0x1A[23]. This bit is part of the location MSK.

Interface error mask. Set to 1 to hide the error bit.

Location 0x1B (PWS)

PWS.SC

The field SC is a bit located at address 0x1B[0]. This bit is part of the location PWS.

SPI CRC (incoming) validated if SC = 1, ignored if SC = 0.

PWS.S17

The field S17 is a bit located at address 0x1B[1]. This bit is part of the location PWS.

SPI ignore 17th clock to allow negative edge host sampling.

PWS.H2T

The field H2T is a bit located at address 0x1B[2]. This bit is part of the location PWS. Turns uses hysteresis if 1.

0 = Use nonhysteresis angle for turns counter

1 = Use hysteresis angle for turns counter

This affects special register PTANG (0x3A).

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PWS.DM

The field DM is a bit located at address 0x1B[3]. This bit is part of the location PWS.

Disable Manchester interface.

If 1, any Manchester input.

PWS.SPDRV

SENT and PWM pin drive strength.

PWS.ZAL

The field ZAL is a bit located at address 0x1B[9]. This bit is part of the location PWS.

Zero offset after linearization:

0 = Before linearization and rotation
1 = After linearization

PWS.PO

POR offline. SSENT only. If 1, SSENT is offline at POR. If 0, SSENT goes online with slot counter 0.

PWS.LS

The field LS is a bit located at address 0x1B[10]. This bit is part of the location PWS.

Linearization scale:

0 = ±22.5 degrees
1 = ±45 degrees

PWS.IS

Idle sync (SSENT only). If 1, an idle SENT bus > 511 ticks resets the slot counter to 0.

PWS.ELI

The field ELI is a bit located at address 0x1B[11]. This bit is part of the location PWS.

Enable linearization:

0 = Disabled
1 = Enabled

PWS.PES

The field PES is a bit located at address 0x1B[12]. This bit is part of the location PWS.

PWM error select (if PEO = 1).

0 = PWM tristated, must reset (or set PEO back to 0 in shadow) to release the PWM output.

1 = PWM carrier frequency halved and highest priority error output on PWM as selected duty cycle.

PWS.PEO

The field PEO is a bit located at address 0x1B[13]. This bit is part of the location PWS.

PWM error output enable. If 1, PES selects the response to an enabled error.

PWS.PHE

The field PHE is a bit located at address 0x1B[14]. This bit is part of the location PWS.

PWM hysteresis enable. If 1, use hysteresis on angle going to PWM.

PWS.MEPE

The field MEPE is a bit located at address 0x1B[15]. This bit is part of the location PWS.

If 1, the Manchester auxiliary interrupt pulse and the F_AUX pulse are enabled; else, the auxiliary interrupt pulse and the F_AUX pulse are ignored, and Manchester communication is only accessible when PWM and SENT are deactivated.

PWS.PWM_FREQ

The field PWM_FREQ is a bit field located at address 0x1B[19:16]. This bit field is part of the location PWS.

PWM frequency select. Together with the PWS.PWM_BAND field, defines the PWM carrier frequency. See the PWM Output section for more details.

PWS.PWM_BAND

The field PWM_BAND is a bit field located at address 0x1B[22:20]. This bit field is part of the location PWS.

PWM frequency band. Together with the PWS.PWM_FREQ field, defines the PWM carrier frequency. See tthe PWM Output section for more details.

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PWS.PEN

The field PEN is a bit located at address 0x1B[23]. This bit is part of the location PWS.

When set to 1, PWM is enabled and overrides any SENT setting.

If 0, SENT_MODE field determines state of PWM/SENT pin.

PWS.FP_ADJ

Function pulse adjust. Long SSENT (SENT_MODE 7) only. Increases the lower threshold of the F_OUTPUT pulse by the number of ticks in this field (0 through 3).

Location 0x1C (ANG)

ANG.ZERO_OFFSET

The field ZERO_OFFSET is a bit field located at address 0x1C[11:0]. This bit field is part of the location ANG.

Post-compensation zero offset (or DC adjust) at angle resolution. This value is subtracted from the measured angle. PWS.ZAL bit determines if ZERO_OFFSET is applied before or after linearization.

ZAL = 0	ZERO_OFFSET precedes linearization.
ZAL = 1	ZERO_OFFSET follows linearization.

ANG.HYSTERESIS

The field HYSTERESIS is a bit field located at address 0x1C[17:12]. This bit field is part of the location ANG.

Angle hysteresis threshold, angle resolution × 4 (14 bit). Range is approximately 0 degrees to 1.384 degrees.

ANG.RO

The field RO is a bit located at address 0x1C[18]. This bit is part of the location ANG.

Rotation direction (pre-linearization). If set to 0, increasing angle movement is in the clockwise direction when looking down on the top of the die. If set to 1, increasing angle movement is in the counter-clockwise direction.

ANG.RD

The field RD is a bit located at address 0x1C[19]. This bit is part of the location ANG.

Rotate die. Rotates final angle by 180 degrees. This is the last step in the angle processing algorithm. This is a convenient setting to adjust one die in a dual-die package for conformance to the other die.

ANG.ORATE

The field ORATE is a bit field located at address 0x1C[23:20]. This bit field is part of the location ANG.

Reduces the output rate by averaging samples. 2^{ORATE} samples are averaged. ORATE values greater than 12 are reduced to 12 in the logic, meaning that up to 4096 samples = 4 ms can be selected as averaging time.

Location 0x1D (LPC)

LPC.TCP

The field TCP is a bit located at address 0x1D[11]. This bit is part of the location LPC.

Turns counter PLL:

0	Turns uses ZCD angle.
1	Turns uses PLL angle, except if PLL lock is lost. Ensure the ZCD_TURNS_OFFSET aligns the ZCD angle near the PLL angle.

LPC.TURNS_INIT

The field TURNS_INIT is a bit field located at address 0x1D[19:18]. This bit field is part of the location LPC.

Turns initialization at power-up.

00, 01	Turns counter zeroed at power-up.
10	Turns counter set to full settings angle (turns register may be non-zero).
11	Turns counter set to settled angle offset from 180- or 45-degree configuration (MSB 10 or 12 bits zeroed), turns register starts at zero.

LPC.T45

The field T45 is a bit located at address 0x1D[23]. This bit is part of the location LPC.

Turns counter resolution is 45° if set to a 1, and 180° if set to a 0.

Location 0x1E (COM)

COM.MAG_THRES_LO

The field MAG_THRES_LO is a bit field located at address 0x1E[5:0]. This bit field is part of the location COM.

Magnetic field low comparator value. Field value equals low field error threshold in gauss divided by 16.

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COM.MAG_THRES_HI

The field MAG_THRES_HI is a bit field located at address 0x1E[11:6]. This bit field is part of the location COM.

Magnetic field high comparator value. Field value equals maximum field threshold in gauss divided by 32. If set to 0, high threshold is disabled.

COM.DHR

The field DHR is a bit located at address 0x1E[12]. This bit is part of the location COM.

Disable hard reset. Initiates in serial CTRL register special if 1.

COM.DST

The field DST is a bit located at address 0x1E[13]. This bit is part of the location COM.

Disable self-test. Initiates in serial CTRL register special if 1.

COM.CUD

The field CUD is a bit located at address 0x1E[14]. This bit is part of the location COM.

If 1, the CUSTOMER word 0x1F uses the DUR and DEL configuration in addition to the CUSTOMER2 word 0x17.

COM.DEL

The field DEL is a bit located at address 0x1E[16]. This bit is part of the location COM.

Disable EEPROM lock for CUST2 (EEPROM word 0x17) and, if CUD = 1, CUST word 0x1F. EEPROM lock does not affect the ability to write to word 0x17 (and 0x1F if enabled).

COM.DUR

The field DUR is a bit located at address 0x1E[17]. This bit is part of the location COM.

Disable unlock requirement for CUST2 (EEPROM word 0x17) and, if CUD = 1, CUST word 0x1F.

COM.CSE

The field CSE is a bit located at address 0x1E[18]. This bit is part of the location COM.

Enable CVH self-test at power-up.

COM.LBE

The field LBE is a bit located at address 0x1E[19]. This bit is part of the location COM.

Power-up logic BIST enable.

COM.LOCK

The field LOCK is a bit field located at address 0x1E[23:20]. This bit field is part of the location COM.

Lock options:

1100 Lock EEPROM writes.

0011 Lock EEPROM writes and shadow register writes.

Location 0x1F (CUS)

CUS.CUSTOMER

The field CUSTOMER is a bit field located at address 0x1F[23:0]. This bit field is part of the location CUS. This field may be written with customer tracking, ID, or any other pertinent data.

Location 0x20 (LIN00)

LIN00.LINEARIZATION ERROR SEGMENT 0

The field LINEARIZATION ERROR SEGMENT 0 is a bit field located at address 0x20[11:0]. This bit field is part of the location LIN00.

Correction value at segment boundary. Signed, resolution is based on LS bit. Is subtracted from sensor angle to produce linearized angle.

LS = 0 Range is ±22.5 degrees.

LS = 1 Range is ±45 degrees.

LIN00.LINEARIZATION ERROR SEGMENT 1

The field LINEARIZATION ERROR SEGMENT 1 is a bit field located at address 0x20[23:12]. This bit field is part of the location LIN00.

Correction value at segment boundary. Signed, resolution is based on LS bit. Is subtracted from sensor angle to produce linearized angle.

LS = 0 Range is ±22.5 degrees.

LS = 1 Range is ±45 degrees.

NOTE: Linearization segments 2 through 29 have been omitted from the datasheet for reasons of brevity.

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Location 0x2F (LIN15)

LIN15.LINEARIZATION ERROR SEGMENT 30

The field LINEARIZATION ERROR SEGMENT 30 is a bit field located at address 0x2F[11:0]. This bit field is part of the location LIN15.

Correction value at segment boundary. Signed, resolution is based on LS bit. Is subtracted from sensor angle to produce linearized angle.

LS = 0 Range is ±22.5 degrees.

LS = 1 Range is ±45 degrees.

LIN15.LINEARIZATION ERROR SEGMENT 31

The field LINEARIZATION ERROR SEGMENT 31 is a bit field located at address 0x2F[23:12]. This bit field is part of the location LIN15.

Correction value at segment boundary. Signed, resolution is based on LS bit. Is subtracted from sensor angle to produce linearized angle.

LS = 0 Range is ±22.5 degrees.

LS = 1 Range is ±45 degrees.

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SAFETY AND DIAGNOSTICS

The A33003 was developed in accordance to the ASIL design flow. It incorporates several diagnostics.

Alive Counter

A 32-bit counter increments periodically from zero after a power-on reset or a hard reset. It is read via AUX.ALV. The alive increment period is 8.192 ms.

The alive counter can overflow. The overflow period of the counter is [2^{32} × 8.192] ms. This period is approximately 400 days.

Oscillator Watchdogs

The watchdogs run constantly when in full-power or “wake” modes. They are disabled during sleep mode and are reset when waking up to ensure there is not a false positive due to a partial clock count. These watchdogs are intended to detect gross failures of either oscillator. Logic running on clocks based on each oscillator effectively counts clock periods produced in the other clock domain and compares to expected limits.

Logic Built-In Self-Test (LBIST)

Logic BIST is implemented to verify the integrity of the A33003 logic. It can be executed in parallel with the CVH self-test. LBIST is effectively a form of auto-driven scan. The logic to be tested is broken into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudorandom data. The output of the scan chains are fed back into a multiple-input shift register (MISR) that accumulates the shifted bits into a 31-bit signature.

LBIST takes approximately 30 ms to complete.

LBIST can be enabled to run on power-up by setting COM.LBE bit in EEPROM (0x1E bit 19).

The test is complete following initialization when either:

- STA.SDN = 1 (special done) or
- STA.LBR = 0 (LBIST not running).

A failure is indicated by ERR.STF = 1.

CVH Self-Test

CVH self-test is a method of verifying the operation of the CVH transducer without applying an external magnetic field. This feature is useful for both manufacturing test and for integration debug. The CVH self-test is implemented by changing the switch configuration from the typical operating mode into a test configuration, allowing a test current to drive the CVH in place of the magnetic field. By changing the direction of the test current and by changing the elements in the CVH that are driven, the self-test circuit emulates a changing angle of magnetic field. The measured angle is monitored to determine a passing or failing device.

CVH self-test typically takes 52 ms to verify.

Self-test can be run on power-up, by setting the EEPROM field COM.CSE = 1.

Self-test can also be invoked via the serial control register by issuing the corresponding SPECIAL command.

The test is complete when either:

- STA.SDN = 1 (special done) or
- STA.CSTR = 0 (CVH self-test not running).

Failure is indicated by:

- ERR.STF = 1 (assuming it was cleared before test was run).

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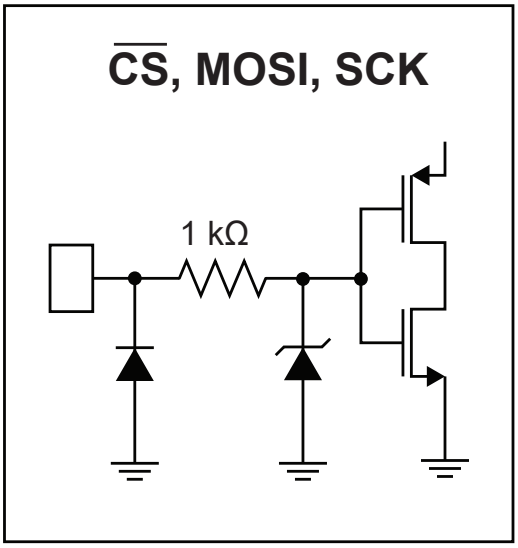
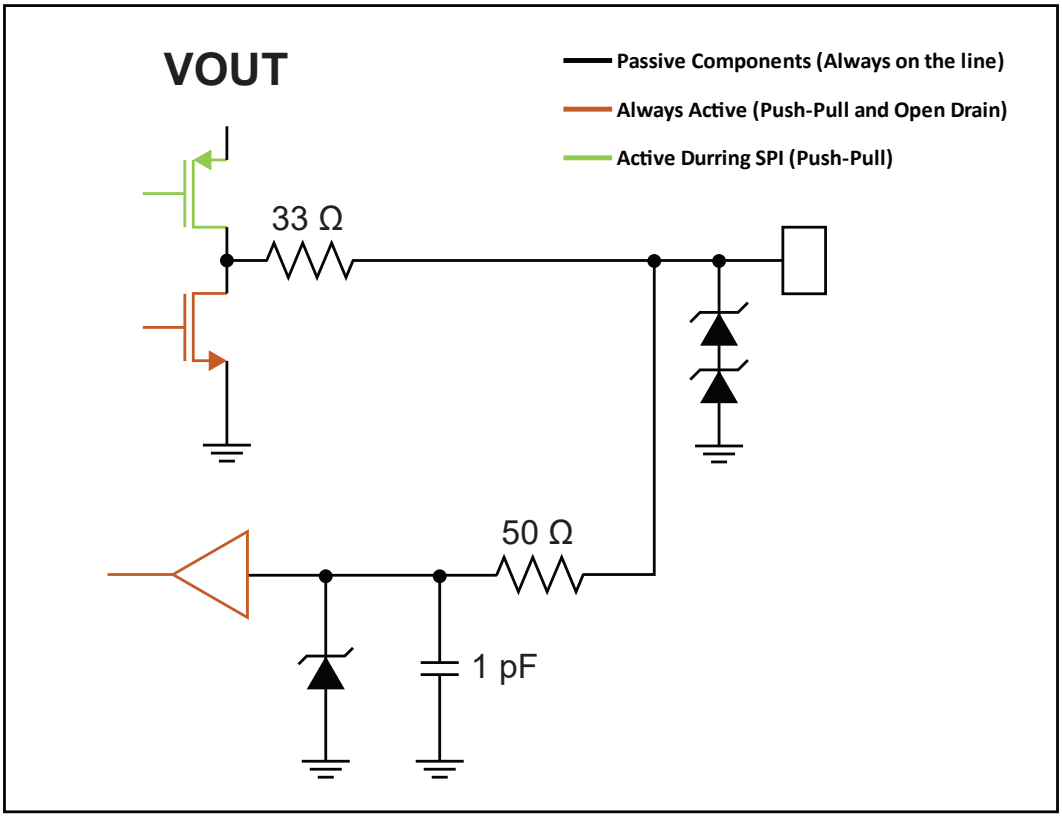
I/O STRUCTURES





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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

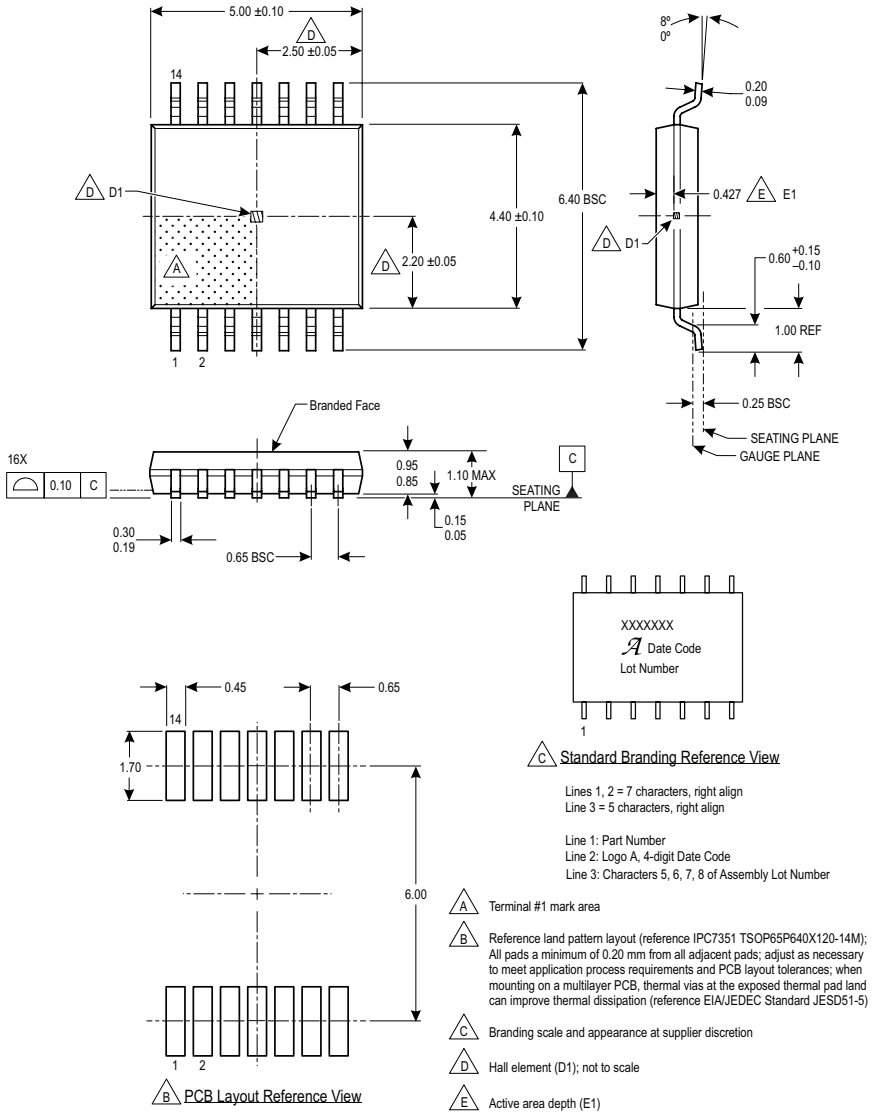

Figure 36: Package LU, 14-Pin TSSOP, Single Die

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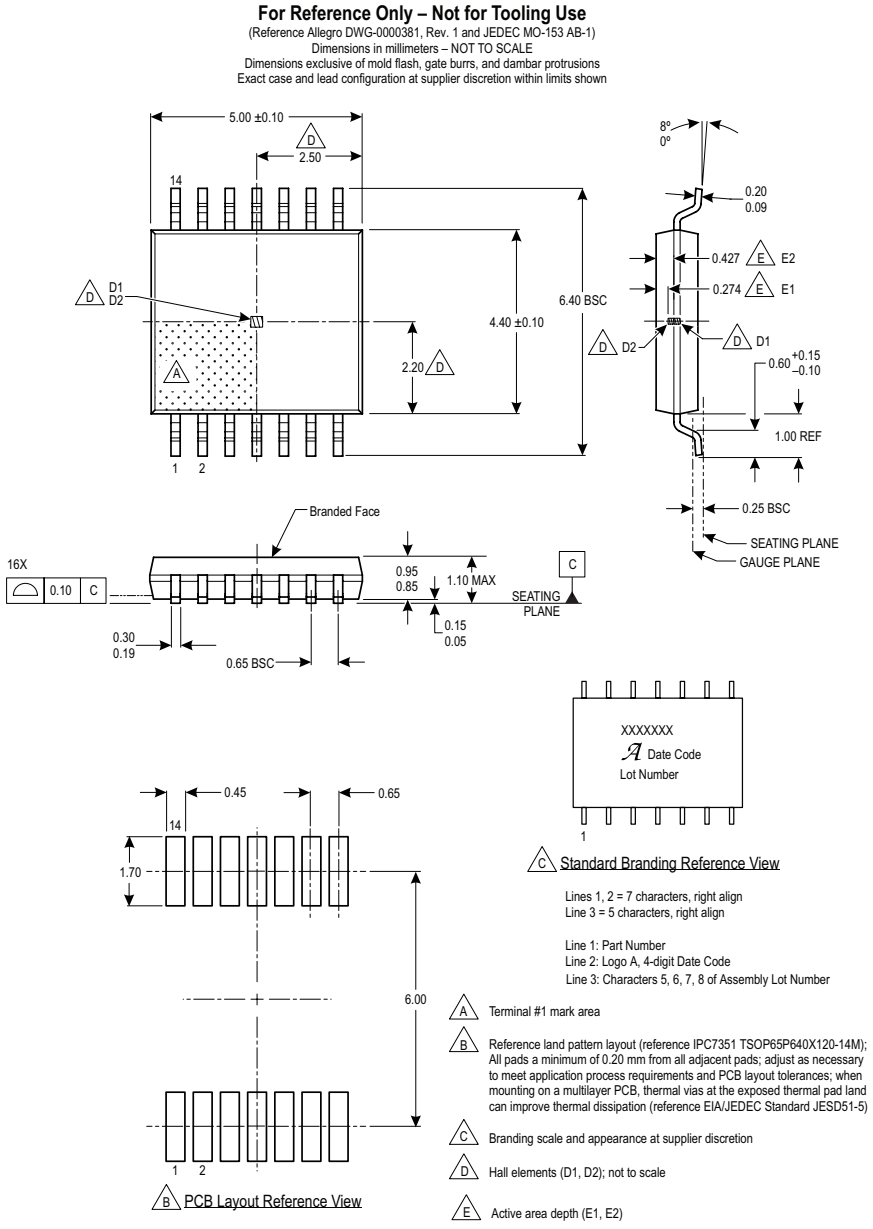

Figure 37: Package LU, 14-Pin TSSOP, Dual Die

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APPENDIX A: SENT OUTPUT DESCRIPTION

SENT Output Mode

The SENT output converts the measured magnetic field angle to a binary value mapped to the full-scale output (FSO) range of 0 to 4095, shown in Figure 38. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAE J2716 JAN2010).

The SENT frame can be configured by setting the following parameters in EEPROM (shown in Figure 38):

- SENT_MODE
- SENT_DRIVER
- DATA_MODE
- SCN_MODE
- SENT_ENABLE
- SENT_TICK

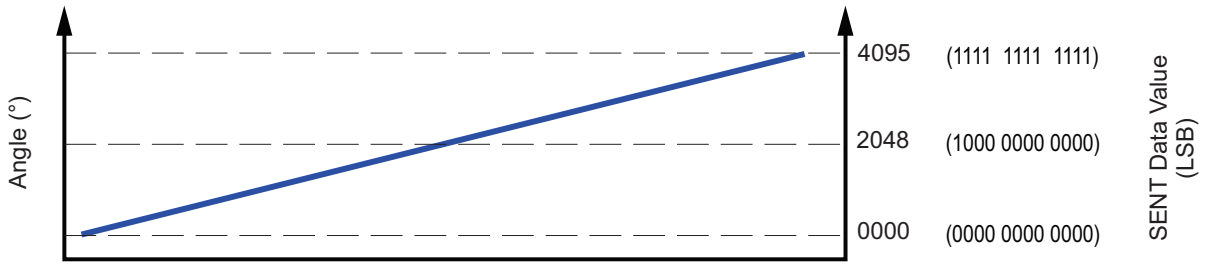

Figure 38: Angle is Represented as a 12-bit Digital Value

Table 18: Main SENT Parameter Location [1]

Address	Bits	Parameter Name	Description
0x19	22:16	SENT_TICK	Sets tick rate coefficient.
	14:12	SENT_MODE	Sets frame update rate, enables TSENT, SSENT, ASENT.
	11:8	DATA_MODE	Set data nibble format.
	7	CIS	CRC nibble includes the status and communication nibble data.
	6:4	SCN_MODE	Configure status and communication nibble contents.
0x1B	23	PEN	PWM enable. When 1, this overrides the SENT_MODE setting.
	6:4	SENT_DRIVER	SENT pin drive strength.

[1] For information about the SSENT and ASENT configuration bits, see the SSENT Specific Fields section and the ASENT/SSENT Specific Fields section, respectively.

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MESSAGE STRUCTURE

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state, which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at 5 ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the falling edge may be adjusted using the SENT_DRIVER parameter.

The duration of a nibble is denominated in ticks. The period of a tick is set by the SENT_TICK parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence (see Table 18):

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides A33003 status and the optional serial data determined by the setting of the SCN_MODE parameter.
3. **Data:** Angle information and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

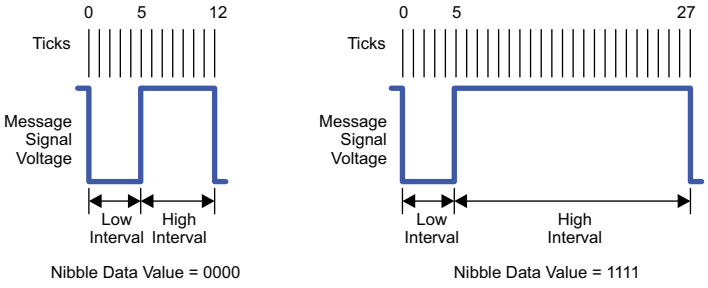

Figure 39: General Value Formation for SENT

0000 (left), 1111 (right)

Table 19: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

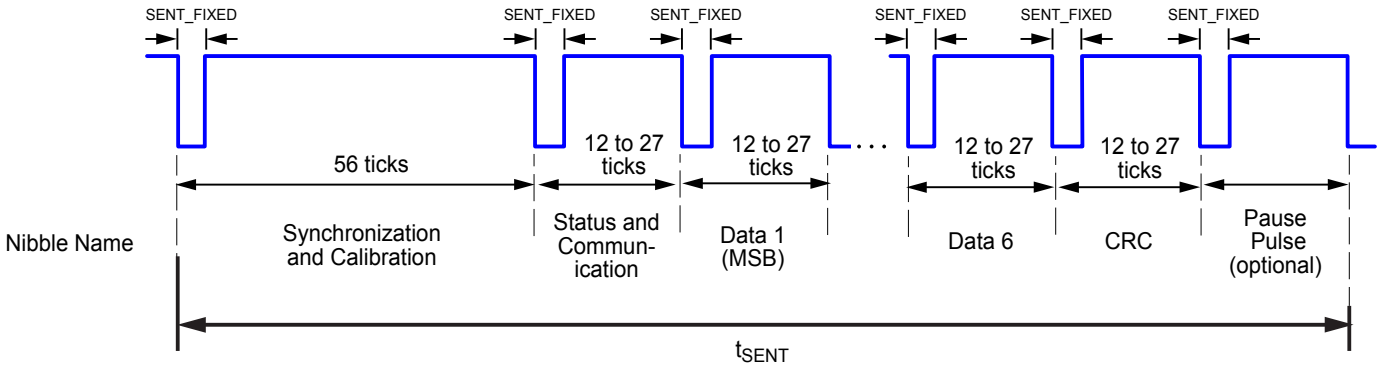

Figure 40: General Format for SENT Message Frame

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Synchronization and Calibration Pulse

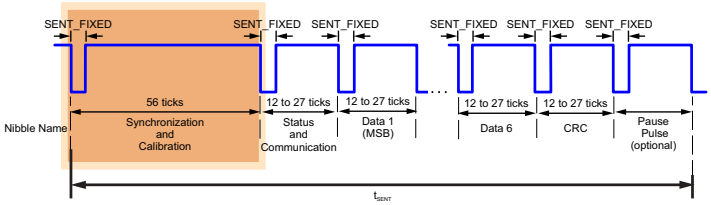

Figure 41: Synchronization and Calibration Pulse within the SENT Message Frame

The synchronization and calibration pulse is 56 ticks wide, measured from falling edge to falling edge, and delineates the start of a new message frame. The host microcontroller uses this pulse to rescale the subsequent nibble values to correct for clock variation between the controller and the sensor.

Status and Communication Nibble

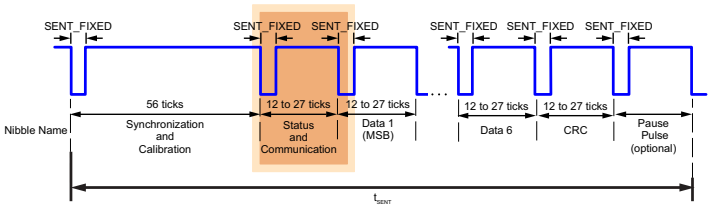

Figure 42: Status and Communication Nibble within the SENT Message Frame

The status and communication nibble (SCN) provides diagnostic information along with other status and environmental data. Nibble contents are controlled via the SCN_MODE field within EEPROM. By default, contents of the SCN are not included in the 4-bit CRC at the end of each SENT frame. The CIS bit within EEPROM enables CRC coverage of the SCN contents. It should be noted that this option is not specified in the SAE J2716 SENT standard. With the CIS bit set, the CRC is no longer compliant with that outlined in the SENT specification.

The SCN has three different types of bit values that may be present, depending on the SCN_MODE setting. These are:

a) Soft/Hard Error: Overall condition of the A33003, separated into soft and hard error flags. Detailed error information can be obtained via the expanded data nibbles, set via DATA_MODE, or through the slow serial communication.

Hard Error Flag:

Hard error flags cannot be masked and asserts independent of EEPROM mask bits.

- Latched indefinitely if any of the following occur:
  - □ Watchdog timeout
  - □ EEPROM hard error (multi-bit fault)
  - □ Self-test error
- Temporarily sets but clears after the following conditions pass:
  - □ Reset/POR
  - □ ZCD integrity error
  - □ Angle averaging error
  - □ Temperature sensor out of range
  - □ PLL not in lock

Soft Error Flag:

Soft error flags may be masked by setting the appropriate mask bit in EEPROM address 0x1A.

- Latched temporarily, clears on next SENT frame unless condition is still asserted.
  - □ Any unmasked errors asserted

b) ID Data: Die ID bits set via SA0 (SCLK) and SA1 (MOSI) pins.

- ID[0]: Value set by the logic level of the SA0 pin.
- ID[1]: Value set by the logic level of the SA1 pin.

c) Serial Data: Two bits, consisting of the SERIALSYNC and SERIALDATA bits. Together they form the "Short Serial Message" (per SAE J2716, paragraph 5.2.4.1).

- SERIALSYNC: Indicates the start of a 16-bit serial message.
- SERIALDATA: Serial data, transmitted one bit at a time, MSB first.

Table 20: SCN Bit Contents

SCN_ MODE	Bit 3	Bit 2	Bit 1	Bit 0
000	0	0	SOFT	HARD
001	SERIALSYNC	SERIALDATA	SOFT	HARD
010	ID[1]	ID[0]	SOFT	HARD
011	0	0	0	SOFT+HARD
100	0	0	ID[1]	ID[0]
101	SERIALSYNC	SERIALDATA	ID[1]	ID[0]
110	SOFT	HARD	ID[1]	ID[0]
111	SERIALSYNC	SERIALDATA	0	SOFT+HARD

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Short Serial Message Format

The SENT specification allows additional data transfer via specific bits within the SCN. This data stream is also referred to as the "slow channel".

The A33003 implements "Short Serial Message Format" as described in paragraph 5.2.4.1 of the SAE J2716 specification. A 16-bit data packet is transmitted one bit at a time over consecutive SENT message frames, starting with the MSB. The beginning of each 16-bit packet is indicated by a 1 in the SERIALSYNC bit. The message data is transmitted bit-by-bit via the SERIALDATA bit. The 16-bit message packet is separated into three different fields:

a) MESSAGE ID (4 bits):
Four leading bits of the serial data packet, used to identify data contents. Data rotates through the 16 message IDs as shown in Table 21. The message ID may be considered the 4 LSBs of a 12-bit alive counter that increments every 16 SENT frames

b) Message DATA (8 bits):
Eight bits of data.

c) CRC (4 bits):
CRC checksum, used to validate the message ID nibble and the two data nibbles. Same CRC algorithm as that used for the SENT message frame.

Sixteen separate SENT frames are needed to construct a complete 16-bit serial message. To transmit all 8 unique serial data messages (MESSAGE ID 0:7), a total of 128 SENT transmissions are necessary. 256 SENT transmissions are required for a complete rotation of the 16 MESSAGE ID fields.

Table 21: Short Serial Message Format in SENT Status and Communication Nibble

SNC Bit	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SERIALSYNC	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SERIALDATA	MESSAGE ID				DATA								CRC			

Table 22: Serial Output Data

Message ID (4 bits)	Data (8 bits)
0 (8)	8-bit alive counter (increments by one, every 0-through-15 rotation of the message ID field).
1 (9)	Temperature in degrees Celsius, offset by +64 (subtract 64 to get measured temperature).
2 (10)	Status, bits [15:8]. See Table 23.
3 (11)	Status, bits [7:0]. See Table 23.
4 (12)	Magnetic field reading in gauss, divided by 8 (multiply by 8 to obtain gauss rating).
5 (13)	CUSTOMER [23:16] from EEPROM 0x1F.
6 (14)	CUSTOMER [15:8] from EEPROM 0x1F.
7 (15)	CUSTOMER [7:0] from EEPROM 0x1F.

SENT Data Nibbles

The angle value is embedded within the first three (if using a 12-bit angle value) or four (if using a 16-bit angle value) nibbles of every SENT frame and transmitted MSB first. Additional information may be transmitted by extending the number of data nibbles, up to 6. The contents and number of data nibbles in every SENT frame are configured using the DATA_MODE field in EEPROM.

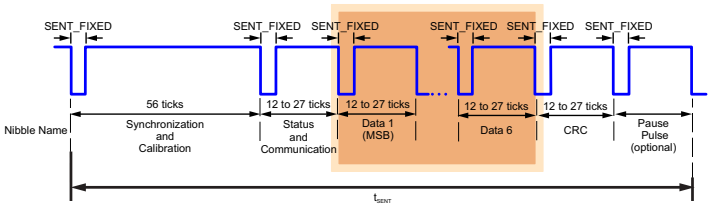

Figure 43: SENT Data Nibbles within the SENT Message Frame

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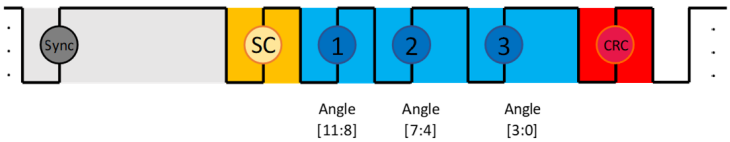
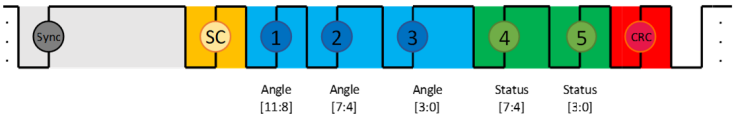
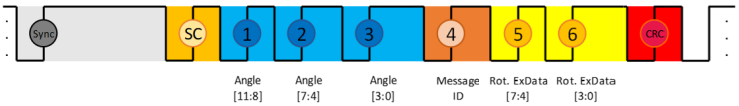
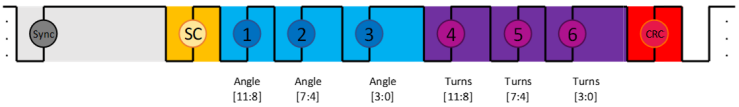
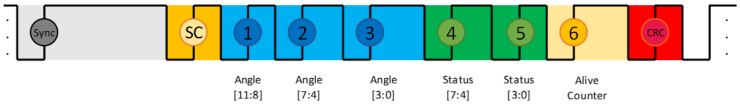
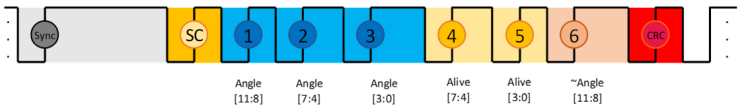
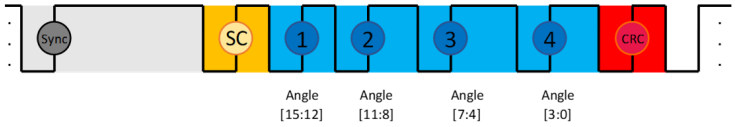
SENT Data Mode Options

DATA_MODE = 0 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data CRC = Cyclical Redundancy Check	
DATA_MODE = 1 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Status Bits CRC = Cyclical Redundancy Check	 Status[0] = 0: Status[7:1] = Upper 7 bits of SENT status flags Status[0] = 1: Status [7:1] = Lower 7 bits of SENT status flags See Table 23 for details of each status flag.
DATA_MODE = 2 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4 = Message ID 5,6 = Rotating Extended Data CRC = Cyclical Redundancy Check	 Rotating Extended Data (Nibbles 5 and 6) follow the serial message format. Message ID (Nibble 4) indicates the ID for each 8-bit packet of the serial message. See Table 21 and Table 22.
DATA_MODE = 3 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4,5,6 = Turns Counter CRC = Cyclical Redundancy Check	
DATA_MODE = 4 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Status 6 = Alive Counter CRC = Cyclical Redundancy Check	 Status[0] = 0: Status[7:1] = Upper 7 bits of SENT status flags Status[0] = 1: Status [7:1] = Lower 7 bits of SENT status flags
DATA_MODE = 5 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4,5 = Alive Counter 6 = 1's Complement of Data Nibble 1 CRC = Cyclical Redundancy Check	 When combined with SCN_MODE = 3, this implements the "Single Secure Sensor" requirement outlined in SAE J2716, Appendix A.
DATA_MODE = 6 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3,4 = Angle Data CRC = Cyclical Redundancy Check	

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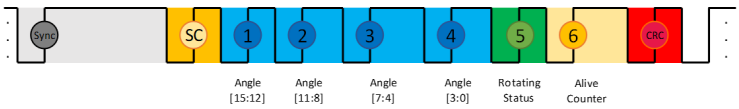
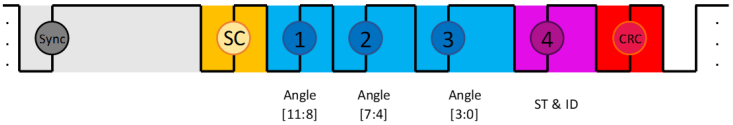
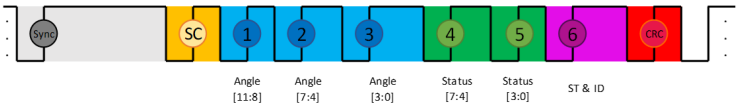
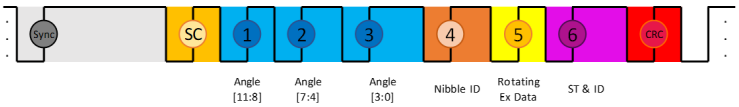
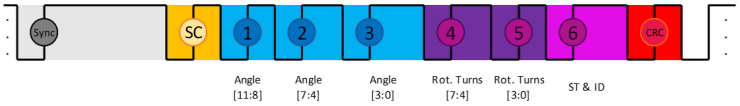
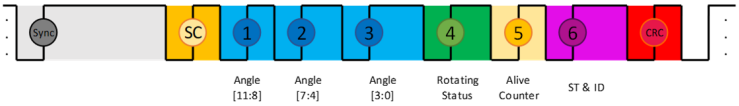
DATA_MODE = 7 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3,4 = Angle Data 5 = Rotating Status 6 = Alive Counter CRC = Cyclical Redundancy Check	 Status rotates through the status register. The alive counter [1:0] can be used to identify the quadrant of the status register data.
DATA_MODE = 8 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4 = Self-Test and ID CRC = Cyclical Redundancy Check	
DATA_MODE = 9 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Status 6 = Self-Test and ID CRC = Cyclical Redundancy Check	 Status[0] = 0: Status[7:1] = Upper 7 bits of SENT status flags Status[0] = 1: Status [7:1] = Lower 7 bits of SENT status flags
DATA_MODE = 10 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4 = Nibble ID 5 = Rotating Extended Data 6 = Self-Test Flag and ID CRC = Cyclical Redundancy Check	 Rotating extended data (Nibble 5) follow the serial message format. Message ID = 0 indicates rotating data is 4 MSBs of first packet. Message ID = 1 indicates rotating data is 4 LSBs of first packet. See Table 21 and Table 22. For a detailed data mode description, refer to the Rotating Data Information for SENT DATA_MODE 10 (rotation spanning 16 SENT frames) section.
DATA_MODE = 11 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4,5 = Rotating Turns Counter CRC = Cyclical Redundancy Check	 Rotating turns [7] = 0: Rotating turns [6:0] = Upper half of turns register. Rotating turns [7] = 1: Rotating turns [6:0] = Lower half of turns register.
DATA_MODE = 12 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4 = Rotating Status 5 = Alive Counter 6 = Self-Test and ID CRC = Cyclical Redundancy Check	 Status rotates through the status register. The alive counter [1:0] can be used to identify the quadrant of the status register data.

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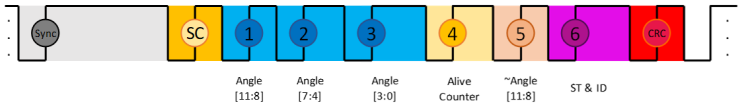
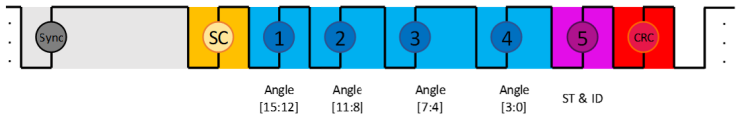
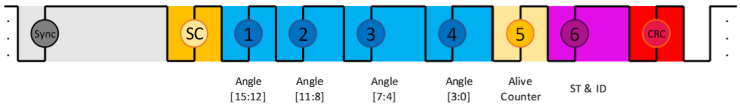
DATA_MODE = 13 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3 = Angle Data 4 = Alive Counter 5 = 1's Compliment of Nibble 1 6 = Self-Test and ID CRC = Cyclical Redundancy Check	 Modified version of the "Single Secure Sensor" implementation as outlined in Appendix A of SAE J2716.
DATA_MODE = 14 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3,4 = Angle Data 5 = Self-Test and ID CRC = Cyclical Redundancy Check	
DATA_MODE = 15 Data Nibbles: Sync = Synchronization Pulse SC = Status and Communication Nibble 1,2,3,4 = Angle Data 5 = Alive Counter 6 = Self-Test and ID CRC = Cyclical Redundancy Check	

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Self-Test and ID Nibble

The self-test and ID (ST&ID) nibble is optional. It is included as one of the extended nibbles when using DATA_MODE = 4:7. This nibble consists of the following three data bits (MSB is always 0):

Bit 3	Bit 2	Bit 1	Bit 0
0	ST	ID[1]	ID[0]

Figure 44: ST&ID Nibble

The ST bit indicates a failure of one of the three internal self-tests (CVH self-test and logic BIST). If set, this indicates significant failure of the sensor, and a reset should be initiated.

ID[0] and ID[1] provide the sensor ID value as determined via the logic values of the SA0 and SA1 pins.

This nibble is particularly useful when sharing SENT lines, because it allows the self-test diagnostic results and corresponding sensor ID to be quickly determined without a significant latency penalty (only one nibble to the SENT frame).

SENT Status Bit Description

The extensive status and error flags of the A33003 may be read at any time via SPI or by entering Manchester communication mode. To facilitate error/status flag reporting by way of the unidirectional SENT protocol, a selection of these flags are communicated via extra data nibbles when using DATA_MODE = 1, 4, 7, 9, or 12. These status flags are also transmitted via the slow serial protocol through the SCN.

The flags are 0 if the condition is clear and 1 if the condition is true. For transient conditions, the flag clears after the bit is presented on the SENT output.

Table 23: SENT Status Flag Definitions

Bit	Symbol	Definition
15	SF15	PLL not in lock.
14	SF14	Angle averaging (ORATE) or zero-crossing integrity error.
13	SF13	POR (power-on reset) occurred.
12	SF12	Temperature sensor out of range.
11	SF11	Self-test error (CVH self-test or LBIST).
10	SF10	EEPROM hard error.
9	SF9	Oscillator watchdog error.
8	R	Always 0. Indicates MSB byte.
7	SF7	Magnetic sense low.
6	SF6	Undervoltage, on V_{CC} line or analog regulator output.
5	SF5	EEPROM soft error.
4	SF4	Saturation in math computations.
3	SF3	SENT contention.
2	SF2	Magnetic sense high.
1	SF1	Turns counter overflow.
0	R	Always 1. Indicates LSB byte.

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Status Flag Locations for SENT DATA_MODE 1, 4, and 9 (spanning 2 SENT frames)

Nibble 4				Nibble 5			
SF15	SF14	SF13	SF12	SF11	SF10	SF9	R (0)

Nibble 4				Nibble 5			
SF7	SF6	SF5	SF4	SF3	SF2	SF1	R (1)

Status Flag Locations for SENT DATA_MODE 7 and 12 (spanning 4 SENT frames)

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF15	SF14	SF13	SF12	X	X	0	0

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF11	SF10	SF9	R(0)	X	X	0	1

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF7	SF6	SF5	SF4	X	X	1	0

Nibble 4 (Status Nibble)				Nibble 5 (Alive Counter)			
SF3	SF2	SF1	R(1)	X	X	1	1

Turns Count Information for SENT DATA_MODE 11 (spanning 2 SENT frames)

Nibble 4			Nibble 5
0	0	TURNS[11:10]	TURNS[9:6]

Nibble 4			Nibble 5
1	0	TURNS[5:4]	TURNS[3:0]

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Rotating Data Information for SENT DATA_MODE 10 (rotation spanning 16 SENT frames)

Nibble 4 (Rotating Data)				Nibble 5 (Rotating Data)			
NibID				NibData			
0	0	0	0	8-bit Alive counter MSBs [7:4]			
0	0	0	1	8-bit Alive counter LSBs [3:0]			
0	0	1	0	Temperature MSBs [7:4]			
0	0	1	1	Temperature LSBs [3:0]			
0	1	0	0	SF15	SF14	SF13	SF12
0	1	0	1	SF11	SF10	SF9	0
0	1	1	0	SF7	SF6	SF5	SF4
0	1	1	1	SF3	SF2	R	1
1	0	0	0	Magnetic Field [7:4]			
1	0	0	1	Magnetic Field [3:0]			
1	0	1	0	CUSTOMER [23:20]			
1	0	1	1	CUSTOMER [19:16]			
1	1	0	0	CUSTOMER [15:12]			
1	1	0	1	CUSTOMER [11:8]			
1	1	1	0	CUSTOMER [7:4]			
1	1	1	1	CUSTOMER [3:0]			

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SENT CRC Nibble

The CRC nibble is a 4-bit error checking code, implemented per the SAE J2716 SENT recommended specification.

The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$, initialized to 0101.

By default, the checksum covers only the contents of the data nibbles (nibbles 3:6). By setting the CIS bit within EEPROM, the contents of the SCN are included within the CRC nibble, which deviates from the SENT standard.

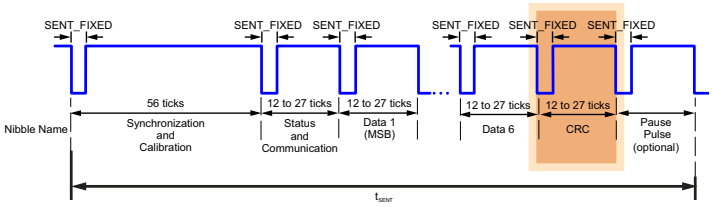

Figure 45: CRC Nibble within the SENT Message Frame

SENT Pause Pulse (Optional)

The pause pulse is an optional addition to the SENT message frame, transmitted following the CRC nibble. It acts to "fill in" the frame until the beginning of the next SENT transmission. The pulse may behave in one of two ways, based on the SENT_MODE setting.

With SENT_MODE set to 2, a pause pulse is inserted until new angle data is available. The inserted pause pulse is a minimum of 12 ticks in length. If a pause longer than 768 ticks is required, the pulse restarts, requiring a minimum of 12 more ticks.

For SENT_MODE values 3 through 7, the sensor operates in either triggered or addressable/sequential SENT mode. In these modes the sensor outputs a SENT message frame in response to host action (either a trigger or a function pulse). When not responding to the host, the sensor outputs a pause pulse of indefinite length (i.e., remains high until a host request).

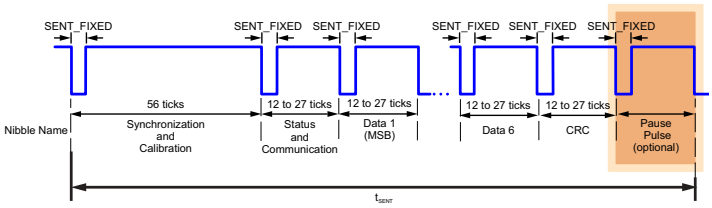

Figure 46: Pause Pulse within the SENT Message Frame

SENT_MODE 2	Low	High	Low	High
	5 Ticks	7 to 763 Ticks	5 Ticks	7 to 763 Ticks

SENT_MODEs 3 through 7	Low	High	Low (host)
	5 Ticks	Infinite (until pulled low by host)	Trigger (Min of 1.8 µs) or Function Pulse

Figure 47: SENT Pause Pulse

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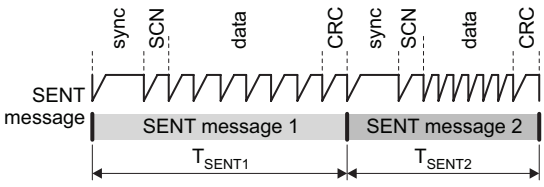
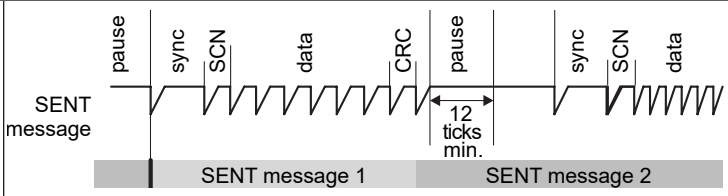
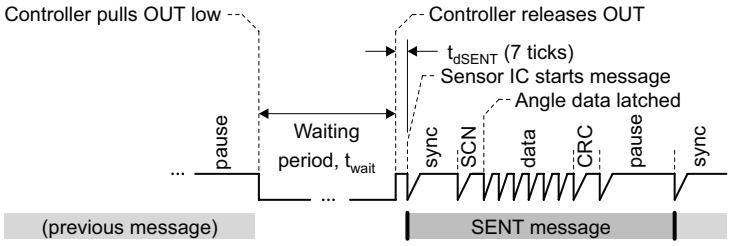
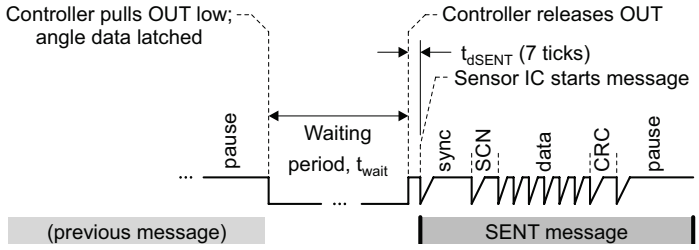
SENT OUTPUT MODE

The timing and method of SENT transmission may be configured using the SENT_MODE field within EEPROM. The method of SENT transmission falls within the following three categories:

- **Free-Running SENT**
  Angle data is automatically placed on the SENT line with no prompting from the host. Depending on settings, the SENT message frames may be transmitted back-to-back or synchronized with each update of the angle value.
- **Triggered SENT (TSENT)**
  A SENT message frame occurs only when initiated by the host. The A33003 sensor outputs a continuous pause pulse, during which the host triggers a SENT frame by pulling the SENT line low for a minimum of $T_{Trig(MIN)}$. Once released, the sensor responds with a SENT message frame.
- **Shared SENT**
  Two distinct formats—sequential SENT (SSENT) and addressable SENT (ASENT)—allow four compatible devices to share a single SENT line.

SENT_MODE	Visual	Description
000_2 (0)	–	SENT disabled.
001_2 (1)		Streaming output with variable message duration and no pause pulse. Angle data is sampled near the end of the status and communication nibble. Maximum age at time of sampling is 2^{ORATE} × 2 µs. Depending on tick time and ORATE setting, the same data may be transmitted multiple times. This mode provides the quickest data delivery rate.
010_2 (2)		SENT message frames are synchronized with the device internal update rate. Pause pulse is inserted until fresh data becomes available. Angle data is sampled between 1 to 2 tick times of the synchronization pulse. Pause pulse varies in length between 12 and 2^{ORATE} × 2 µs. (Pulse restarts after 768 ticks).
011_2 (3)		TSENT SCN sampling: Controller initiates a SENT transmission by pulling the line low during a pause pulse. After a delay of t_{dSENT}, the controller releases the output, then the SENT message begins. Angle data is latched at the end of the SCN. When latched, the data age may be up to (2^{ORATE} + 2 µs) + $t_{RESPONSE}$. This option is useful when the controller requires a prompt with a minimum "age" for the angle data.
100_2 (4)		TSENT falling-edge sampling: Similar to SENT_MODE = 3, except angle data is latched once the output line is pulled low. Useful when multiple ICs are connected to a single controller. Allows synchronous sampled data to be retrieved one device at a time, by releasing the trigger for each individual sensor. When latched, data age may vary by up to (2^{ORATE} + 2 µs) + $t_{RESPONSE}$.
101_2 (5)	–	Addressable SENT (ASENT). See Shared SENT Protocol section.
110_2 (6)	–	Sequential SENT (SSENT). See Shared SENT Protocol section.
111_2 (7)	–	Long sequential SENT. See Shared SENT Protocol section.

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SHARED SENT PROTOCOL

Addressable SENT (ASENT) and sequential SENT (SSENT) are extensions of the Allegro triggered SENT (TSENT) protocol. ASENT and SSENT allow multiple Allegro sensors with SENT output capability to coexist on a single shared SENT bus. The host (ECU) is able to select one sensor at a time, addressing that sensor to respond with a SENT output packet, thus polling each sensor on the bus over some period of time.

Like TSENT, the ASENT and SSENT protocols require an open-drain system configuration in which any sensor or the host can pull the SENT line low. The SENT line is pulled high by an external resistor to a known V_{CC}. A high level is attainable on the bus only when no device is actively pulling the line low.

In ASENT and SSENT, each sensor on the bus is assigned a unique sensor ID number between 0 and 3, allowing up to four sensors to coexist on the bus. This sensor ID number is assigned by the logic state of the SA0 and SA1 pins.

Function Pulses

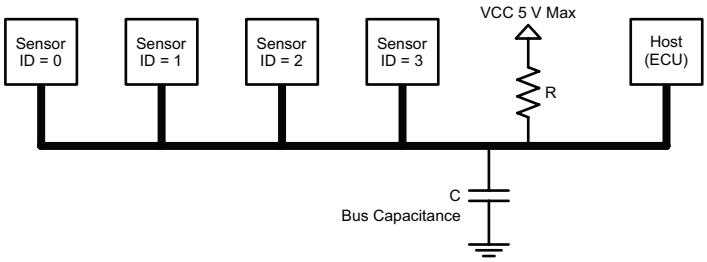

Figure 48: Shared SENT Bus Example

This section describes the different function pulses that are referenced in the Addressable SENT (ASENT) section and the Sequential SENT (SSENT) section.

The host sends communications to a sensor or sensors via different function pulses, which are equivalent in nature to a TSENT trigger pulse, but with defined widths. A function pulse is placed on the SENT bus by the host pulling the SENT line low for a defined number of ticks greater than a typical SENT pulse low period. The duration of the low time is measured by the sensors and interpreted as a designated function.

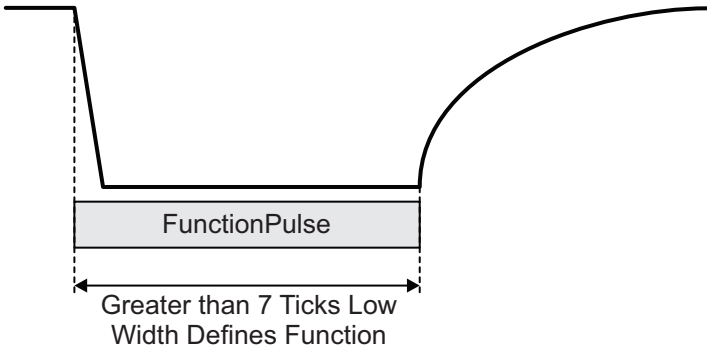

Figure 49: Function Pulse (Output by Host)

Functions that are acted upon by all sensors simultaneously are designated broadcast pulses. Functions that are acted upon by only one sensor are designated addressing pulses and are associated with a target sensor ID. A function pulse may be defined as both a broadcast pulse and an addressing pulse. For instance, all sensors sample and hold data, but only one transmits a SENT packet.

A sensor that does not support a specific function does not respond to the function pulse.

Function pulses must be greater in duration than the SENT pulse low time (5 ticks on the A33003), not to be mistaken as a part of a typical SENT transmission

The duration of function pulses are defined in SENT ticks in order to scale with the SENT frame itself. Minimum and maximum pulse durations are set such that they satisfy electrical and timing characteristics.

The various function pulses with their expected tick ranges are shown in Table 24 through Table 26.

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Table 24: ASENT Functional Pulses

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	NO_SAMPLE	15	17	19	Addressed sensor responds with SENT frame, containing either held data (from F_SAMPLE) or current data.
F_SAMPLE	Addressing/ Broadcast	NO_FSAMPLE SAMPLE_ADR	31	35	39	Except sensors configured with NO_FSAMPLE = 1, all sensors sample and hold their magnetic data. If SAMPLE_ADR = 1, this is also an addressing pulse, and addressed sensor responds with SENT frame.
F_AUX	Addressing/ Broadcast	Manchester Communication	56	63	70	If MEPE = 1, device enables Manchester communication. Otherwise, ignored.

Table 25: SSENT Functional Pulses. SENT_MODE = 6

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	NO_SAMPLE ZERO_SAMPLE	15	17	19	Addressed sensor responds with SENT frame, containing either held data (from slot 0 sampling or F_SAMPLE) or current data. If ZERO_SAMPLING = 1 and SLOT = 0, sensors sample and hold their magnetic data.
F_SAMPLE	Addressing/ Broadcast	NO_FSAMPLE SAMPLE_ADR	31	35	39	Except sensors configured for NO_FSAMPLE = 1, all sensors sample and hold their magnetic data. If SAMPLE_ADR = 1, this is also an addressing pulse, and addressed sensor responds with SENT frame.
F_AUX	Addressing/ Broadcast	Manchester Communication	56	63	70	If MEPE = 1, device enables Manchester communication. Otherwise, ignored.
F_SYNC	Broadcast		93	104	115	All sensors synchronize their slot counters such that the next slot is for sensor ID 0.

Table 26: Long SSENT Functional Pulses. SENT_MODE = 7

Function	Type	Related Options	Min Tick	Nom Tick	Max Tick	Description
F_OUTPUT	Addressing/ Broadcast	NO_SAMPLE ZERO_SAMPLE	9 [1]	Per micro-controller spec	81	Addressed sensor responds with SENT frame, containing either held data (from slot 0 sampling) or current data. If ZERO_SAMPLING = 1 and SLOT = 0, sensors sample and hold their magnetic data.
F_SYNC	Broadcast		105	140	171	All sensors synchronize their slot counters such that the next slot is for sensor ID 0.
F_AUX	Addressing/ Broadcast	Manchester Communication	216	240	264	If MEPE = 1, device enables Manchester communication. Otherwise, ignored.

[1] At tick times less than 1.5 µs, the nominal 5-tick low portion of a SENT pulse within the SENT frame may overlap with F_OUTPUT range, resulting in contention. The low side of the F_OUTPUT pulse may be increased via the PWS.FP_ADJ EEPROM field. All sensors sharing a bus must have the same FP_ADJ setting.

Sensor Measurement Range

Sensors measure function pulses to a wider range of tick times to allow for variance in falling/rising threshold and oscillator variance from sensor to sensor. Sensor measurement ranges for each type of function pulse are:

Function	Sensor Measurement Range ASENT or SSENT	Sensor Measurement Range SSENT Long
F_OUTPUT	13:27	7:94
F_SAMPLE	28:49	N/A
F_AUX	50:83	196:297
F_SYNC	84:133 (SSENT only)	95:195

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SEQUENTIAL SENT (SSENT)

SSENT Addressing Protocol

The SSENT protocol requires sensors on the bus to be polled in sequential order, meaning increasing, consecutive, and rotating order by sensor ID starting with sensor ID 0. The slot for a sensor is the time at which that sensor is expected to respond to an addressing pulse and other sensors are expected to not respond.

Each sensor independently maintains a slot counter that is incremented each time the sensor detects an addressing pulse. This slot counter becomes the slot number, which is used by the sensor to decide which sensor is being polled by the host. The slot counter is compared to the sensor ID and, if they match, that sensor responds with the SENT frame, and all other sensors do not respond, although they increment their own slot counter.

If the slot counter is incremented past the total number of sensors on the bus (MAX_SENSOR option), the slot counter is returned to 0. Each sensor must be programmed consistently with the total number of sensors so they all roll over to 0 at the same count. Sensors do not increment their slot counter on a broadcast pulse.

The SSENT protocol relies on each sensor maintaining the exact same slot number by counting the addressing pulses. In order to synchronize all sensors to the same slot number, the SSENT protocol has a broadcast F_SYNC pulse that is used by the host to force all sensors to reset their slot counter to 0.

Long SSENT (SENT_MODE = 7) allows the A33003 to work with existing shared SENT methodologies. The added overhead decreases the rate at which messages may be transmitted.

In order to reduce the burden on the host, and also to improve detection and recovery from bus contention or system errors affecting the SENT bus, the SSENT protocol has the following configuration options that can be selected.

- SLOT_MARKING. When enabled, each sensor waits a different length of time following an addressing pulse, based on their sensor ID. This leaves the SENT bus in a high state for a varying duration before the sensor pulls the line low to begin the SENT frame. All sensors on the bus (including the addressed sensor) measure this time to interpret the sensor ID of the transmitting sensor. By comparing this to the slot counter, each sensor can recognize if an unexpected sensor responded to the addressing pulse. By default, the sensor would then drop offline, because it cannot be known which sensor is out-of-sync. This option increases the overhead on the bus and therefore reduces the maximum rate at which sensors can be polled. Slot marking increases the polling time of a sensor by the slot marking time for that sensor. All sensors on a bus must be configured with the same choice for this option.

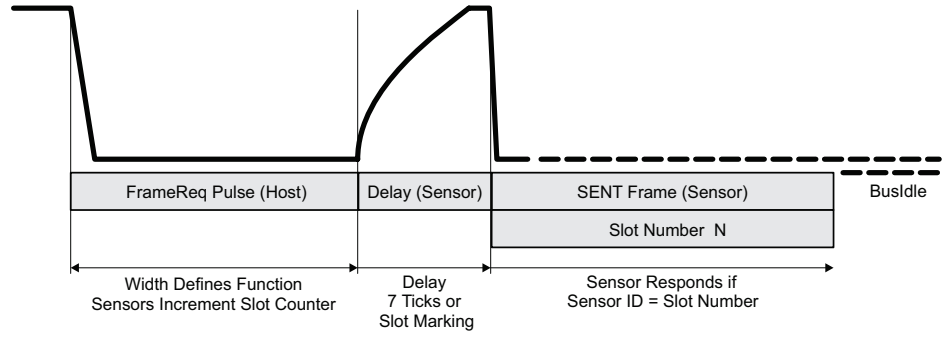

Figure 50: SSENT Sensor Addressing

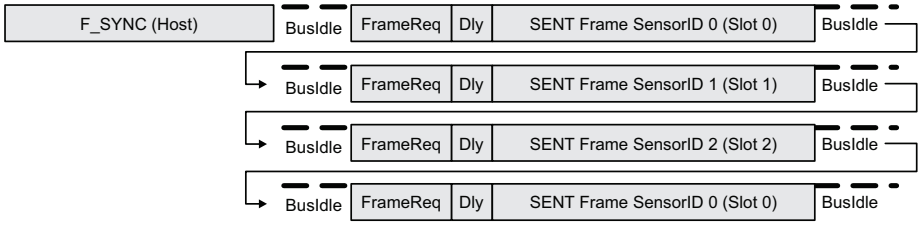

Figure 51: SSENT Sensor Addressing—No Slot Marking (Three Sensors on Bus)

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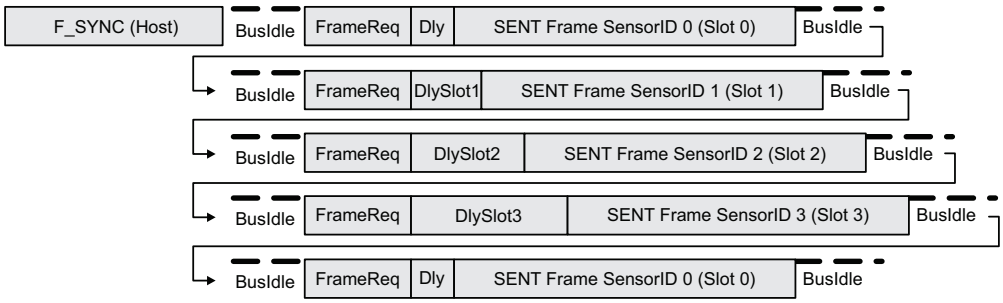

Figure 52: SSENT Sensor Addressing—With Slot Marking (Four Sensors on Bus)

Table 27: Slot Marking Delay Time

Sensor ID	Delay Time in Ticks (Nominal) [1]
0	7
1	18
2	36
3	62

[1] Delay time not intended for use by host. Tick values are approximate and differ from part to part due to oscillator variance.

- POR_OFFLINE. When enabled, a sensor remains offline until the host issues F_SYNC, or one of the other synchronization options takes effect (C_IDLE_SYNC). If disabled, a sensor powers up with its slot counter set to 0 and goes directly online. This allows the sensors to initialize without any host interaction. However, if a sensor gets a power-on reset after the bus is in operation, its counter may be out of sync with other sensors, and this could result in bus contention.
- IDLE_SYNC. When enabled, a sensor monitors the bus for a long high (bus idle) period greater than 510 ticks and resets its slot counter to 0. This option can be used if sensor polling is expected to always be periodic and continuous, such that the only extended bus idle time occurs after power-up.

SSENT Function Pulses

- **F_OUTPUT:** The addressed sensor returns a SENT frame with sampled magnetic data:
  - □ If data from a sample-and-hold operation is available (F_SAMPLE or via C_ZERO_ SAMPLE = 1), that data is returned.
  - □ If data from a sample-and-hold operation is not available, current data is sampled and returned:
    - ♦ If configured with C_ZERO_SAMPLE = 1, the sensor performs a sample-and-hold on the rising edge of the F_OUTPUT pulse for slot 0.
    - ♦ If configured with C_NO_SAMPLE = 1 and C_ZERO_ SAMPLE = 0, the sensor never performs a sample-and-hold, so it always returns current data in response to F_OUTPUT.
- **F_SAMPLE:** Except for sensors configured with NO_SAMPLE = 1, all sensors sample and hold their data at the rising edge of the pulse:
  - □ If SAMPLE_ADR = 0, this is a broadcast pulse to a sensor, and that sensor does not respond.
  - □ If SAMPLE_ ADR = 1, this is also an addressing pulse to a sensor, and the addressed sensor returns a SENT frame with either the sampled or current data.

  SAMPLE_ADR must be configured the same for all parts on the bus.
- **F_SYNC:** All sensors synchronize their slot numbers by setting their slot counters such that the next addressing pulse is for slot 0.

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ADDRESSABLE SENT (ASENT)

ASENT Addressing Protocol

The ASENT protocol allows sensors to be polled in an arbitrary order. The sensor ID is transmitted by the host following any addressing pulse as a series of 0, 1, 2, or 3 incremental address (IncAdr) pulses. After this sequence, the SENT line is left in a high state. After a time period of about 18 nominal ticks, each sensor recognizes that there are no more incoming IncAdr pulses. The sensor whose ID matches the number of IncAdr pulses received responds.

ASENT Function Pulses

- **F_OUTPUT:** Addressed sensor returns a SENT frame with sampled magnetic data:
  - □ If data from a sample-and-hold operation (F_SAMPLE) is available, that data is returned
  - □ If data from a sample-and-hold operation is not available, current data is sampled and returned.
  - □ If configured with NO_SAMPLE = 1, the sensor does not sample and hold, so it always returns current data in response to F_OUTPUT.
- **F_SAMPLE:** Except for sensors configured with NO_ SAMPLE = 1, all sensors sample and hold their data at the rising edge of the pulse:
  - □ If SAMPLE_ADR = 0, this is a broadcast pulse to a sensor, and that sensor does not respond.
  - □ If SAMPLE_ADR = 1, this is also an addressing pulse to a sensor, and the addressed sensor returns a SENT frame with either the sampled or current data.

  The SAMPLE_ADR must be configured the same for all parts on the bus.
- **F_AUX:** Sensor(s) output becomes disabled, pending a Manchester access or exit code:
  - □ If an incorrect access or exit code is sent to the device, SENT operation resumes.
  - □ To return to SENT functionality and ignore incorrect Manchester messages after the access code has been sent, an exit code must be sent.

ASENT Host Requirements:

- The host must initiate SENT frame output by selecting appropriate function pulses.
- Following any function pulse, the host must detect timeouts or SENT frame contention and take appropriate recovery action.

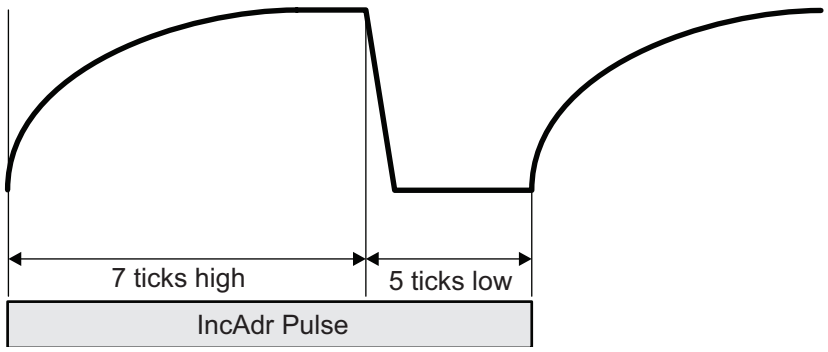

Figure 53: ASENT IncAdr Pulse (Output by Host)

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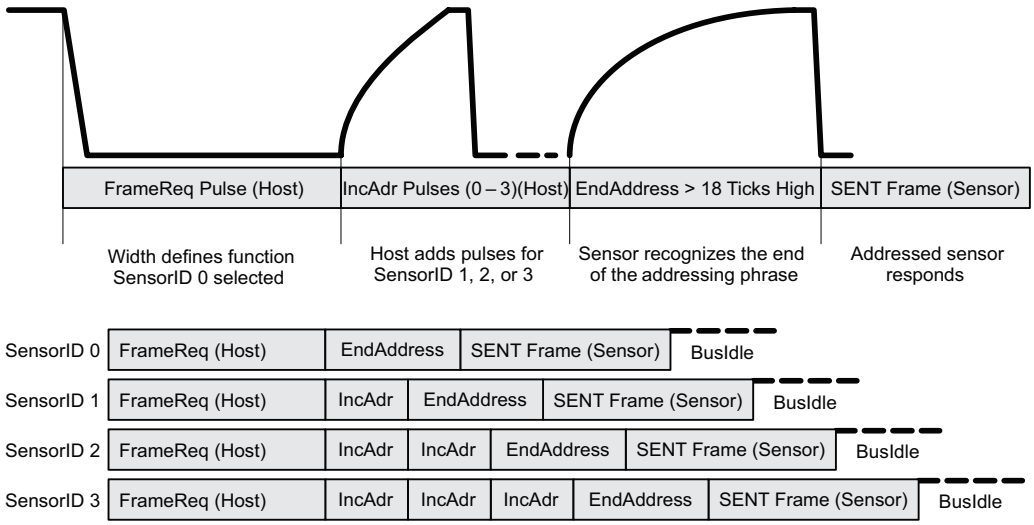

Figure 54: ASENT Sensor Addressing

SENSOR MAGNETIC DATA SAMPLING

Sensors sample their magnetic data based on a combination of function pulse and configuration options. Two types of sampling are supported: sample-on-output and sample-and-hold.

Sample-on-Output:

Sample-on-output is when the sensor samples magnetic data within a short time period preceding the transmission of that data in the SENT frame. This provides the host with a minimal latency between the data sample and its reception at the host. The sensor uses sample-on-output in the following cases:

- An F_OUTPUT function is addressed to that sensor and no held data is present.

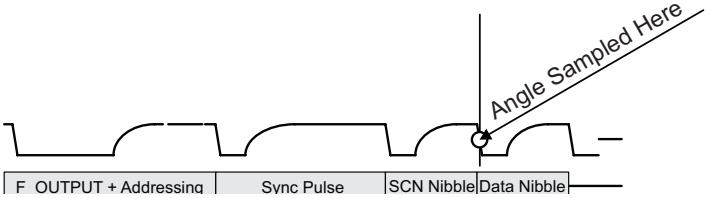

Figure 55: Sample-on-Output Example

Sample-and-Hold

Sample-and-hold is when the sensor samples magnetic data on the rising edge of a specific function pulse and holds it for output in a SENT frame later in time, when addressed. This allows the data sampling from multiple sensors to be synchronized, with the tradeoff in latency. The sensor performs a sample-and-hold of its magnetic data in the following cases:

- An F_SAMPLE function is broadcast, unless the sensor is configured with NO_FSAMPLE = 1.
- The host initiates an F_OUTPUT function in SSENT mode, the slot number is for sensor ID 0, and the sensor is configured with ZERO_SAMPLE = 1.

Once the sensor has data held from a sample-and-hold, it transmits it in the SENT frame the next time it is addressed. If the sensor is again polled before another sample-and-hold, then that sensor returns the same data unless certain events intervene, in which case the sample-and-hold data is discarded. These events are:

- A diagnostic is executed that prevents the SENT interface from obtaining valid magnetic data from the sensor logic (CVH_SELFTEST).
- The SENT interface is disabled; for instance, the SENT line is taken over by the receipt of a Manchester access code.

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If a sensor is polled and no sample-and-hold data is available (for instance, if the part comes online after a sample-and-hold has been issued), it samples current data. It is not required that all sensors on a shared bus be configured the same for sampling. This allows a subset of the sensors on a shared bus to be synchronized for data sample, while others always perform sample-on-output.

SENSOR STATES: OFFLINE, BUS SYNC, AND ONLINE

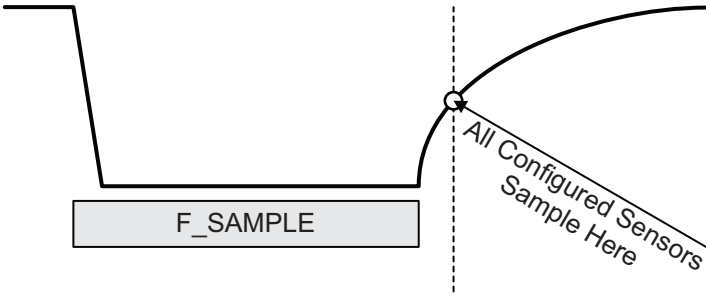

Figure 56: Sample-and-Hold (SSENT or ASENT)

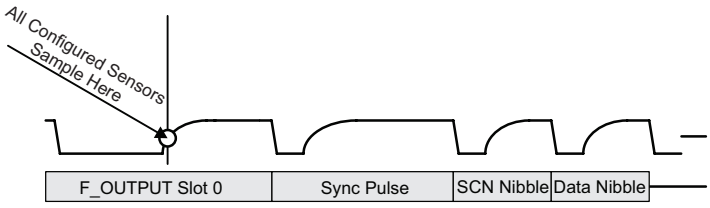

Figure 57: Sample-and-Hold

SSENT with ZERO_SAMPLE = 1

Offline

Offline is when the sensor is not actively interpreting the state of a shared SENT bus. In the offline state, the sensor does not drive the SENT bus. A sensor is offline:

- During Manchester.
- When unpowered.
- After power-up.
- After a reset that would reset the SENT logic (POR).
- During CVH self-test.
- After a bus contention is detected (unless stated otherwise).

The sensor exits the offline state and enters the BusSync state once its SENT logic becomes functional, after it monitors the SENT bus long enough to flush any internal synchronization or filtering pipelines and sees the SENT bus high. This is necessary to guarantee that any subsequent low pulses are measured as their full duration.

Bus Synchronization (BusSync)

BusSync is the state in which the sensor determines to which addressing pulse it should respond. For ASENT, this state is unnecessary, and it immediately transitions from offline to online. For SSENT, the sensor first monitors the SENT bus until it can synchronize its slot counter to the other sensors on the bus before responding to any addressing pulse, but always responds to broadcast pulses, even in the BusSync state.

A sensor configured for SSENT sets its slot counter and exits BusSync to online when:

- The host issues an F_SYNC pulse. The sensor immediately knows the next slot is for sensor ID 0, and can then respond correctly.
- IDLE_SYNC is enabled and the bus is high (BusIdle) for at least a fixed (greater than 510 ticks) period of time.
- POR_OFFLINE = 0, and the sensor exits the power-on-reset state.

Online

In the online state, the sensor is actively interpreting the shared bus, looking for and responding to function pulses. From online, a sensor goes offline when:

- It is powered down or reset.
- In response to a Manchester activation (F_AUX).
- It detects a bus contention (SSENT mode).

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SENT Message Frame Descriptions

The general format of a SENT message frame is shown in Figure 40. The individual sections of a SENT message are described in Table 28.

Table 28: SENT Message Frame Section Definitions

Section	Description
Synchronization and Calibration	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section, for ease of distinction by the external controller.
Syntax	Tick count: 56
Status and Communication	
Function	Provides the external controller with the status of the A33003 and indicates the format and contents of the DATA section.
Syntax	Nibbles: 1 Tick count: 12 to 27 Field width: 4 bits 1:0 Device status (indicates either a hard or soft error condition) 3:2 Message serial data protocol (set by SCN_MODE parameter)
Data	
Function	Provides the external controller with data selected by the SENT_DATA parameter.
Syntax	Nibbles: 3 to 6 Tick count: 12 to 27 (each nibble) Field width: 4 bits (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the data nibbles.
Syntax	Nibbles: 1 Tick count: 12 to 27 (each nibble) Field width: 4 bits
Pause Pulse	
Function	Additional time can be added at the end of a SENT message frame to synchronize each SENT message with the internal angle measurement updates, determined by the SENT_UPDATE parameter.
Syntax	Quantity of ticks: 12 tick minimum and 768 tick maximum (length determined by SENT_UPDATE option and by the individual structure of each SENT message. If a pause pulse reaches 768 ticks, it restarts with a minimum length of 12 ticks) Quantity of bits: n/a

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SENT Data Programming Parameters

Table 29: SCN_MODE (Register Address: 0x19, bits 6:4)

Function	Status and Communication Nibble Format Defines role of bits within the status and communication nibble
Syntax	Field width: 3 bits
Related Commands	–
Values	

SCN_MODE	Bit 3	Bit 2	Bit 1	Bit 0
000	0	0	SOFT	HARD
001	SERIALSYNC	SERIALDATA	SOFT	HARD
010	ID[1]	ID[0]	SOFT	HARD
011	0	0	0	SOFT+HARD
100	0	0	ID[1]	ID[0]
101	SERIALSYNC	SERIALDATA	ID[1]	ID[0]
110	SOFT	HARD	ID[1]	ID[0]
111	SERIALSYNC	SERIALDATA	0	SOFT+HARD

Options	–
Examples	The SERIALSYNC and SERIALDATA bits form a 16-bit message, transmitted over 16 consecutive SENT frames. The message contents are arranged as follows:

Short Serial Message

SCN Bit	Nibble #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SERIALSYNC	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SERIALDATA	MESSAGE ID				DATA								CRC			

Table 30: SENT_DRIVER (Register Address: 0x1B, bits 6:4)

Function	Output Signal Configuration Sets configuration of the output signal slew-rate control. Sets the ramp rate on the gate of the output driver, thereby changing slew rate at the output.
Syntax	Field width: 3 bits
Related Commands	–
Values	

Code	Fall Time (80% to 20% Typical Values) (µs)	
	C_{LOAD} = 100 pF	C_{LOAD} = 1 nF
000 (Default)	0.031	0.102
001	0.075	0.105
010	0.130	0.226
011	0.180	0.296
100	0.460	0.622
101	0.930	1.100
110	1.900	1.900
111	2.900	2.700

Options	–
Examples	–

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Table 31: DATA_MODE (Register Address: 0x19, bits 11:8)

Function	Data Nibble Format Quantity and contents of data nibbles in message. (Does not relate to data contained in the status and communication nibble.)
Syntax	Field width: 4 bits
Related Commands	–
Values	0: Nibbles 1,2,3: Angle data (nibbles 4,5,6 skipped) 1: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits, alternates between two 8-bit words 2: Nibbles 1,2,3: Angle data Nibbles 4,5,6: Rotating extended data (see the Short Serial Message Format section) 3: Nibbles 1,2,3: Angle data Nibbles 4,5,6: Turns count data 4: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits, alternates between two 8-bit words Nibble 6: Alive counter 5: Nibbles 1,2,3: Angle data Nibbles 4,5: 8-bit alive counter Nibble 6: 1's complement of nibble 1 6: Nibbles 1,2,3,4: Angle data 7: Nibbles 1,2,3,4: Angle data Nibble 5: Status bits, alternates between four 4-bit words Nibble 6: Alive counter 8: Nibbles 1,2,3: Angle data Nibble 4: Self-test and ID 9: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits, alternates between two 8-bits words 10: Nibbles 1,2,3: Angle data Nibbles 4,5: Rotating extended data (see the Short Serial Message Format section) Nibble 6: Self-test and ID 11: Nibbles 1,2,3: Angle data Nibbles 4,5: 8-bit turns counter Nibble 6: Self-test and ID 12: Nibbles 1,2,3: Angle data Nibbles 4,5: Status bits, alternates between two 8-bit words Nibble 6: Self-test and ID 13: Nibbles 1,2,3: Angle data Nibble 4: Alive counter Nibble 5: 1's complement of Nibble 1 Nibble 6: Self-test and ID 14: Nibbles 1,2,3,4: Angle data Nibble 5: Self-test and ID 15: Nibbles 1,2,3,4: Angle data Nibble 5: Alive counter Nibble 6: Self-test and ID
Options	–
Examples	–

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Table 32: SENT_MODE (Register Address: 0x19, bits 14:12)

Function	Selects between the various SENT update rates. Also used to select various modes of triggerable SENT.
Syntax	Field width: 3 bits
Related Commands	–
Values	000: Disable, no SENT output. 001: No pause pulse; new frame immediately follows previous frame. 010: SENT message frame synchronized to internal angle update rate. Pause pulse inserted to ensure each new SENT transmission corresponds to a fresh angle sample. 011: Triggered SENT mode (TSENT). Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller, SENT message begins once output is released. Data latched near end of SCN. 100: Triggered SENT mode (TSENT). Pause pulse held indefinitely until receipt of trigger pulse (OUT pulled low) from the controller, SENT message begins once output is released. Data latched on falling edge of trigger. 101: Addressable SENT mode (ASENT). See Shared SENT Protocol section. 110: Sequential SENT mode (SSENT). See Shared SENT Protocol section. 111: Long SSENT. Supports alternative SENT line sharing protocol. See Shared SENT Protocol section.
Options	–
Examples	–

Table 33: SENT_TICK (Register Address: 0x19, bits 22:16)

Function	Tick Duration Sets the SENT tick time: SENT_TICK/16 MHz = tick (µs)		
Syntax	Field width: 7 bits Any value from 0 to 127 can be used (although an internal limit of one clock period is forced)		
Related Commands	–		
Values	Code	Tick Time (µs)	Coefficient
	000 0000 [1]	0.0625	1/16 (a minimum of one clock period is forced internally)
	000 0001 [1]	0.0625	1/16
	000 0010 [1]	0.125	2/16
	000 0011 [1]	0.1875	3/16
	000 0100 [1]	0.25	4/16
	000 1000	0.5	8/16
	001 0000	1	16/16
	001 1000	1.5	24/16
	011 0000	3	48/16
	110 0000	6	96/16
	111 1110	7.875	126/16
	111 1111	7.9375	127/16
Options	–		
Examples	–		

[1] Tick times shorter than 0.5 µs are not guaranteed.

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Table 34: CIS (Register Address: 0x19, bit 7)

Function	SENT CRC includes the status and communication nibble (SCN)
Syntax	Field width: 1 bit
Related Commands	–
Values	0: SCN is not included in the CRC nibble. 1: SCN bits are included via the CRC nibble (does not conform to the J2716 SENT standard)
Options	–
Examples	–

ASENT/SSENT SPECIFIC FIELDS

Table 35: MAXID (Register Address: 0x19, bits 25:24)

Function	Specifies highest sensor ID number on the shared SENT bus
Syntax	Field width: 2 bits
Related Commands	–
Values	00: Highest ID value is 0. Sensor is not sharing the SENT line 01: Highest ID value is 1. Two sensors are sharing the SENT line 10: Highest ID value is 2. Three sensors are sharing the SENT line 11: Highest ID value is 3. Four sensors are sharing the SENT line
Options	–
Examples	–

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Table 36: NS (Register Address: 0x19, bit 3)

Function	No Sample. Sensor does not sample angle on receipt of an F_SAMPLE pulse
Syntax	Field width: 1 bit
Related Commands	–
Values	0: On receipt of an F_SAMPLE pulse, sensor samples and holds angle data 1: Sensor does not sample and hold data on receipt of an F_SAMPLE pulse
Options	–
Examples	–

Table 37: FA (Register Address: 0x19, bit 0)

Function	F_SAMPLE addressing. Sensor treats the F_SAMPLE pulse as an addressing pulse
Syntax	Field width: 1 bit
Related Commands	–
Values	0: F_SAMPLE is treated as a broadcast pulse. If NS ≠ 1, sensors sample and hold angle data on any F_SAMPLE pulse. 1: F_SAMPLE is treated as an addressing pulse. If NS ≠ 1, sensors only sample and hold angle data on an F_SAMPLE pulse if properly addressed.
Options	–
Examples	–

SSENT SPECIFIC FIELDS

Table 38: IS (Register Address: 0x1B, bit 8)

Function	IDLE_SYNC. If SENT bus idle for more than 510 ticks, sensor resets its slot counter (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: Sensor takes no action for an idle SENT line 1: If SENT line is idle for greater than 510 ticks, internal slot counter is reset to 0. All sensors sharing a SENT line should have matching IS settings
Options	–
Examples	–

Table 39: PO (Register Address: 0x1B, bit 7)

Function	POR_OFFLINE. After power-on reset, sensor remains offline (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: After a power-on reset, sensor goes online with a slot counter of 0 1: After a power-on reset, sensor remains offline; after slot counter synchronization via an F_SYNC pulse or IDLE_SYNC, sensor goes online
Options	–
Examples	–

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Table 40: SM (Register Address: 0x19, bit 15)

Function	SLOT_MARKING enable (SSENT only).
Syntax	Field width: 1 bit
Related Commands	–
Values	0: No slot marking pulses 1: Sensor outputs a bus high delay after an addressing pulse, based on sensor ID
Options	–
Examples	–

Table 41: ZS (Register Address: 0x19, bit 2)

Function	ZERO_SAMPLING. Sensor samples and holds data at Slot 0 (SSENT only)
Syntax	Field width: 1 bit
Related Commands	–
Values	0: When sensor sloct counter resets to 0, no special action is performed 1: When sensor slot counter resets to 0, sensor performs a sample and hold
Options	–
Examples	–

Table 42: FP_ADJ (Register Address: 0x1B, bits 25:24)

Function	Function Pulse Adjust. Only for long SSENT (SENT_MODE = 7). Increases the lower threshold of F_OUTPUT pulse by 0 to 3 ticks. Reduces possible misinterpretation of F_OUTPUT pulses at sub-1.5 µs tick times
Syntax	Field width: 2 bits
Related Commands	–
Values	00: No Change to F_OUTPUT pulse width. Minimum width = 9 ticks 01: Minimum width of F_OUTPUT increased by 1 tick. Min = 10 ticks 10: Minimum width of F_OUTPUT increased by 2 ticks. Min = 11 ticks 11: Minimum width of F_OUTPUT increased by 3 ticks. Min = 12 ticks
Options	–
Examples	–

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APPENDIX B: ANGLE ERROR AND DRIFT DEFINITION

Angle error is the difference between the actual positon of the magnet and the position of the magnet as measured by the angle sensor IC (without noise). This measurement is performed by reading the angle sensor IC output and comparing it with a high-resolution encoder. See Figure 58.

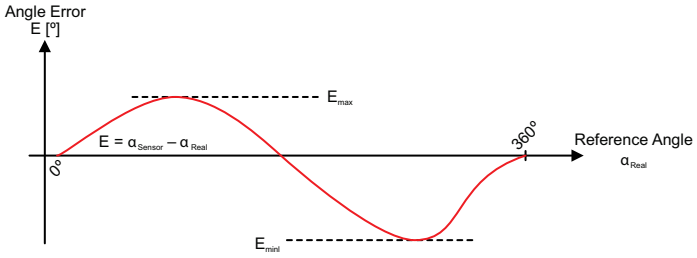


Figure 58: Angle Error Definition

Angle Error Definition

Throughout this document, the term “angle error” is used extensively. Thus, it is necessary to introduce a single angle error definition for a full magnetic rotation. The term “angle error” is calculated according to the following formula:

$$AngleError = max(|E_{max}| , |E_{min}|)$$

In other words, it is the maximum deviation from a perfect straight line between 0 degrees and 360 degrees. For the purpose of a generic definition, the offset of the IC angle profile is removed prior to the error calculation, as shown in Figure 58. The offset itself depends on the starting IC angle position relative to the encoder 0° and thus can differ anywhere from 0° to 360°.

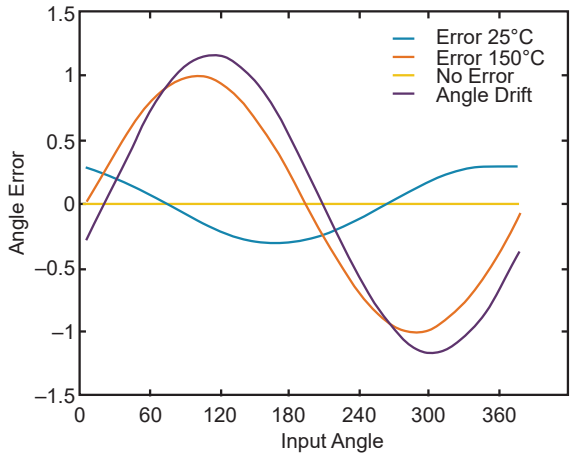
Angle Drift

Angle drift is the change in the observed angular position over temperature, relative to 25°C.

During Allegro factory trim, drift is measured at 150°C. The value is calculated using the following formula:

$$Angle_{Drift} = Angle_{25°C} – Angle_{150°C}$$

where each angle value is an array corresponding to 16 angular positions around a circle.



NOTE: This data is a simple representation of angle drift and not real data. Also, the error at 25°C and 150°C are often out of phase. This can cause a drift larger than the maximum error specification of the part, as shown.

Figure 59: Angle Drift of 150°C in Reference to 25°C

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REVISION HISTORY

Number	Date	Description
–	September 30, 2019	Initial release
1	November 22, 2019	Added footnote to Selection Guide table (page 2); updated footnote 4 (page 10)
2	October 6, 2020	Updated Interrupt Pulse Hold Time values (page 7); changed PWI to PWS (pages 23, 27, 50); corrected package drawing Hall element labels (page 62); updated Hard Error Flag and Soft Error Flag descriptions (page A-3); updated Sent Output Mode table (page A-12), tables 24-26 (page A-14); added Sensor Measurement Range section (page A-14).
3	October 14, 2020	Added footnote to Figure 3 (page 5); updated SEN.SENT_MODE description (page 53) and FWS.FP_ADJ description (page 56).
4	January 13, 2021	Updated ASIL status (page 1), Selection Guide (page 2), Bypass Pin Output Voltage (page 6), footnote 1 (page 9), Linearization section (pages 17-18), Package Drawing reference numbers (pages 62-63), Figure 46 (page A-11); added CRC section (page 27).
5	April 20, 2021	Updated “ISO 26262:2011” to “ISO 26262” (page 1), Features and Benefits (page 1-2), Angle Measurement section (page 13), Table 10 (page 32), Figure 29 (page 29), Figure 32 (page 31), and SENT Output Mode table (page A-12)
6	November 29, 2021	Removed 125°C version and corrected part number of 150°C version in selection guide (page 2); removed 125°C performance characteristics table (page 10); corrected part number (page 11); removed performance characteristics charts for 125°C version (page 12; entire page removed); In EEPROM Table, swapped the order of columns 1 and 2 (Shadow Memory Address and EEPROM Address), changed Register Names MPWS and PLPC to PWS and LPC respectively, changed Bit 1 “da” to “xa” (page 50, formerly page 51); clarified definition of SEN.XA (page 52, formerly page 53); corrected rotation direction parenthetical in ANG.ro definition (page 56, formerly page 57); In Table 22, corrected references to other table (was Table 19, now Table 23) (page A-4).
7	March 30, 2023	Updated reference design (page 5), updated SPI interface specifications (page 6), corrected footnote numbering (pages 6 through 9), added EEPROM Margin Check section (pages 39 and 40), added SENT error mask description and corrected typo in H2T bit name (page 54), updated product outline drawings (pages 61 and 62), clarified reference to data mode descriptions (page A-6), and made minor branding, editorial, and formatting corrections (all pages), including removal of archaic language (e.g., MOSI redefined as controller-out/peripheral in), addition of cross-references and hyperlinks, minimization of the use of capitalization and quotation marks, use of capitalization for bit addresses, and recreation of low-resolution images.
8	May 14, 2024	Corrected reverse voltage specification (page 2), updated EEPROM margin test (page 40), and changed the term “normal” to “typical” throughout.

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