

# Atmel AVR473: ATAVRSB202 Hardware User Guide



## Features

- Atmel® ATmega32HVB Smart Battery device evaluation and development kit
- High-side N-FETs
- 5mΩ sense resistor current measurements with 18-bit CC-ADC
- Input filters for cell voltages to the 12-bit voltage ADC
- All components on one side
- Polarity safety FET
- Holes for mounting of pin headers or wires
- ISP connector for programming via SPI, and debugging via debugWIRE interface

## 1 Introduction

The Atmel ATAVRSB202 Smart Battery board is an evaluation and development kit for the new Atmel® AVR® Smart Battery device, the [Atmel ATmega32HVB](#). This device is made for battery packs with two, three, or four lithium-ion and lithium-polymer cells in series, and feature autonomous battery protection as well as very accurate voltage, current, and temperature monitoring capabilities. The device provides the means to protect the battery pack and surroundings from hazardous conditions and gain the most from the batteries.

The kits consist of both hardware and firmware, with hardware documented here and firmware in the Atmel AVR474 application note. The boards have an edge connector for connection to the [Atmel ATAVRSB200 demonstration board](#), but can for development purposes also be used standalone.

**Figure 1-1.** Atmel SB202 evaluation kit.



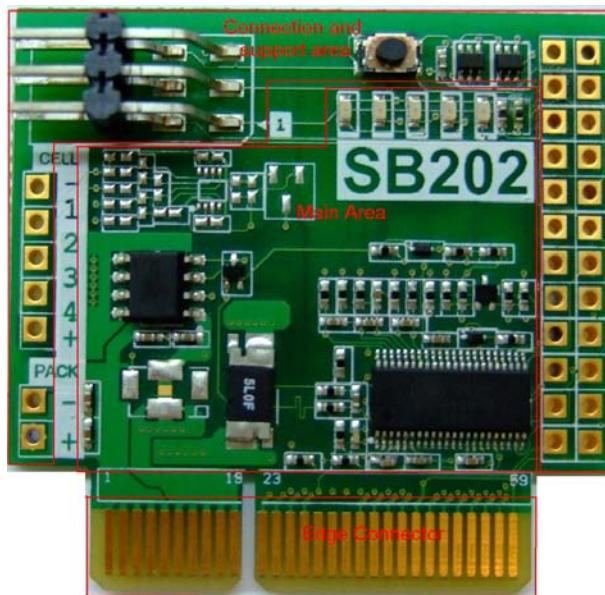
Rev. 8230A-AVR-03/11



## 2 Hardware

The Atmel SB202 board consists of three parts: the edge connector, the main area, and the connector and support area. The main area contains all the circuitry needed in a battery pack design.

**Figure 2-1.** SB202 block layout.



### 2.1 Main area

The main area contains the [Atmel ATmega32HVB](#) device, charge and discharge N-FETs, 5mΩ sense resistor, decoupling capacitors, filter capacitors/resistors for the voltage and current ADCs, and ESD protection.

### 2.2 Connector and support area

The connector area contains holes for three pin headers with 1x2, 1x5, and 2x12 pins to give access to several signals and device pins, as shown in [Table 2-1](#), [Table 2-2](#), and [Table 2-3](#). Pin headers with 2.54mm spacing or wires can be soldered in here. A connector for in-circuit programming is surface mounted. Lastly, the area contains a board ID system, which is described in more details in the following subsections.

**Table 2-1.** Signals that can be found on the 1x2 pin header holes.

Name	Description
PACK+ (J1)	Battery-pack positive input/output. Also connected to BATT pin
PACK- (J2)	Battery-pack negative input/output (ground)

**Table 2-2.** Signals that can be found on the 1x5 pin header holes.

Name	Description
CELL+/ PV4 (J3)	Cell stack positive terminal. / Cell4 positive input
PV3 (J4)	Cell3 positive input
PV2 (J5)	Cell2 positive input

Name	Description
PV1 (J6)	Cell1 positive input
CELL- / NV (J7)	Cell stack negative terminal

**Table 2-3.** Signals that can be found on the 2x12 pin header holes.

Name	Description
VREF (J32)	Voltage reference positive pin
VREF Gnd (J33)	Voltage reference ground pin
VFET (J21)	VFET pin. Supply voltage to the device
VREG (J19)	Voltage regulator output pin
Reset (J18)	Reset pin
Ground (J20)	Ground pin
PA3 (J31)	Button switch input pin
PA2 (J30)	Not used
PA1 (J29)	External NTC 2 ADC input
PA0 (J28)	External NTC 1 ADC input
PB7 (J17)	SPI MISO pin
PB6 (J16)	SPI MOSI pin
PB5 (J15)	SPI SCK pin
PB4 (J14)	LED 1 output pin
PB3 (J13)	LED 2 output pin
PB2 (J12)	LED 3 output pin
PB1 (J11)	LED 4 output pin
PB0 (J10)	LED 5 output pin
PC5 (J27)	Not used
PC4 (J26)	SMB/TWI clock pin
PC3 (J25)	SMB/TWI data pin
PC2 (J24)	One-wire USART pin (not used)
PC1 (J23)	Secondary protection blow input (not used)
PC0 (J22)	External protection input pin

In-system programming (ISP) is possible via the SPI bus interface. [Table 2-4](#) shows the connections. Alternative pin names are also noted.

**Table 2-4.** ISP connector (J2) signals.

Name	Pin no.	Description
MISO	1	Serial data out (PB7)
VCC	2	Supply voltage
SCK	3	Serial clock (PB5)
MOSI	4	Serial data in (PB6)
RESET	5	Reset signal (active low)
GND	6	Ground





## 2.2.1 Polarity safety FET

A voltage negative with respect to ground connected on the input (charger with reverse polarity) will pull the source of the discharge FET to a negative voltage, and with the ground potential on the gate, the FET will likely be turned on. Because the diode of the charge FET will conduct a discharge current, a large current will in this case flow out of the battery cells with the [Atmel ATmega32HVB](#) unable to stop it. An FET (Q3) on the pack input, which pulls the source of the discharge FET to the negative input voltage, is included in the design to avoid this situation. This is an optional part in a design, but is included in the main area.

## 2.2.2 Board ID system

A board identification system is included to allow the Atmel SB200 to recognize which board is inserted. The wiring and thus response of this is the same as on the Atmel SB202, and so the user must select in the software if it is a two-, three-, or four-cell application. The board ID system is not relevant for standalone use of the SB202 or designs with the [ATmega32HVB](#).

## 2.2.3 Cell balancing

The [ATmega32HVB](#) contains internal cell-balancing FETs. Cell balancing is controlled by the internal registers, and will enable an FET between NV, PV1, PV2, PV3, and PV4 on the SB202. The cell balancing current must be limited with series resistors R12, R13, R15, R16, and R17, and must be in the range specified in the [ATmega32HVB datasheet](#).

## 2.3 Edge connector

The edge connector provides a quick and secure connection to the SB200 demonstration board.

### 3 Connecting batteries to Atmel SB202

The SB202 is made for two, three, and four series cell battery packs. The connections are described in the following subsections.

#### **WARNING**

*Li-ion batteries must be handled with care as they may pose a safety hazard if treated incorrectly. It is important that the development of Li-ion battery applications be done by people who are skilled and knowledgeable of the correct use and handling of such batteries.*

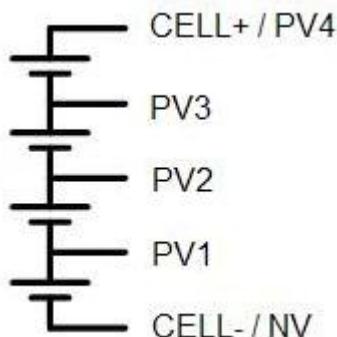
#### 3.1 Four-cell SB202 application

For applications with four series cells, connect the cells as shown in [Figure 3-1](#): negative terminal of cell one to CELL-, negative terminal of cell two and positive terminal of cell one to PV1, negative terminal of cell three and positive terminal of cell two to PV2, negative terminal of cell four and positive terminal of cell three to PV3, and finally positive terminal of cell four to CELL+/PV4.

Load or charge the batteries through PACK+ and PACK-.

To start the part and thus possibly open the FETs, a charge condition must be initiated by a charger.

**Figure 3-1.** Connection of four cells in a series pack to the SB202.



#### 3.2 Three-cell SB202 application

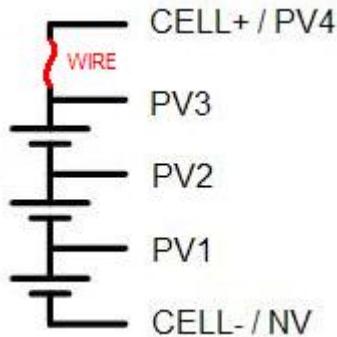
For applications with three series cells, connect the cells as shown in [Figure 3-2](#): Negative terminal of cell one to CELL-, negative terminal of cell two and positive terminal of cell one to PV1, negative terminal of cell three and positive terminal of cell two to PV2, positive terminal of cell three to PV3. PV3 and CELL+/PV4 should be connected through PCB tracks on the Atmel SB200 or through wires. When the SB202 is connected to the SB200 through the side connector, the jumper of the SB200 should be mounted to the correct socket representing the number of cells. Please note that in such a case, an incorrect jumper position may bring short-circuit risks. If the SB202 is used standalone for development (without the SB200), wires will need to be soldered to create the connections.

Load or charge the battery through PACK+ and PACK-.

To start the part and thus possibly turn on the FETs, a charge condition must be initiated by a charger.



**Figure 3-2.** Connection of three cells in a series pack to the SB202.



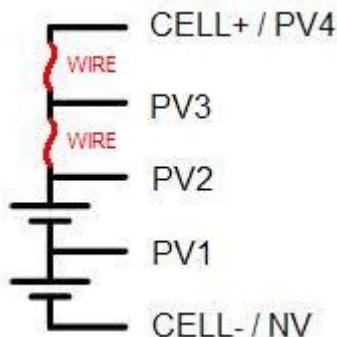
### 3.3 Two-cell SB202 application

For applications with two series cells, connect the cells as shown in [Figure 3-3](#): Negative terminal of cell one to CELL-, negative terminal of cell two and positive terminal of cell one to PV1, positive terminal of cell two to PV2. PV2 and CELL+/PV4 should be connected through PCB tracks on the Atmel SB200 or through wires. When the SB202 is connected to the SB200 through the side connector, the jumper of the SB200 should be mounted to the correct socket representing the number of cells. Please note that in such a case, an incorrect jumper position may bring short-circuit risks. If the SB202 is used standalone for development (without the SB200), wires will need to be soldered to create the connections.

Load or charge the battery through PACK+ and PACK-.

To start the part and thus possibly open the FETs, a charge condition must be initiated by a charger.

**Figure 3-3.** Connection of two cells in a series pack to the SB202.



## 4 Secondary protection

The board has footprints for a secondary protection circuit. This can be soldered in the available footprint to enable a secondary protection on the board.

The secondary protection circuit footprint is made for a Seiko protection circuit, part number S-8244AAGPH-CEGTFG (4.45V).

The fuse footprint is for a Sony fuse, part number SFH-1412A. To solder in this fuse, the track beneath it has to be cut.

The FET for blowing the fuse can be any FET in a SOT-23 package that is rated for the current to blow the fuse. The footprint was made for a PMV31XN FET.

The resistor and capacitor footprints are made for SMD 0402 packaging.

## 5 Programming

The board can be programmed with the Atmel [STK<sup>®</sup>500](#), Atmel [STK600](#), Atmel [AVRISPmkI/mkII](#), Atmel [AVR JTAGICE mkII](#), and Atmel [AVR Dragon<sup>™</sup>](#) via the ISP socket. See the [Atmel ATmega32HVB datasheet](#) and the [Atmel AVR Studio<sup>®</sup>](#) help for connections.

## 6 Debugging

The [Atmel ATmega32HVB](#) features on-chip debugging via a debugWIRE interface, with either the [AVR JTAGICE mkII](#) or the [AVR Dragon](#).

Please notice that if not enabled, the debugWIRE interface must be enabled via the ISP interface, and then disabled after debugging to enable ISP again. This is described in the AVR Studio help. Leaving the [ATmega32HVB](#) with the debugWIRE enable (DWEN) fuse on will increase current consumption.

## 7 Powering up the Atmel SB202

Please see the [ATmega32HVB datasheet](#) for how to wake up the device from power off mode, and thus enable programming and/or operation. The Atmel SB200 provides this functionality automatically and manually.

## 8 Considerations when using the SB202 in the SB200

### WARNING

*Connecting the SB20x in an SB200 with more cells mounted than the cell count selected will result in the destruction of tracks as some tracks might be shorted. Be sure to use the correct board with the correct number of cells.*



## 9 Specifications

Maximum continuous current:  $\pm 6A$

Maximum input voltage: 16.8V

**Table 9-1.** Typical power consumption.

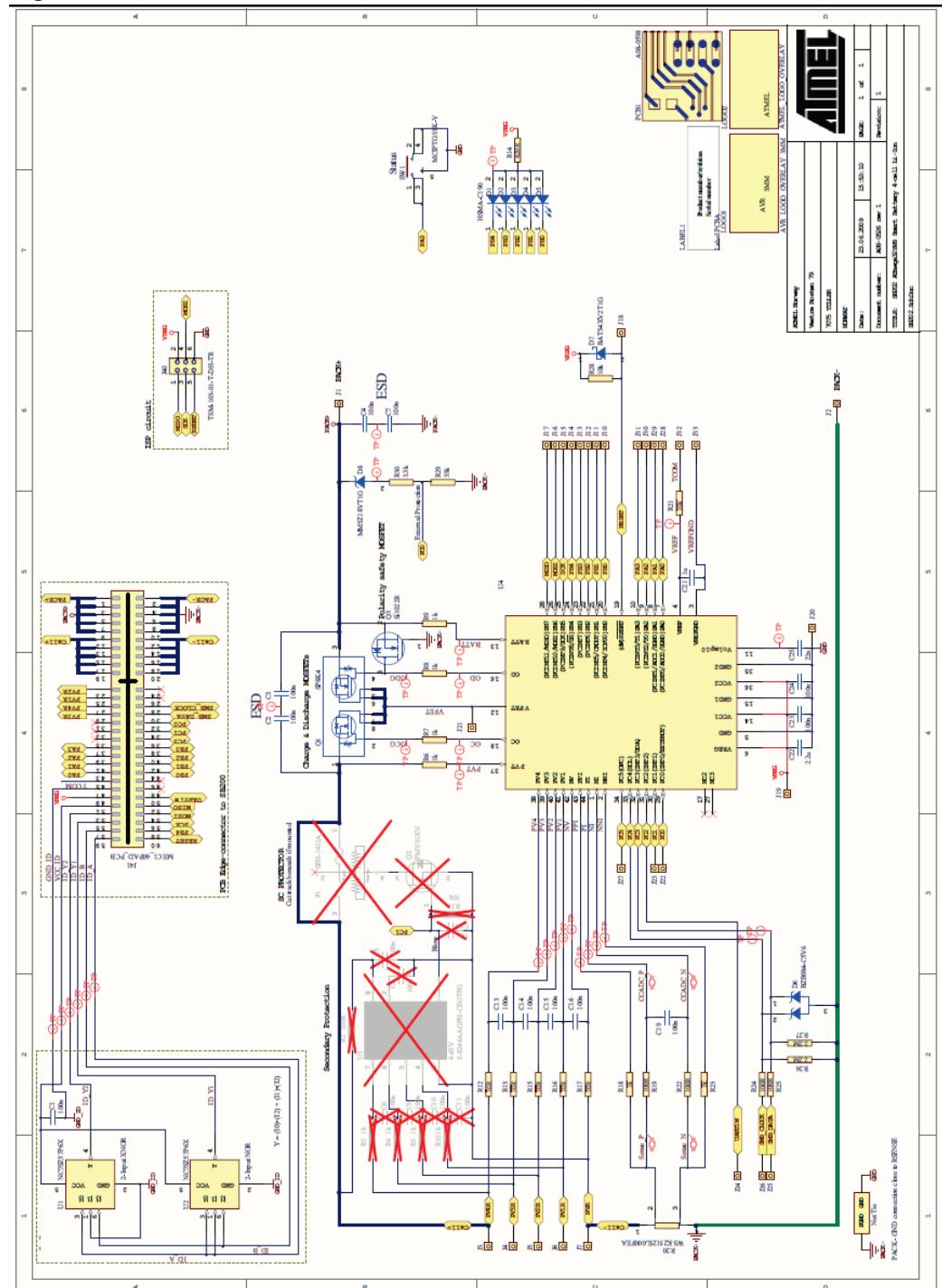
Frequency (MHz)	Active mode ( $\mu A$ )	Idle mode ( $\mu A$ )	Power save ( $\mu A$ )
1	760	215	85

Application current consumption is dependant on the firmware and on whether or not communications in the [Atmel ATmega32HVB](#) are active.

## 10 Schematic

The schematic for the Atmel SB202 is provided in the .zip file that can be downloaded from [Atmel AVR application notes](#). A small version of the common schematic is shown in Figure 10-1.

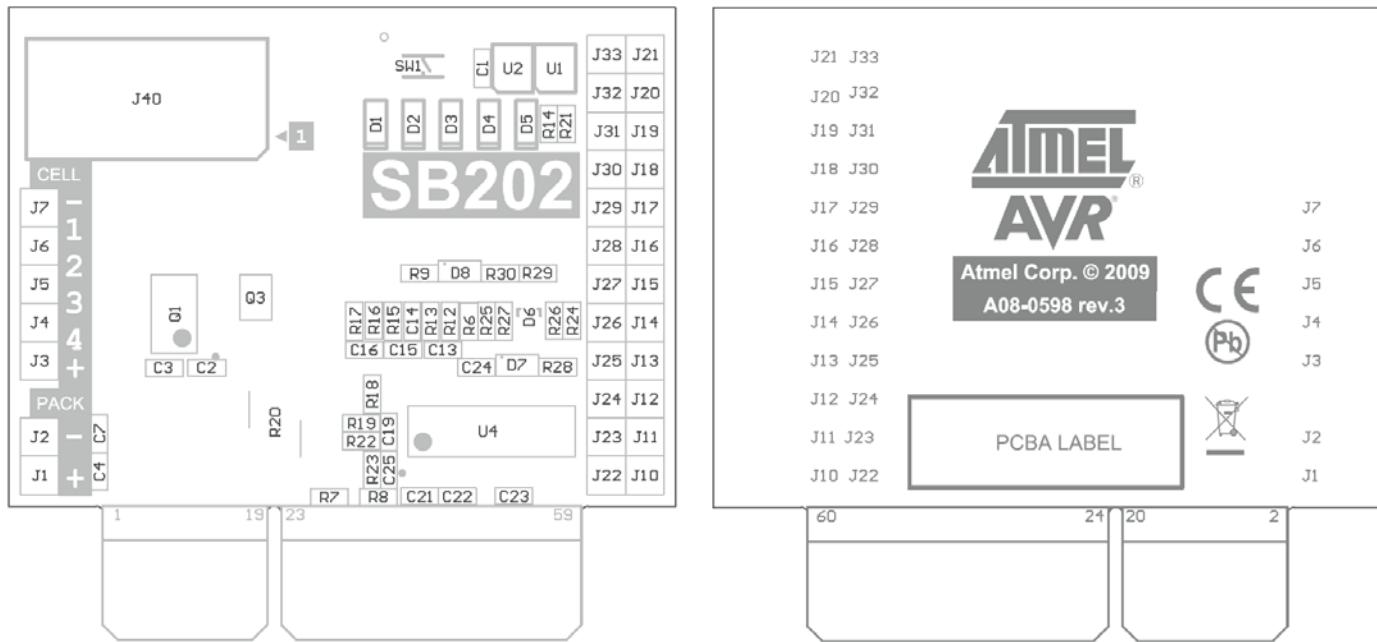
**Figure 10-1.** Schematic for SB202.



## 11 Component placement

Component placement for the Atmel SB202 is provided in the .zip file that can be downloaded from [Atmel AVR application notes](#). A small version of SB202 is shown in Figure 11-1.

Figure 11-1. Assembly drawing.



## 12 Bill of materials (BOM)

The BOM is provided in the .zip file that can be downloaded from [Atmel AVR application notes](#).

## 13 EVALUATION BOARD/KIT IMPORTANT NOTICE

This evaluation board/kit is intended for use for **FURTHER ENGINEERING, DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY**. It is not a finished product, and may not (yet) comply with some or any technical or legal requirements that are applicable to finished products, including, without limitation, directives regarding electromagnetic compatibility, recycling (WEEE), FCC, CE, or UL (except as may be otherwise noted on the board/kit). Atmel supplied this board/kit "AS IS," without any warranties, with all faults, at the buyer's and further users' sole risk. The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies Atmel from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge and any other technical or legal concerns.

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