

CED4204-VB Datasheet

N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
40	0.013 at $V_{GS} = 10$ V	55 ^d	19.5
	0.014 at $V_{GS} = 4.5$ V	45 ^d	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- VBmos[®] Trench Cell
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

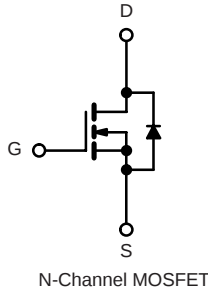
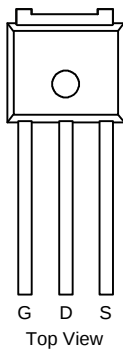


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power Supply
 - Secondary Synchronous Rectification
- DC/DC Converter

TO-251



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$ 55 ^d	A
		$T_C = 70^\circ\text{C}$ 45 ^d	
Pulsed Drain Current	I_{DM}	165	
Avalanche Current	I_{AS}	34	
Single Avalanche Energy ^a	E_{AS}	78	mJ
Maximum Power Dissipation ^a	P_D	$T_C = 25^\circ\text{C}$ 55.5 ^b	W
		$T_A = 25^\circ\text{C}^c$ 2.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	54	$^\circ\text{C/W}$
Junction-to-Case (Drain)	R_{thJC}	2.7	

Notes:

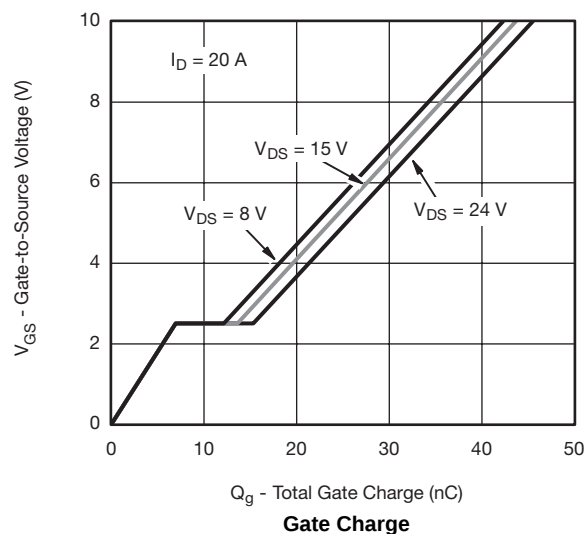
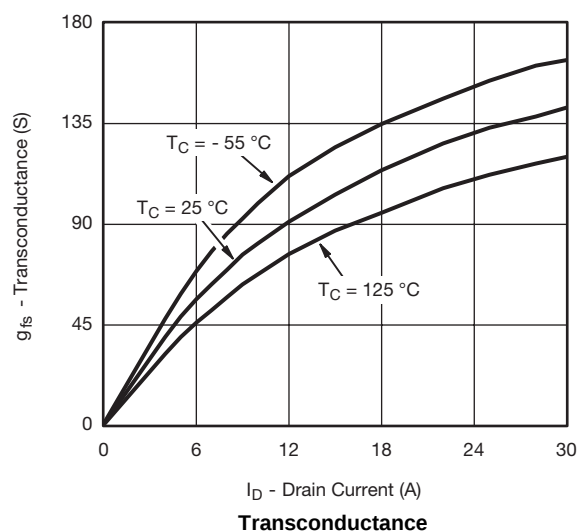
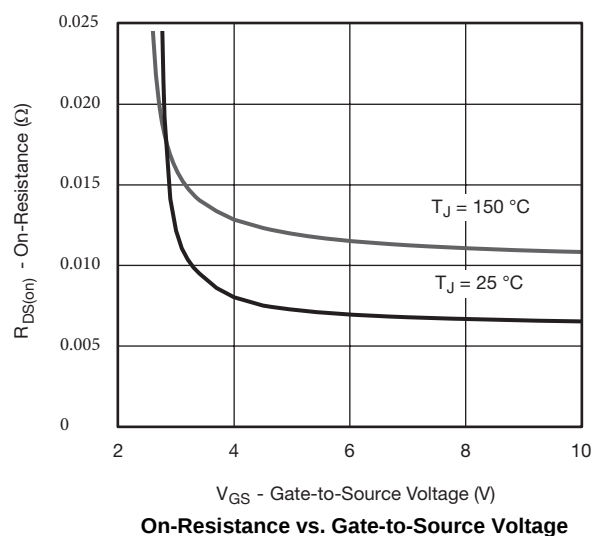
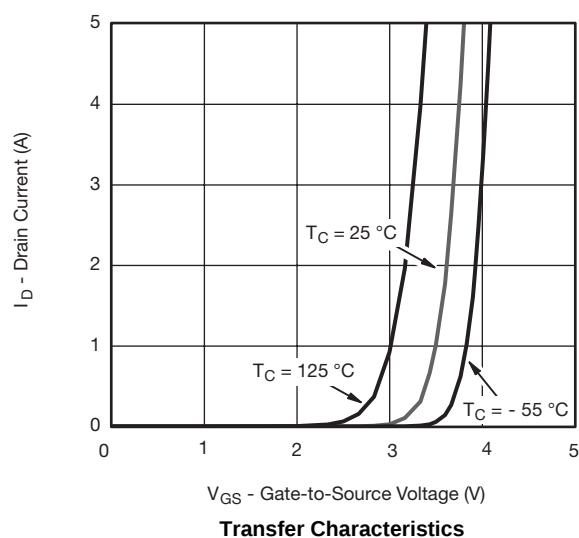
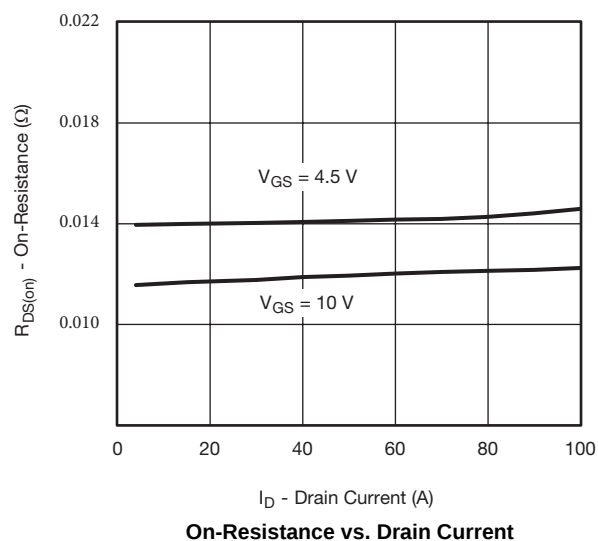
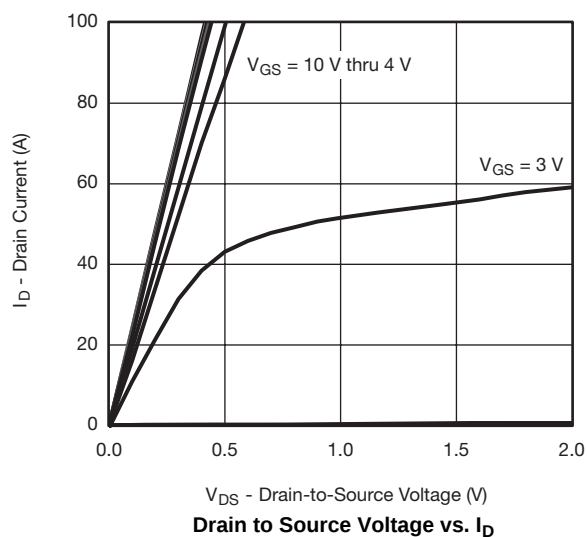
- Duty cycle $\leq 1\%$.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

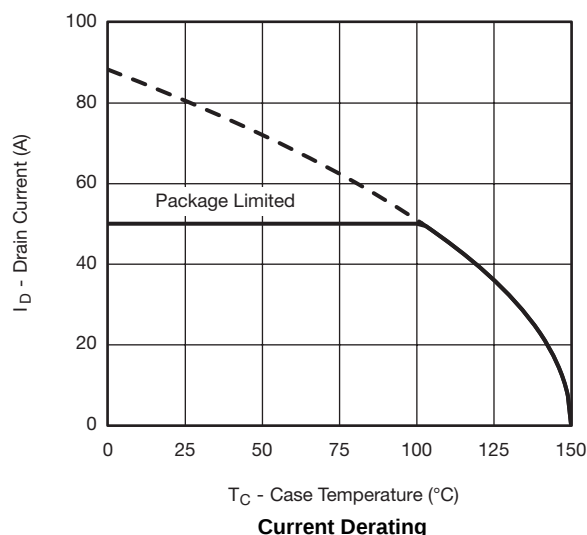
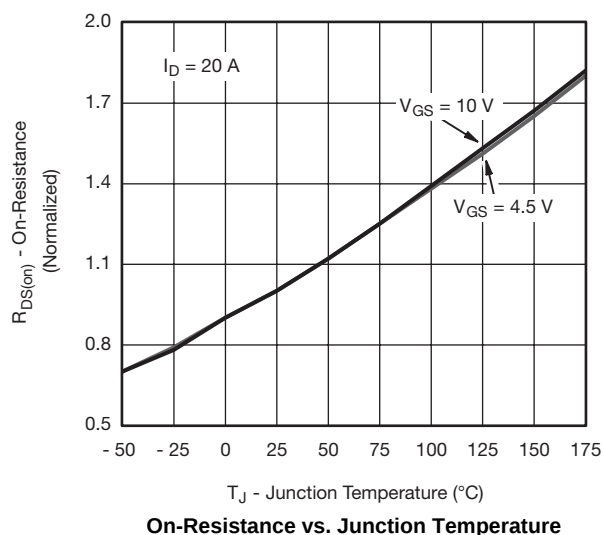
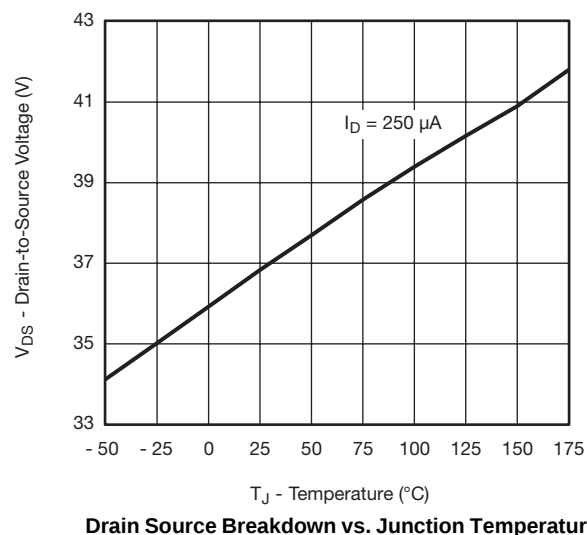
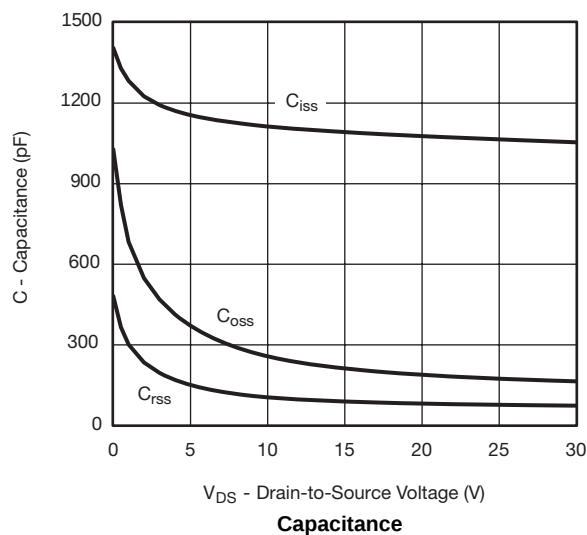
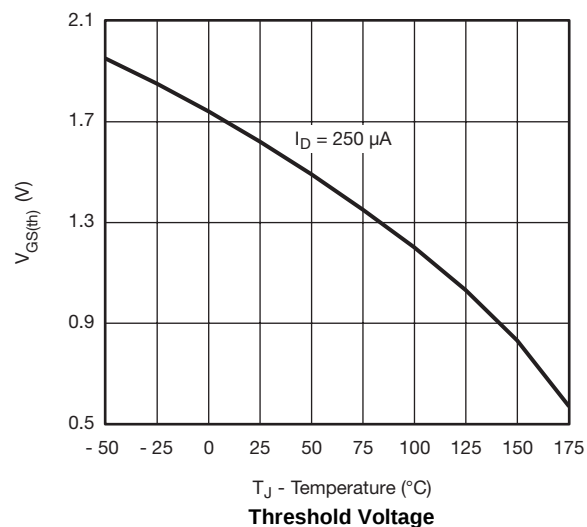
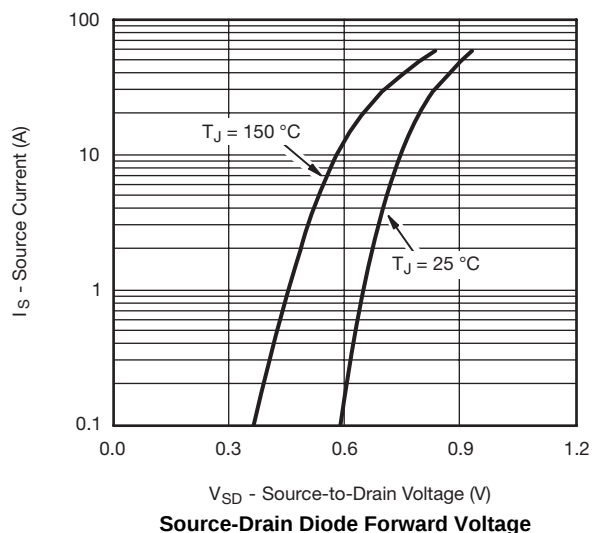
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{DS} = 0 V, I _D = 250 μA	40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0 V			1	μA
		V _{DS} = 40V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 40V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	55			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 22 A		0.013		Ω
		V _{GS} = 4.5 V, I _D = 20 A		0.014		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		100		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		1100		pF
Output Capacitance	C _{oss}			460		
Reverse Transfer Capacitance	C _{rss}			350		
Total Gate Charge ^c	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		36		nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A		25		
Gate-Source Charge ^c	Q _{gs}			6		
Gate-Drain Charge ^c	Q _{gd}			5.7		
Gate Resistance	R _g	f = 1 MHz	0.4	2	4	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		8	16	ns
Rise Time ^c	t _r			9	18	
Turn-Off Delay Time ^c	t _{d(off)}			35	53	
Fall Time ^c	t _f			9	18	
Drain-Source Body Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous Current	I _S				55	A
Pulsed Current	I _{SM}				165	
Forward Voltage ^a	V _{SD}	I _F = 10 A, V _{GS} = 0 V		0.75	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs		34	51	ns
Peak Reverse Recovery Current	I _{RM(REC)}			2	3	A
Reverse Recovery Charge	Q _{rr}			34	51	nC

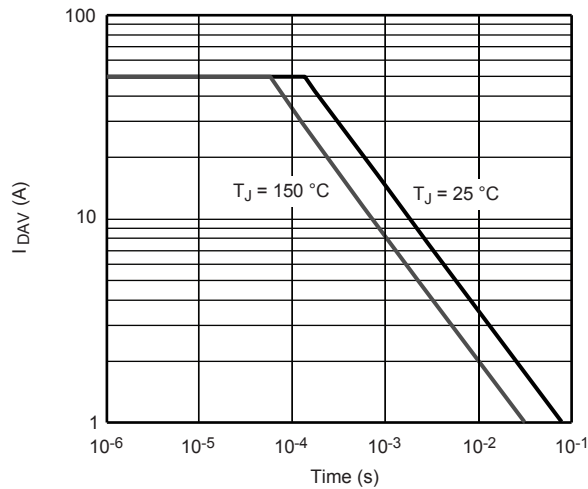
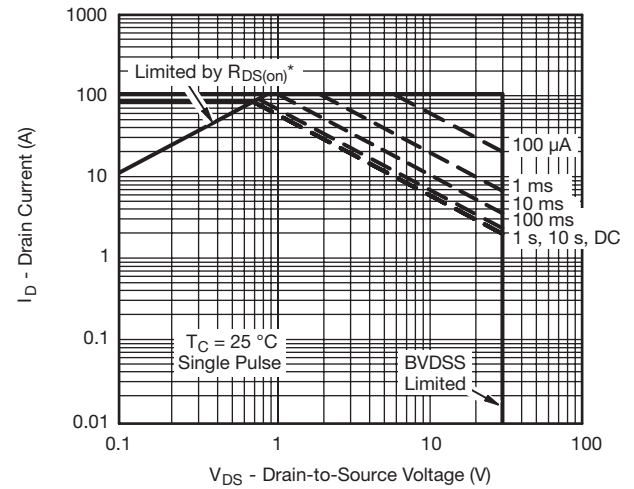
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

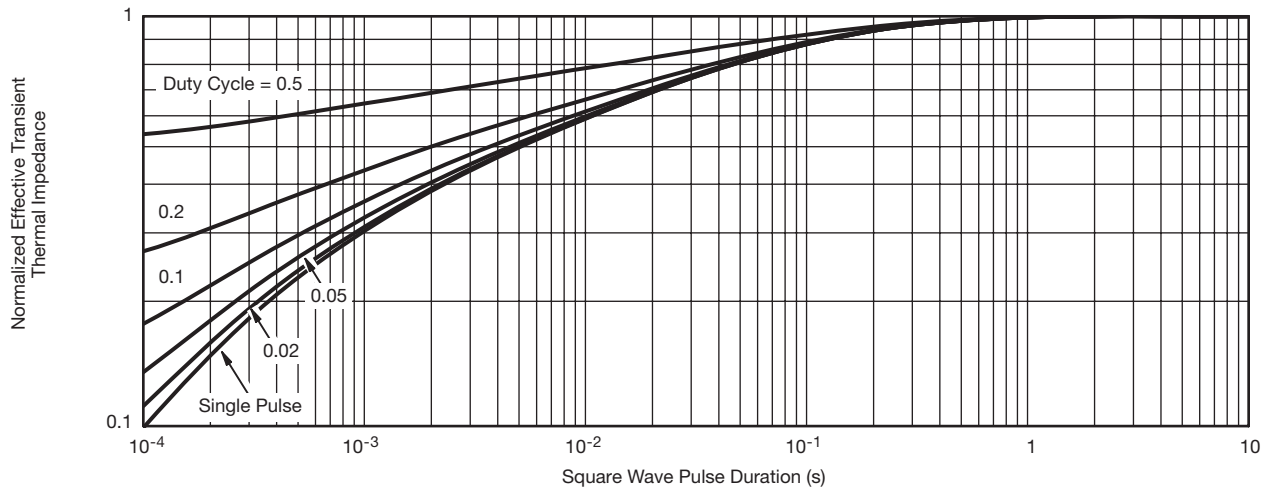
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

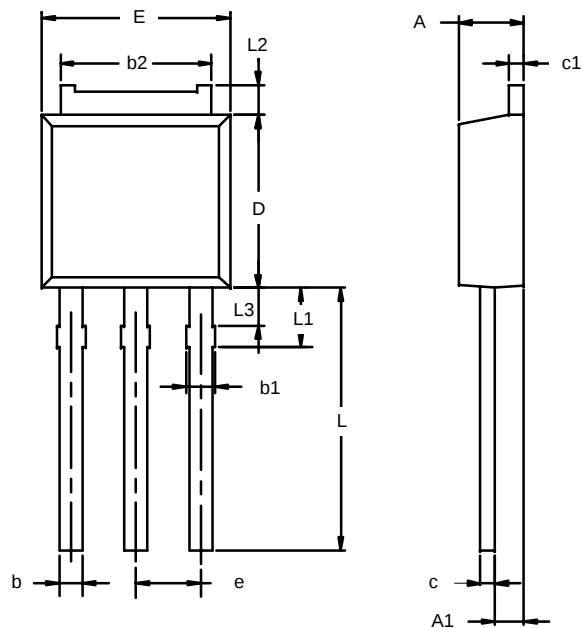
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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Single Pulse Avalanche Current Capability vs. Time


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Case

TO-251AA

Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	3.89	9.53	0.153	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				

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