BLC9H10XS-600A

Power LDMOS transistor

Rev. 1 — 10 August 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

600 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 616 MHz to 960 MHz.

Table 1. Typical performance 940 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.48 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	48	50.5	17.7	53.9	–31.4 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 2. Typical performance 880 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 50 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.4 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	869 to 894	50	50.5	18.3	52.7	–30.8 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 3. Typical performance 780 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 47 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.5 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	758 to 803	47	50.5	17.7	54.2	–33.8 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

Table 4. Typical performance 750 MHz

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 48 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.4 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	729 to 768	48	50.5	17.5	57.2	–30.8 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

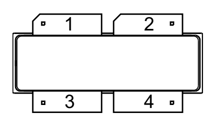
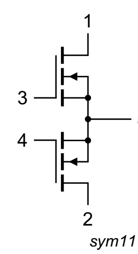
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 616 MHz to 960 MHz frequency range

2. Pinning information

Table 5. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 6. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-600A	-	plastic earless flanged cavity package; 4 leads	SOT1250-2

4. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	105	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		−6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		−6	+11	V

Table 7. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	[1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 50 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 80 °C		
		P_L = 112 W	0.236	k/W
		P_L = 141 W	0.198	k/W

6. Characteristics

Table 9. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.0 mA	105	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 150 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 47 V; I_D = 600 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	24.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	-	9.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.25 A	-	160	203	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.2 mA	105	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 47 V; I_D = 1200 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	49.0	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15.0 A	-	19.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.5 A	-	80	107	mΩ

Table 10. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 760.5 MHz; f_2 = 800.5 MHz; RF performance at V_{DS} = 47 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 758 MHz to 803 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 112 W	16.3	17.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 112 W	-	−16	−10	dB
η_D	drain efficiency	$P_{L(AV)}$ = 112 W	48	53	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 112 W	-	−31	−26	dBc

Table 11. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f = 800.5 MHz; RF performance at V_{DS} = 47 V; I_{Dq} = 600 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 758 MHz to 803 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 155 W	6.4	6.9	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 155 W	663	765	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9H10XS-600A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 52 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.48 V; f = 758 MHz; P_L = 189 W (5 dB OBO); pulsed CW (t_p = 100 μs; δ = 10 %).

7.2 Impedance information

Table 12. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 750 mA (main); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	6.5 − j2.3	2.6 + j0.1	354.1	66.7	18.8
698	4.1 − j2.5	2.1 + j0.4	314.3	59.7	19.4
720	3.9 − j2.9	2.1 + j0.3	302.9	58.5	19.4
746	3.7 − j3.3	2.1 + j0.3	346.9	66.0	19.5
757	3.7 − j3.6	2.1 + j0.0	358.3	68.8	19.1
769	3.6 − j3.8	2.2 + j0.1	363.3	69.7	19.6
790	3.7 − j4.2	1.9 + j0.2	357.5	68.9	19.6
805	3.8 − j4.5	1.9 + j0.1	347.1	65.1	19.3
820	3.8 − j4.7	2.0 + j0.2	364.4	70.4	19.8
869	4.4 − j5.7	1.8 − j0.1	365.9	69.3	19.3

Table 12. Typical impedance of main device *...continued*

Measured load-pull data of main device; I_{Dq} = 750 mA (main); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
880	4.5 – j5.9	1.9 + j0.0	361.4	72.8	19.9
894	4.8 – j6.2	2.1 – j0.1	356.3	72.2	20.0
925	5.7 – j6.8	1.9 – j0.6	349.6	64.0	18.8
960	7.1 – j7.0	1.6 – j0.4	350.0	67.4	19.0
1000	8.9 – j6.6	1.9 – j0.2	336.1	71.3	19.5
Maximum drain efficiency load					
600	6.4 – j2.0	2.5 + j1.9	239.5	79.6	21.0
698	4.1 – j2.3	2.0 + j1.4	253.3	65.9	20.8
720	3.7 – j2.7	1.8 + j1.7	227.9	72.5	21.2
746	3.6 – j3.2	1.9 + j1.4	248.0	78.6	21.0
757	3.5 – j3.4	1.9 + j1.4	243.3	78.7	21.0
769	3.5 – j3.7	2.1 + j0.9	282.8	79.6	20.8
790	3.5 – j4.1	2.4 + j1.8	218.6	80.6	22.2
805	3.7 – j4.3	2.0 + j1.8	232.0	76.0	22.3
820	3.6 – j4.6	2.1 + j1.2	289.5	78.8	21.7
869	4.1 – j5.3	1.6 + j1.5	218.5	80.0	22.6
880	4.3 – j5.6	1.6 + j1.3	224.5	79.7	22.8
894	4.5 – j5.9	1.5 + j1.1	247.5	79.4	22.0
925	5.3 – j6.4	1.7 + j1.2	221.6	79.8	22.5
960	6.6 – j6.5	1.1 + j1.0	186.1	78.8	22.6
1000	8.6 – j6.0	1.2 + j0.7	214.8	77.3	21.9

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 13. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1400 mA (peak); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	3.3 – j1.3	1.2 + j0.0	682.7	67.7	18.2
698	2.1 – j1.4	1.2 + j0.1	693.3	69.7	19.2
720	2.1 – j1.6	1.1 + j0.1	696.9	69.8	19.2
746	2.0 – j1.8	1.2 + j0.0	688.2	68.2	19.1
757	2.0 – j1.8	1.2 + j0.0	680.6	70.3	19.3
769	1.8 – j1.9	1.2 + j0.0	673.6	70.5	19.8
790	1.9 – j2.2	1.0 + j0.0	665.5	69.6	19.7
805	2.0 – j2.4	0.9 + j0.0	670.5	70.3	19.3
820	1.9 – j2.4	0.9 + j0.0	688.1	71.5	19.5

Table 13. Typical impedance of peak device *…continued*

Measured load-pull data of peak device; I_{Dq} = 1400 mA (peak); V_{DS} = 50 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
869	2.2 – j2.7	1.1 – j0.5	670.7	64.0	18.8
880	2.2 – j2.8	1.1 – j0.5	668.4	65.3	19.1
894	2.3 – j3.0	1.1 – j0.5	671.2	66.8	19.2
925	2.7 – j3.1	1.0 – j0.4	664.5	68.6	19.4
960	3.3 – j3.2	1.0 – j0.4	648.7	69.2	19.5
1000	4.0 – j2.9	1.0 – j0.5	623.2	67.2	19.5
Maximum drain efficiency load					
600	3.2 – j1.2	1.2 + j1.1	439.5	81.3	20.8
698	2.1 – j1.4	1.1 + j1.2	403.3	80.6	22.1
720	2.0 – j1.5	1.1 + j1.2	408.6	81.5	22.1
746	1.9 – j1.7	1.1 + j1.0	439.3	80.7	21.8
757	1.9 – j1.9	1.1 + j0.9	452.9	79.7	21.7
769	1.9 – j2.0	0.9 + j1.0	397.5	80.0	22.6
790	1.8 – j2.2	0.9 + j0.9	408.1	78.2	22.5
805	1.9 – j2.1	0.9 + j0.6	485.2	79.6	21.2
820	1.8 – j2.2	0.8 + j0.8	387.7	82.8	22.7
869	2.0 – j2.5	0.7 + j0.6	374.6	83.1	22.5
880	1.9 – j2.5	0.7 + j0.6	351.5	82.5	23.2
894	2.0 – j2.7	0.7 + j0.4	378.6	82.9	22.7
925	1.9 – j2.8	0.7 + j0.4	365.8	81.5	23.0
960	2.5 – j2.9	0.7 + j0.2	395.0	79.3	22.6
1000	3.0 – j2.8	0.7 + j0.3	361.3	76.0	23.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

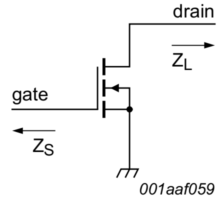
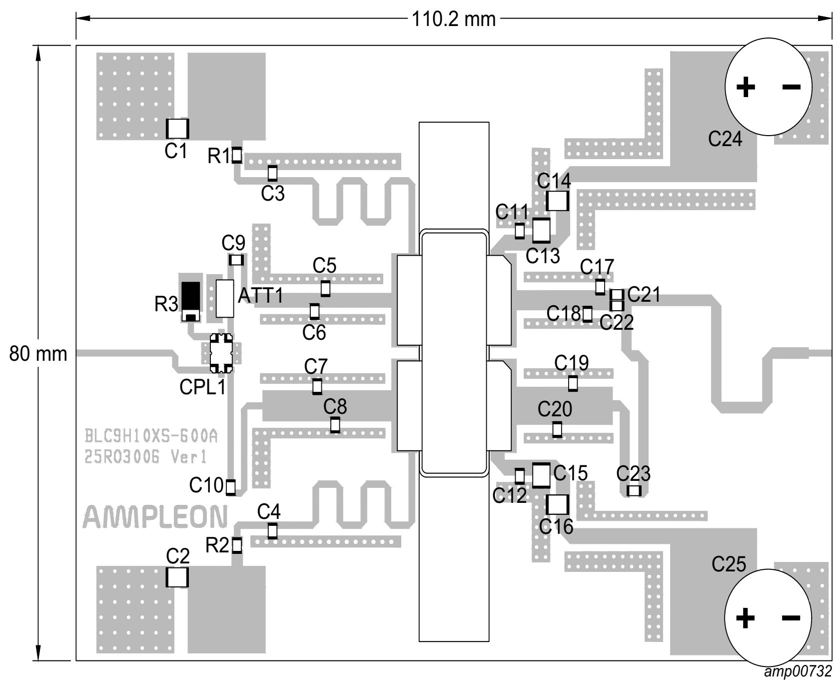


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm. See Table 14 for a list of components.

Fig 2. Component layout

Table 14. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: Hi-Q SMD 1210, GRM32ER71H475KA88L
C3, C4, C9, C10, C11, C12, C23	multilayer ceramic chip capacitor	68 pF	Murata: Hi-Q SMD 0805
C5	multilayer ceramic chip capacitor	8.2 pF	Murata: Hi-Q SMD 0805
C6	multilayer ceramic chip capacitor	3.9 pF	Murata: Hi-Q SMD 0805
C7	multilayer ceramic chip capacitor	8.2 pF	Murata: Hi-Q SMD 0805
C8	multilayer ceramic chip capacitor	7.5 pF	Murata: Hi-Q SMD 0805
C13, C14, C15, C16	multilayer ceramic chip capacitor	4.7 μF, 100 V	Murata: Hi-Q SMD 1210, GRM42-256X7S475K100H530
C17	multilayer ceramic chip capacitor	9.1 pF	Murata: Hi-Q SMD 0805
C18	multilayer ceramic chip capacitor	2 pF	Murata: Hi-Q SMD 0805
C19	multilayer ceramic chip capacitor	12 pF	Murata: Hi-Q SMD 0805
C20	multilayer ceramic chip capacitor	12 pF	Murata: Hi-Q SMD 0805
C21, C22	multilayer ceramic chip capacitor	8.2 pF	Murata: Hi-Q SMD 0805
C24, C25	electrolytic capacitor	470 μF, 63 V	
R1, R2	resistor	4.7 Ω, 1 %	SMD 0805

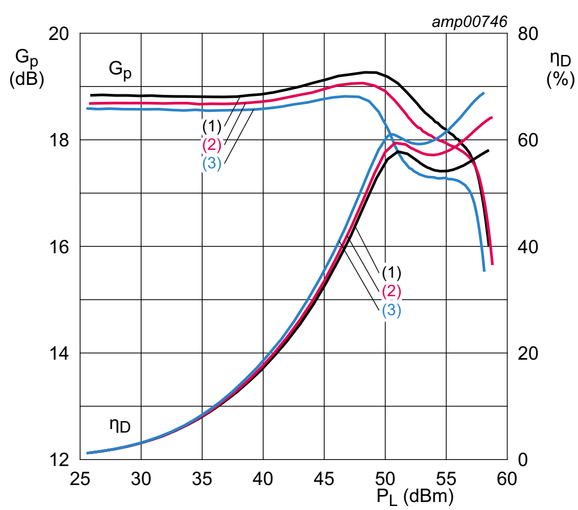
Table 14. List of components *...continued*

See Figure 2 for component layout.

Component	Description	Value	Remarks
R3	resistor	50 Ω, 25 W	Anaren: C16A50Z4
ATT1	attenuator	1 dB, 10 W	Anaren: D10AA1Z4
CPL1	hybrid coupler	2 dB; 90°	Anaren: X3C07F1-02S

7.4 Graphical data

7.4.1 Pulsed CW



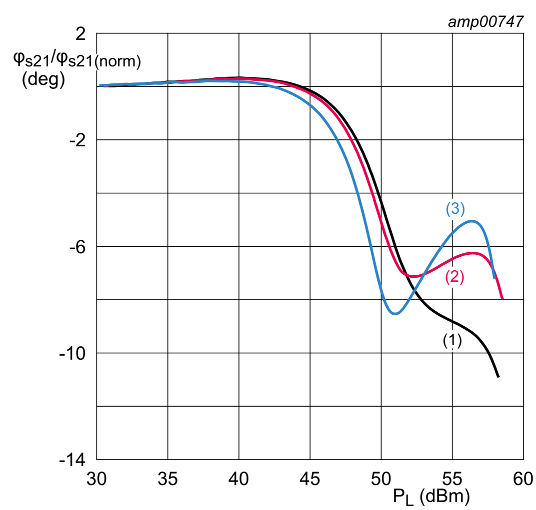
V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V; t_p = 100 μs; δ = 10 %.

(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V; t_p = 100 μs; δ = 10 %.

(1) f = 758 MHz

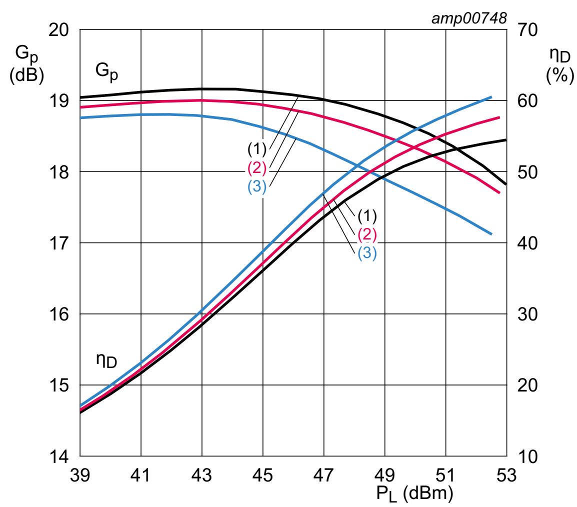
(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 4. Normalized phase response (AM to PM) as a function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping); PAR = 9.9 dB per carrier at 0.01 % probability on CCDF per carrier.



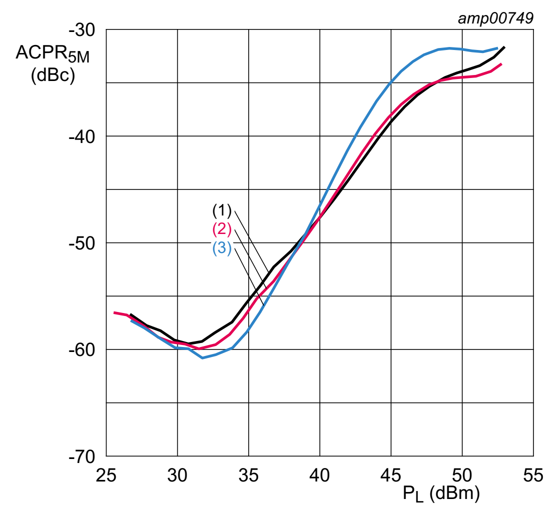
V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



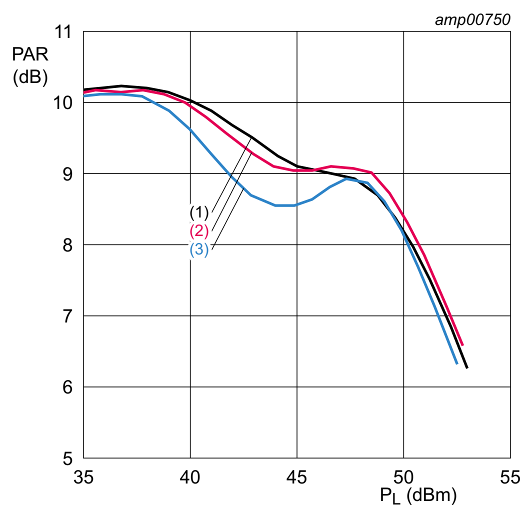
V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 758 MHz

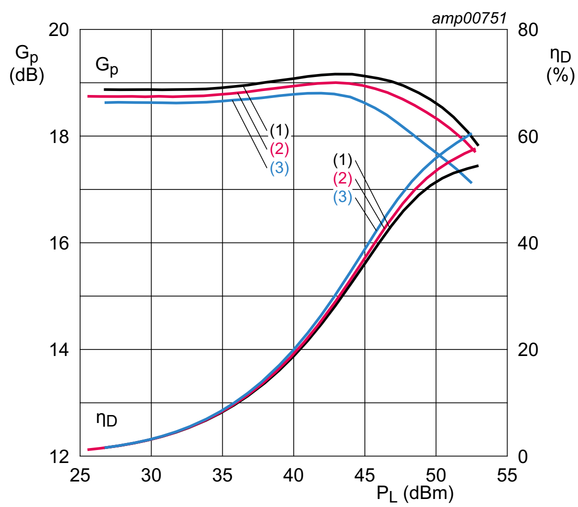
(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (46 % clipping); PAR = 9.9 dB per carrier at 0.01 % probability on CCDF per carrier.



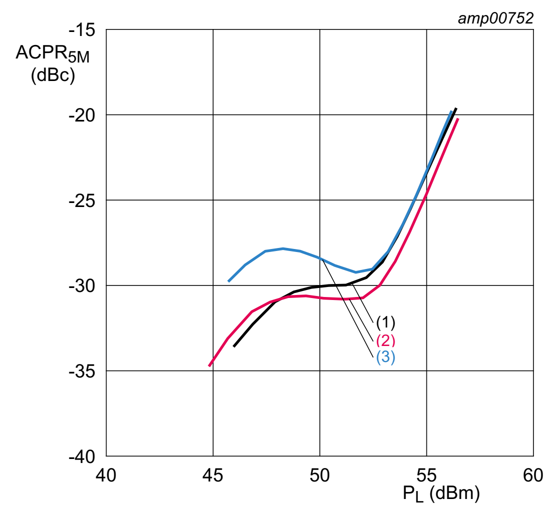
V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

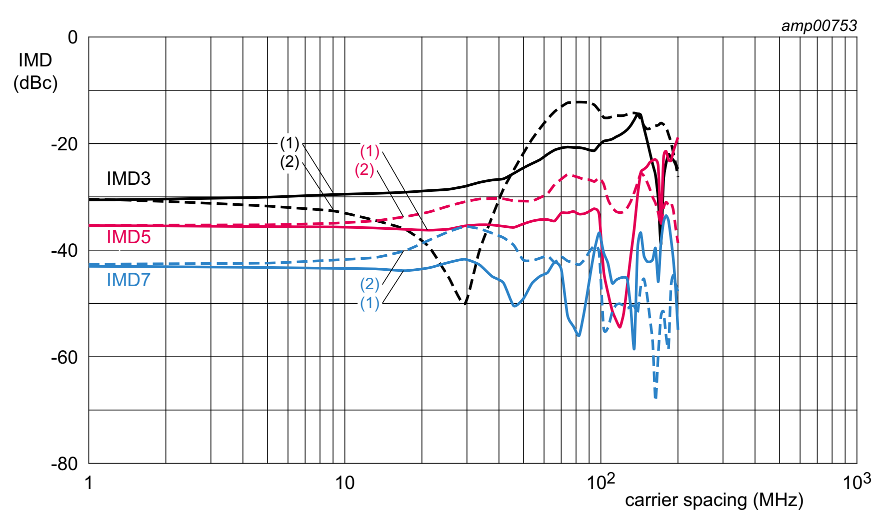
(1) f = 758 MHz

(2) f = 780.5 MHz

(3) f = 803 MHz

Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.4.4 2-Tone VBW



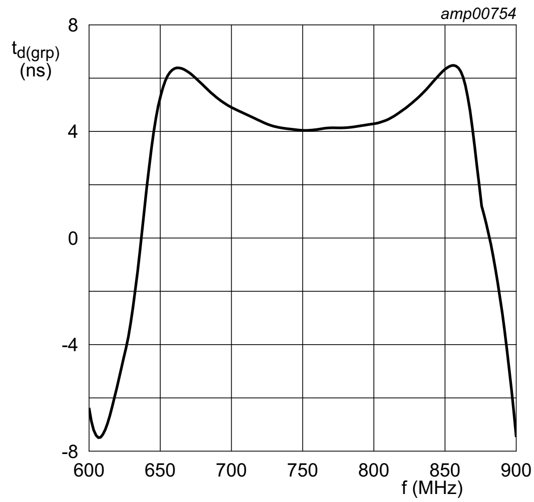
V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

(1) IMD low

(2) IMD high

Fig 10. VBW capability

7.4.5 Group delay

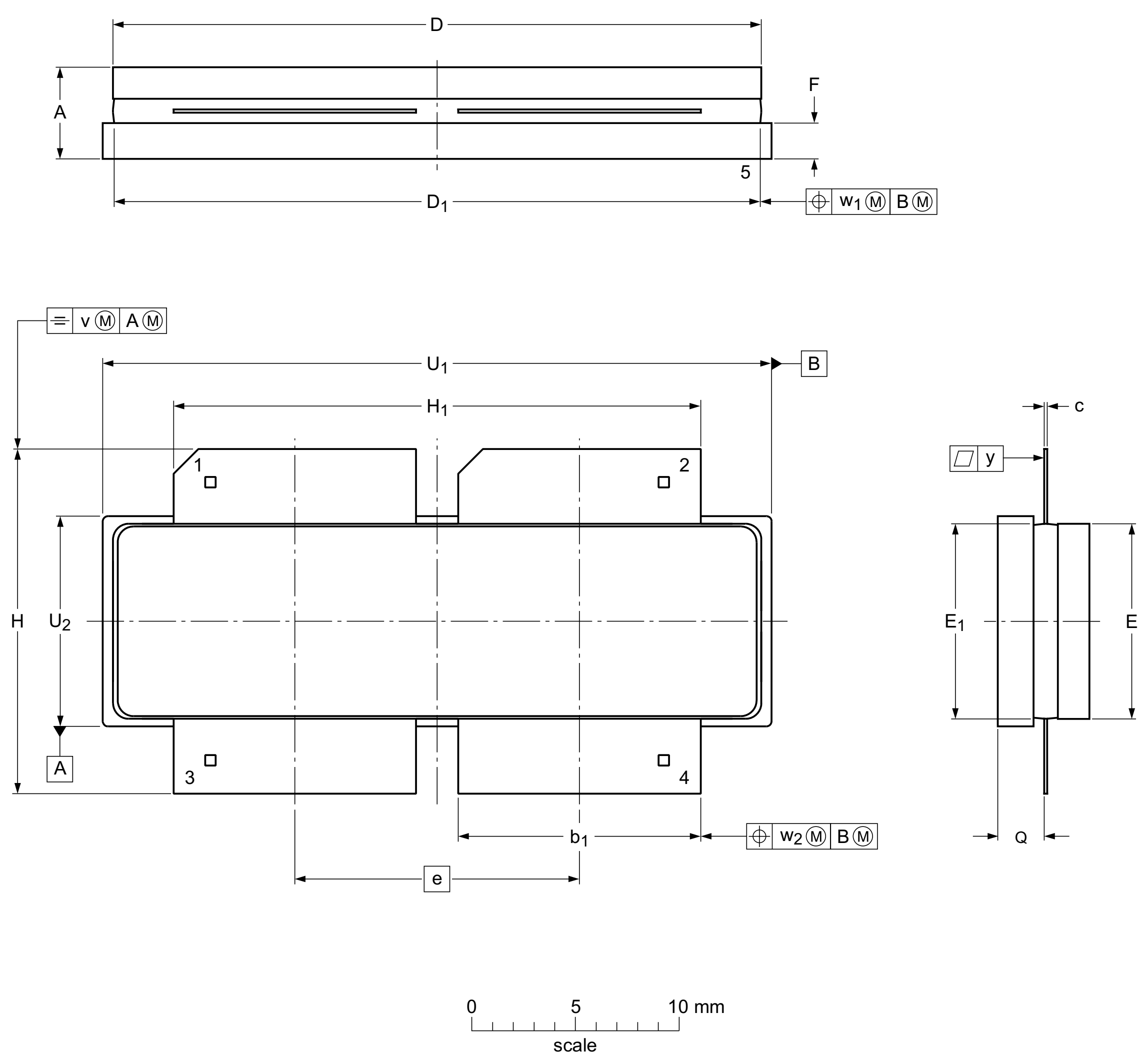


V_{DS} = 48 V; I_{Dq} = 600 mA; $V_{GS(amp)peak}$ = 0.5 V.

Fig 11. Group delay time as a function of frequency; typical values

8. Package outline

Plastic earless flanged cavity package; 4 leads **SOT1250-2**



Dimensions

Unit		A	b_1	c	D	D_1	E	E_1	e	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2	y
mm	max	4.52	11.79	0.18	31.44	31.34	9.60	9.50		1.73	16.71	25.50	2.25	32.33	10.23	0.50	0.50	0.50	0.10
	nom								13.72										
	min	4.12	11.58	0.13	31.04	31.14	9.20	9.30		1.53	16.51	25.30	2.03	32.13	10.03				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1250-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1250-2						17-01-13

Fig 12. Package outline SOT1250-2

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 15. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of ≥ 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 16. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PM	Phase Modulation
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-600A v.1	20180810	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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