BLC10G18XS-552AVT

Power LDMOS transistor

AMPLEON

Rev. 1 — 31 October 2019

Product data sheet

1. Product profile

1.1 General description

550 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 1880 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 30 V; I_{Dq} = 950 mA (main); $V_{GS(amp)peak}$ = 1.1 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	30	49.5	16.8	48.3	–32.1 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

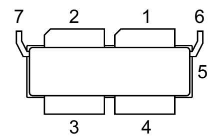
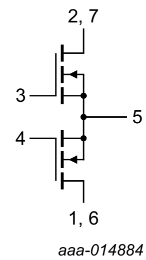
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1880 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G18XS-552AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 30 V; I_{Dq} = 950 mA (main); $V_{GS(amp)peak}$ = 1.03 V; T_{case} = 80 °C		
		P_L = 115 W	0.21	K/W
		P_L = 145 W	0.19	K/W

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6. Characteristics

Table 6. DC characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 950 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 30 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	34	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9.0 A	-	20.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 6.3 A	-	72	108	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 380 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 1900 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 30 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	57	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 19.0 A	-	39	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 13.3 A	-	37	62	mΩ

Table 7. RF characteristics
Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1807.5 MHz; f_2 = 1877.5 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 950 mA (main); $V_{GS(amp)peak}$ = 1.13 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 115 W	15.1	16.1	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 115 W	-	–13	–8	dB
η_D	drain efficiency	$P_{L(AV)}$ = 115 W	44	48	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 115 W	-	–33	–28	dBc

Table 8. RF characteristics
Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f = 1877.5 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 950 mA (main); $V_{GS(amp)peak}$ = 1.13 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 148 W	6.3	6.8	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 148 W	620	705	-	W

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7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G18XS-552AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.15 V; f = 1805 MHz; P_L = 235 W (5 dB OBO); 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 1 A (main); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1810	2.6 – j6.6	1.8 – j3.1	285.36	61.99	16.39
1845	3.5 – j7.3	1.5 – j3.1	286.73	59.31	16.25
1880	4.6 – j7.8	1.6 – j3.2	281.16	60.32	16.41
Maximum drain efficiency load					
1810	2.6 – j6.6	3.2 – j2.2	203.39	68.8	18.26
1845	3.5 – j7.3	3.0 – j1.5	180.88	68.43	18.81
1880	4.6 – j7.8	2.7 – j2.0	199.61	68.01	18.48

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1.9 A (peak); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1810	2.2 – j4.5	1.5 – j2.9	550.81	59.45	16.7
1845	3.3 – j4.0	1.5 – j2.9	541	59.25	17.05
1880	4.0 – j3.5	1.6 – j2.8	529.9	60.76	17.6
Maximum drain efficiency load					
1810	2.2 – j4.5	2.1 – j1.6	393.5	67.11	18.76
1845	3.3 – j4.0	1.5 – j1.6	366.31	65.83	19.35
1880	4.0 – j3.5	1.5 – j1.7	372.09	65.86	19.54

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

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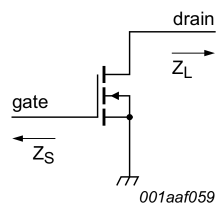
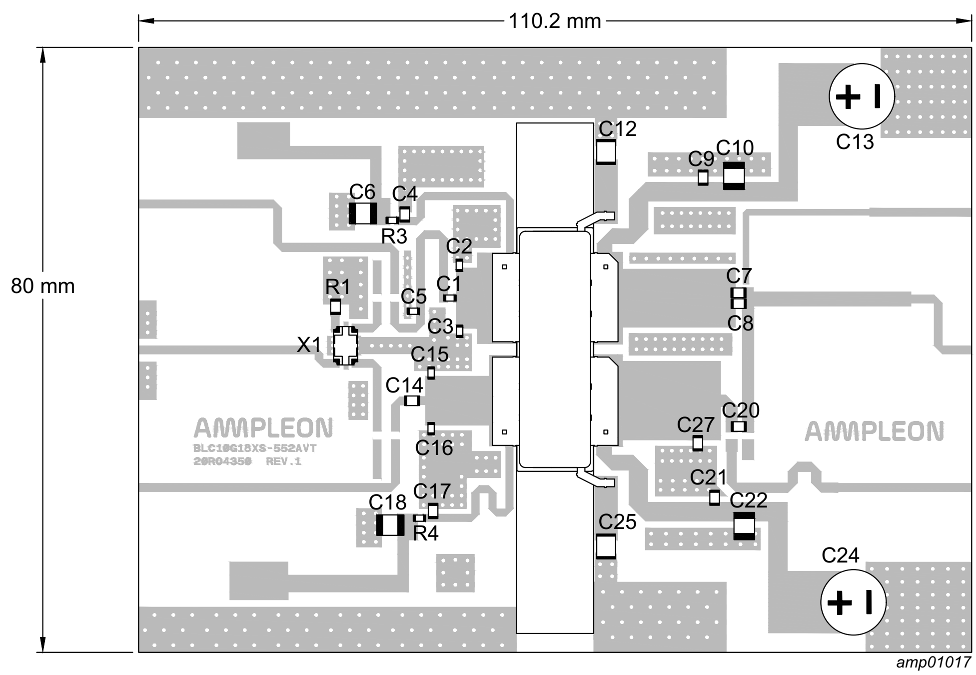


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 11 for a list of components.

Fig 2. Component layout

Table 11. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	1.8 pF	GQM18
C2, C3	multilayer ceramic chip capacitor	1.0 pF	GQM18
C4, C9, C14, C17, C21	multilayer ceramic chip capacitor	18 pF	GQM21
C5	multilayer ceramic chip capacitor	1.8 pF	GQM21
C6, C10, C12, C18, C22, C25	electrolytic capacitor	4.7 μF, 50 V	Murata: X7R
C7, C8	multilayer ceramic chip capacitor	8.2 pF	GQM21
C11, C19, C23, C26	multilayer ceramic chip capacitor		not mounted

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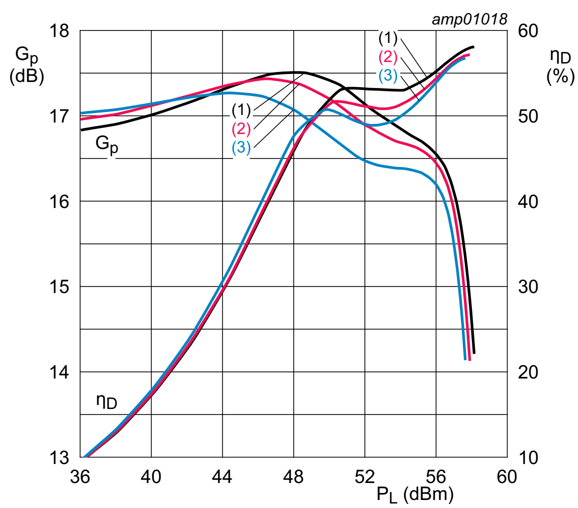
Table 11. List of components *...continued*

See Figure 2 for component layout.

Component	Description	Value	Remarks
C13, C24	multilayer ceramic chip capacitor	470 μF, 63 V	Elco
C15, C16	multilayer ceramic chip capacitor	1.8 pF	GQM21
C20	multilayer ceramic chip capacitor	10 pF	GQM21
C27	multilayer ceramic chip capacitor	0.4 pF	GQM21
R1	resistor	50 Ω	Anaren: C16A50Z4
R2	resistor		not mounted
R3, R4	resistor	5.1 Ω	
X1	hybrid coupler		Anaren: X3C20F1-02S

7.4 Graphical data

7.4.1 Pulsed CW



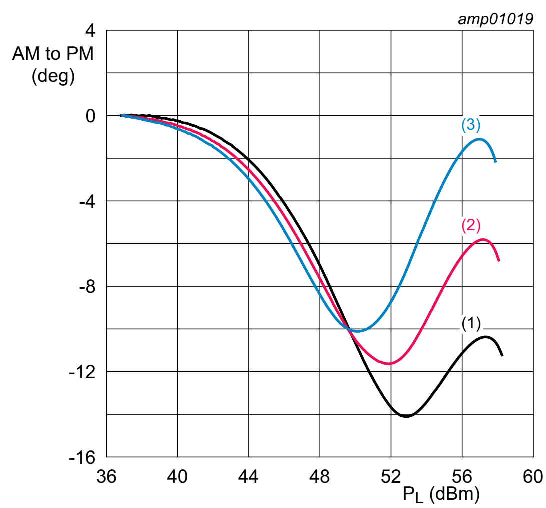
V_{DS} = 30 V; I_{Dq} = 950 mA; $V_{GS(amp)peak}$ = 1.10 V; t_p = 100 μs; δ = 10 %.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 950 mA; $V_{GS(amp)peak}$ = 1.10 V; t_p = 100 μs; δ = 10 %.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

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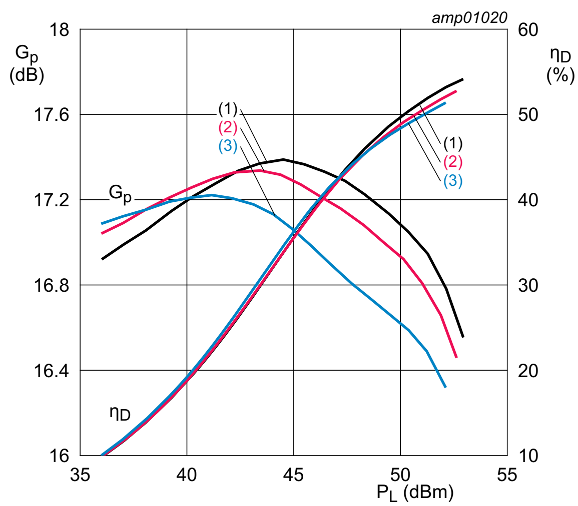
7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.



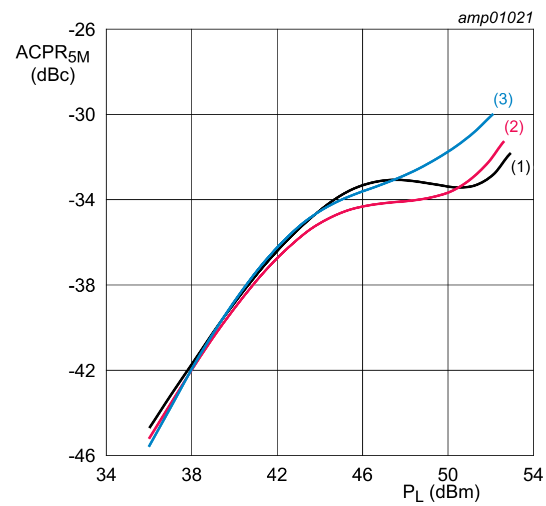
V_{DS} = 30 V; I_{Dq} = 950 mA; $V_{GS(amp)peak}$ = 1.10 V.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



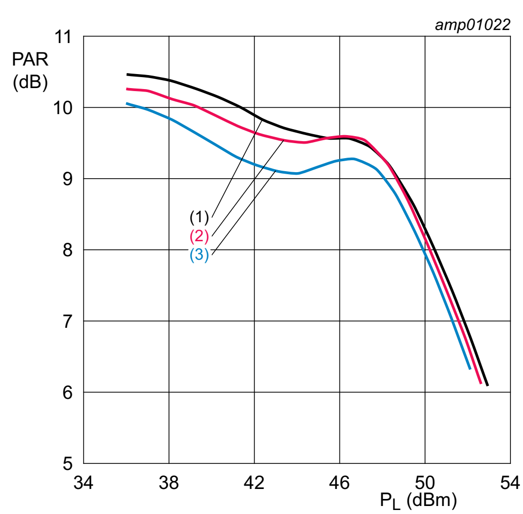
V_{DS} = 30 V; I_{Dq} = 950 mA; $V_{GS(amp)peak}$ = 1.10 V.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 950 mA; $V_{GS(amp)peak}$ = 1.10 V.

(1) f = 1805 MHz

(2) f = 1845 MHz

(3) f = 1880 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

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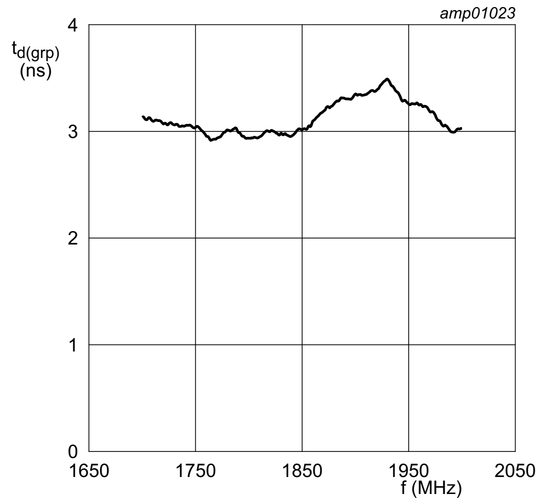
7.4.3 Group delay



V_{DS} = 30 V; I_{Dq} = 950 mA; $V_{GS(amp)peak}$ = 1.10 V.

Fig 8. Group delay time as a function of frequency; typical values

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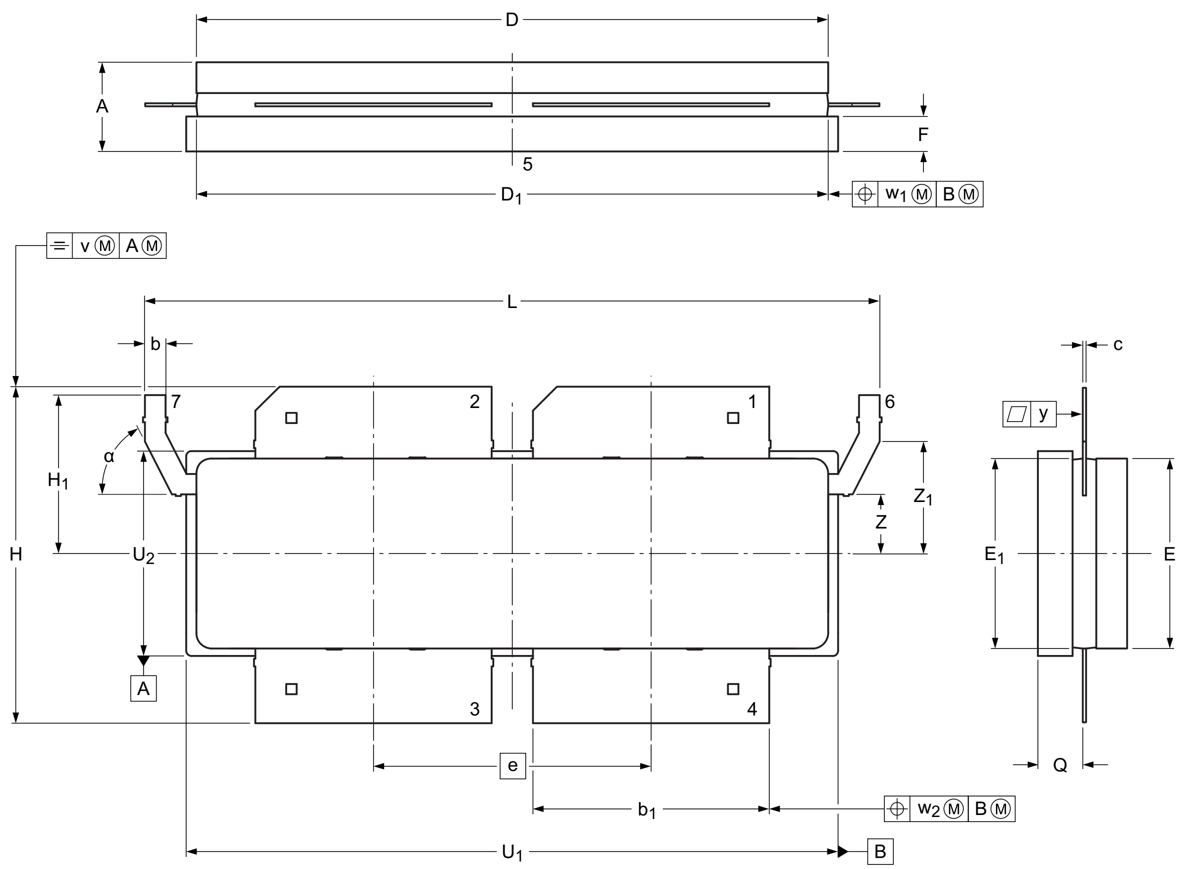
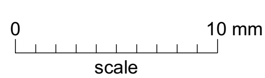
8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-4**



y	α	Z	Z_1
0.1	65°	3.17	5.79
	61°	2.67	5.29



Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
	max	4.52	1.12	11.78	0.18	31.44	31.34	9.60	9.50		36.42	1.73	16.71	8.12	2.25	32.33	10.23	0.5	0.5	0.5
mm	nom									13.72										
	min	4.12	0.91	11.58	0.13	31.04	31.14	9.20	9.30		36.22	1.53	16.51	7.62	2.03	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-4						17-08-31

Fig 9. Package outline SOT1258-4

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9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G18XS-552AVT v.1	20191031	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

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For more information, please visit: **http://www.ampleon.com**

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