

BLC9H10XS-505A

Power LDMOS transistor

Rev. 1 — 6 March 2020

AMPLEON

Product data sheet

1. Product profile

1.1 General description

500 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 617 MHz to 960 MHz.

Table 1. Typical performance 800 MHz

Typical RF performance at $T_{case} = 25\text{ °C}$ in an asymmetrical Doherty test circuit. $V_{DS} = 48\text{ V}$; $I_{DQ} = 500\text{ mA}$ (main); $V_{GS(amp)peak} = 0.5\text{ V}$; unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	791 to 821	48	49.3	18.6	52	-36 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

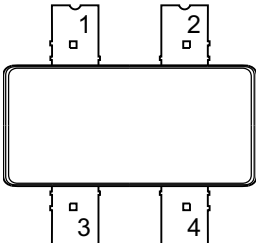
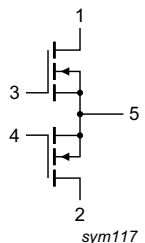
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internal integrated wideband input matching for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 617 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source ^[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-505A	-	air cavity plastic earless flanged package; 4 leads	SOT1273-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+11	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	^[1]	-	225	°C
T_{case}	case temperature	operating ^[1]	-40	+150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 48 \text{ V}$; $I_{Dq} = 500 \text{ mA}$; $V_{GS(peak)} = 0.65 \text{ V}$; $T_{case} = 80 \text{ °C}$		
		$P_L = 81 \text{ W}$	0.346	K/W
		$P_L = 100 \text{ W}$	0.327	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.5\text{ mA}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 150\text{ mA}$	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 48\text{ V}; I_D = 500\text{ mA}$	1.7	2.0	2.7	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	24.3	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.5\text{ A}$	-	10	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5.25\text{ A}$	-	154	203	$\text{m}\Omega$
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 48\text{ V}; I_D = 800\text{ mA}$	1.7	2.0	2.7	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	35.5	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 11\text{ A}$	-	14.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	113	142	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; $f_1 = 793.5\text{ MHz}$; $f_2 = 818.5\text{ MHz}$; RF performance at $V_{DS} = 48\text{ V}$; $I_{Dq} = 400\text{ mA}$ (main); $V_{GS(amp)peak} = 0.5\text{ V}$; $T_{case} = 25\text{ °C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 791 MHz to 821 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 85\text{ W}$	16.8	18.2	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 85\text{ W}$	-	-17	-13	dB
η_D	drain efficiency	$P_{L(AV)} = 85\text{ W}$	46	50	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 85\text{ W}$	-	-33	-28	dBc

Table 8. RF characteristics

Test signal: CW; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ %}$; $f_1 = 791\text{ MHz}$; $f_2 = 821\text{ MHz}$; RF performance at $V_{DS} = 48\text{ V}$; $I_{Dq} = 400\text{ mA}$; $V_{GS(amp)peak} = 0.6\text{ V}$ (typical); $T_{case} = 25\text{ °C}$; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB compression	-	485	500	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9H10XS-505A is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 48 \text{ V}$; $I_{DQ} = 400 \text{ mA}$; $V_{GS(amp)peak} = 0.6 \text{ V}$; $f = 791 \text{ MHz}$; $P_L = 160 \text{ W}$ (5 dB OBO); W-CDMA.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{DQ} = 900 \text{ mA}$ (main); $V_{DS} = 48 \text{ V}$; pulsed CW ($t_p = 100 \mu\text{s}$; $\delta = 10 \%$).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
780	$3.8 - j3.4$	$1.5 - j0.3$	330	65.0	19.3
820	$4.2 - j4.2$	$1.7 - j0.5$	337	66.4	19.1
860	$4.9 - j4.9$	$1.6 - j0.7$	334	65.2	18.8
Maximum drain efficiency load					
780	$3.8 - j3.4$	$1.5 + j1.0$	198	74.6	22.2
820	$4.2 - j4.2$	$1.3 + j0.6$	231	75.7	21.2
860	$4.9 - j4.9$	$1.3 + j0.4$	230	75.9	21.2

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At 3 dB gain compression.

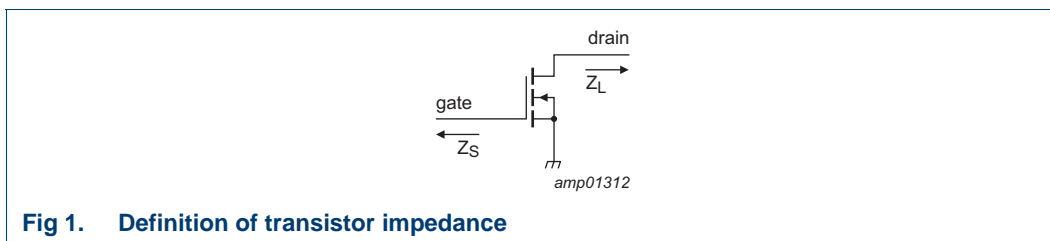
Table 10. Typical impedance of peak device

Measured load-pull data of peak device; $I_{DQ} = 1320 \text{ mA}$ (peak); $V_{DS} = 48 \text{ V}$; pulsed CW ($t_p = 100 \mu\text{s}$; $\delta = 10 \%$).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
780	$3.1 - j2.1$	$1.3 - j1.0$	451	62.4	18.4
820	$4.0 - j3.4$	$1.2 - j0.9$	451	65.6	18.4
860	$4.7 - j3.5$	$1.1 - j1.0$	458	67.3	18.3
Maximum drain efficiency load					
780	$3.1 - j2.1$	$1.1 + j0.0$	324	72.4	20.9
820	$4.0 - j3.4$	$0.9 - j0.2$	343	72.9	20.1
860	$4.7 - j3.5$	$0.9 - j0.2$	319	77.4	20.9

[1] Z_S and Z_L defined in [Figure 1](#).

[2] At 3 dB gain compression.



7.3 Test circuit

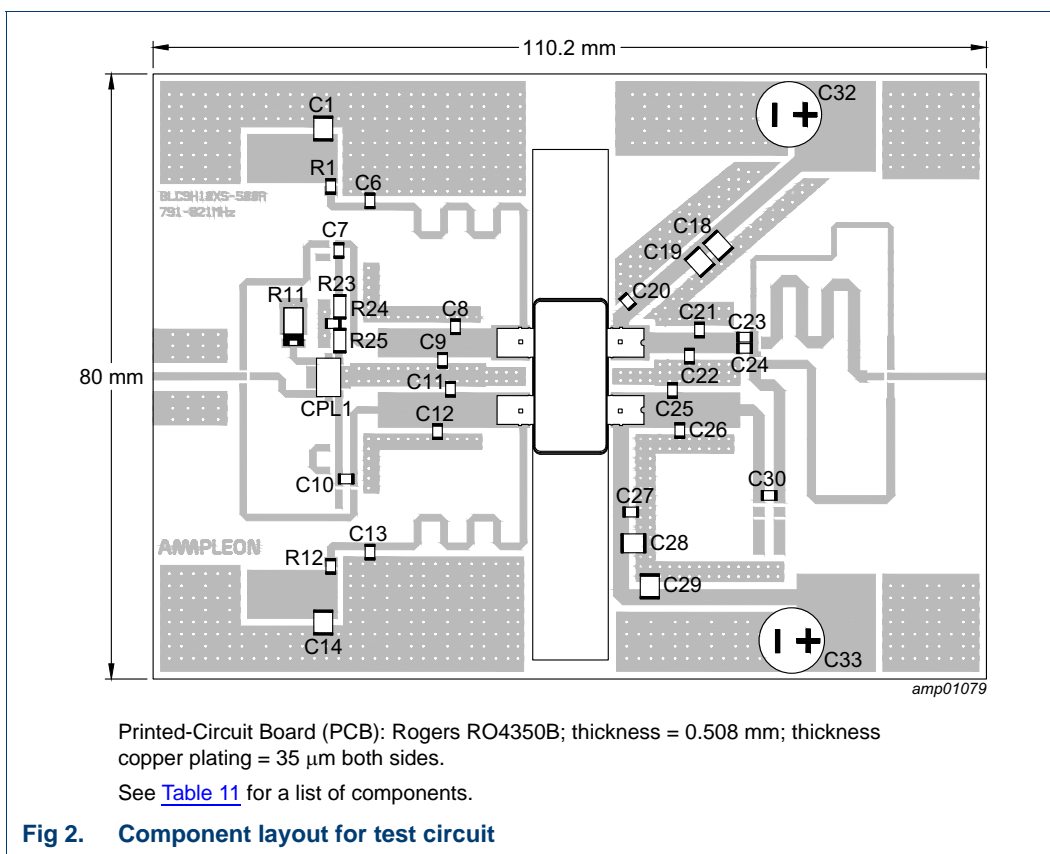


Table 11. List of components

See [Figure 2](#) for component layout.

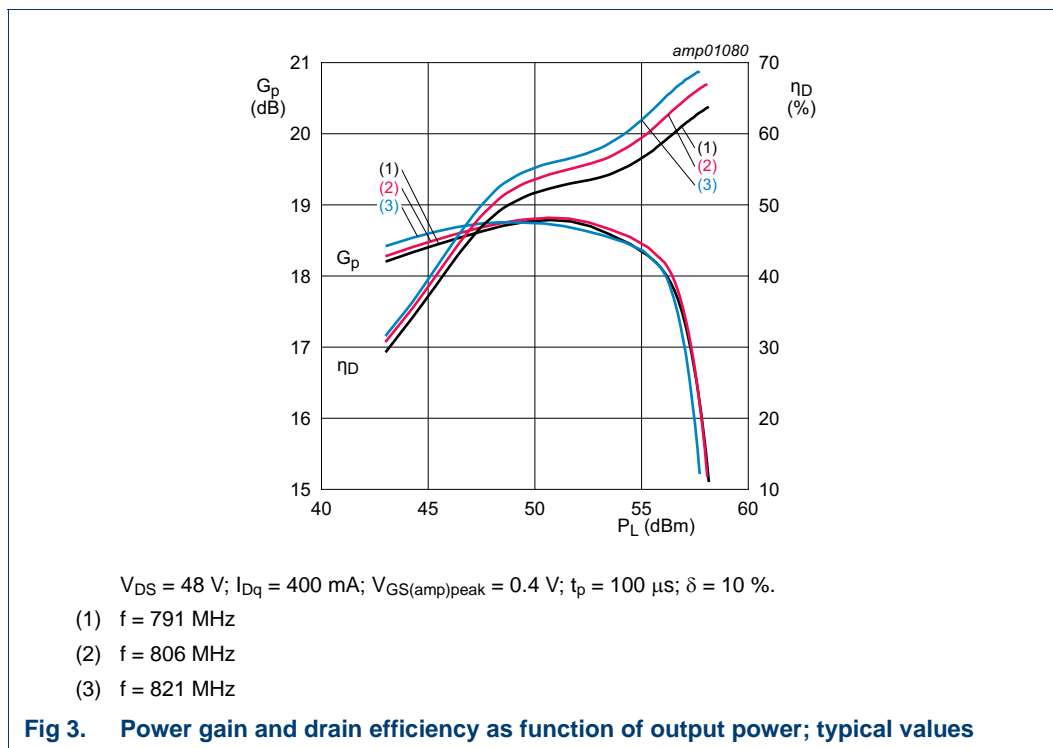
Component	Description	Value	Remarks
C1, C14	multilayer ceramic chip capacitor	4.7 μF , 50 V	Murata: GRM32ER71H475KA88L, SMD 1210
C18, C19, C28, C29	multilayer ceramic chip capacitor	4.7 μF , 100 V	Murata: GRM42-256X7S475K100H530, SMD 1210
C6, C7, C10, C13, C27, C30	multilayer ceramic chip capacitor	68 pF	Murata: Hi-Q, SMD 0805
C8, C9	multilayer ceramic chip capacitor	3.9 pF	Murata: Hi-Q, SMD 0805
C11, C12	multilayer ceramic chip capacitor	5.6 pF	Murata: Hi-Q, SMD 0805
C20	multilayer ceramic chip capacitor	39 pF	Murata: Hi-Q, SMD 0805
C21, C22	multilayer ceramic chip capacitor	8.2 pF	ATC 100B
C23, C24	multilayer ceramic chip capacitor	10 pF	Murata: Hi-Q, SMD 0805

Table 11. List of components ...continued
See [Figure 2](#) for component layout.

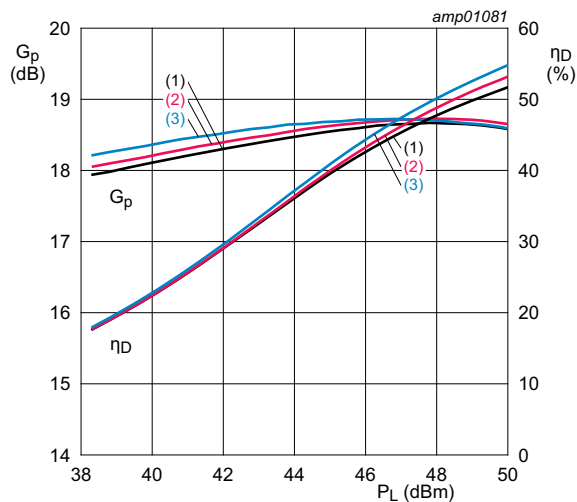
Component	Description	Value	Remarks
C25	multilayer ceramic chip capacitor	12 pF	ATC 800B
C26	multilayer ceramic chip capacitor	10 pF	ATC 800B
C32, C33	electrolytic capacitor	1000 μ F, 100 V	
R1, R12	resistor	4.7 Ω , 1 %	SMD 0805
R11	resistor	50 Ω , 25 W	Anaren: C16A50Z4
R23, R25	resistor	5.1 Ω , 1 %	SMD 1206
R24	resistor	240 Ω , 1 %	SMD 0805
CPL1	hybrid coupler	2 dB, 90°	Anaren: X3C20F1-02S

7.4 Graphical data

7.4.1 Pulsed CW



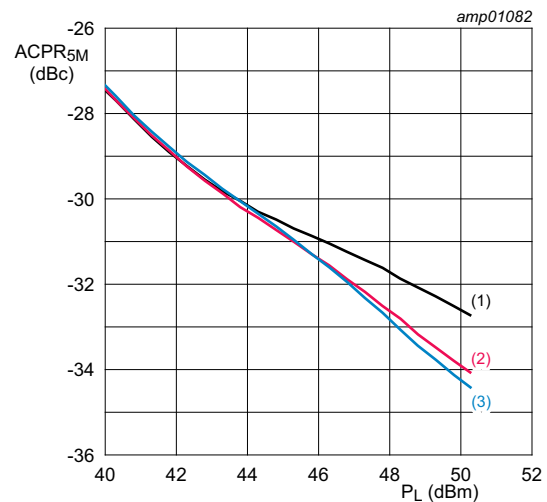
7.4.2 1-Carrier W-CDMA



$V_{DS} = 48$ V; $I_{DQ} = 400$ mA; $V_{GS(amp)peak} = 0.4$ V.

- (1) $f = 791$ MHz
- (2) $f = 806$ MHz
- (3) $f = 821$ MHz

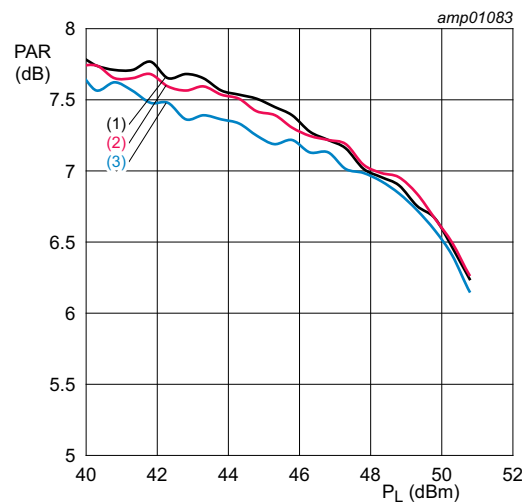
Fig 4. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 48$ V; $I_{DQ} = 400$ mA; $V_{GS(amp)peak} = 0.4$ V.

- (1) $f = 791$ MHz
- (2) $f = 806$ MHz
- (3) $f = 821$ MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

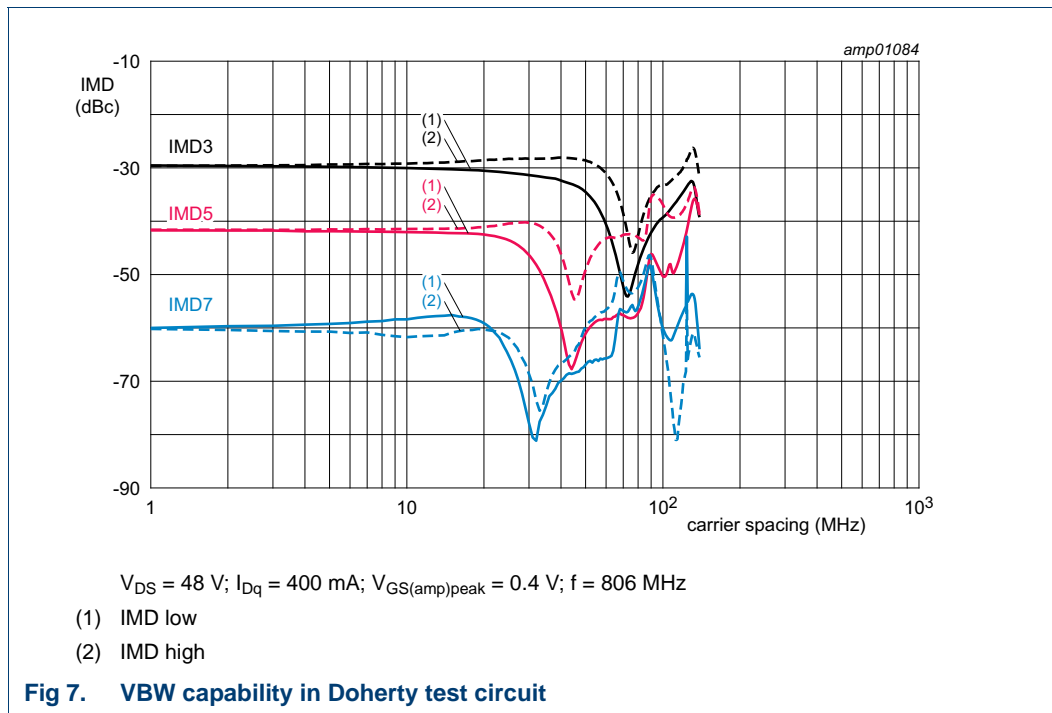


$V_{DS} = 48$ V; $I_{DQ} = 400$ mA; $V_{GS(amp)peak} = 0.4$ V.

- (1) $f = 791$ MHz
- (2) $f = 806$ MHz
- (3) $f = 821$ MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 4 leads

SOT1273-1

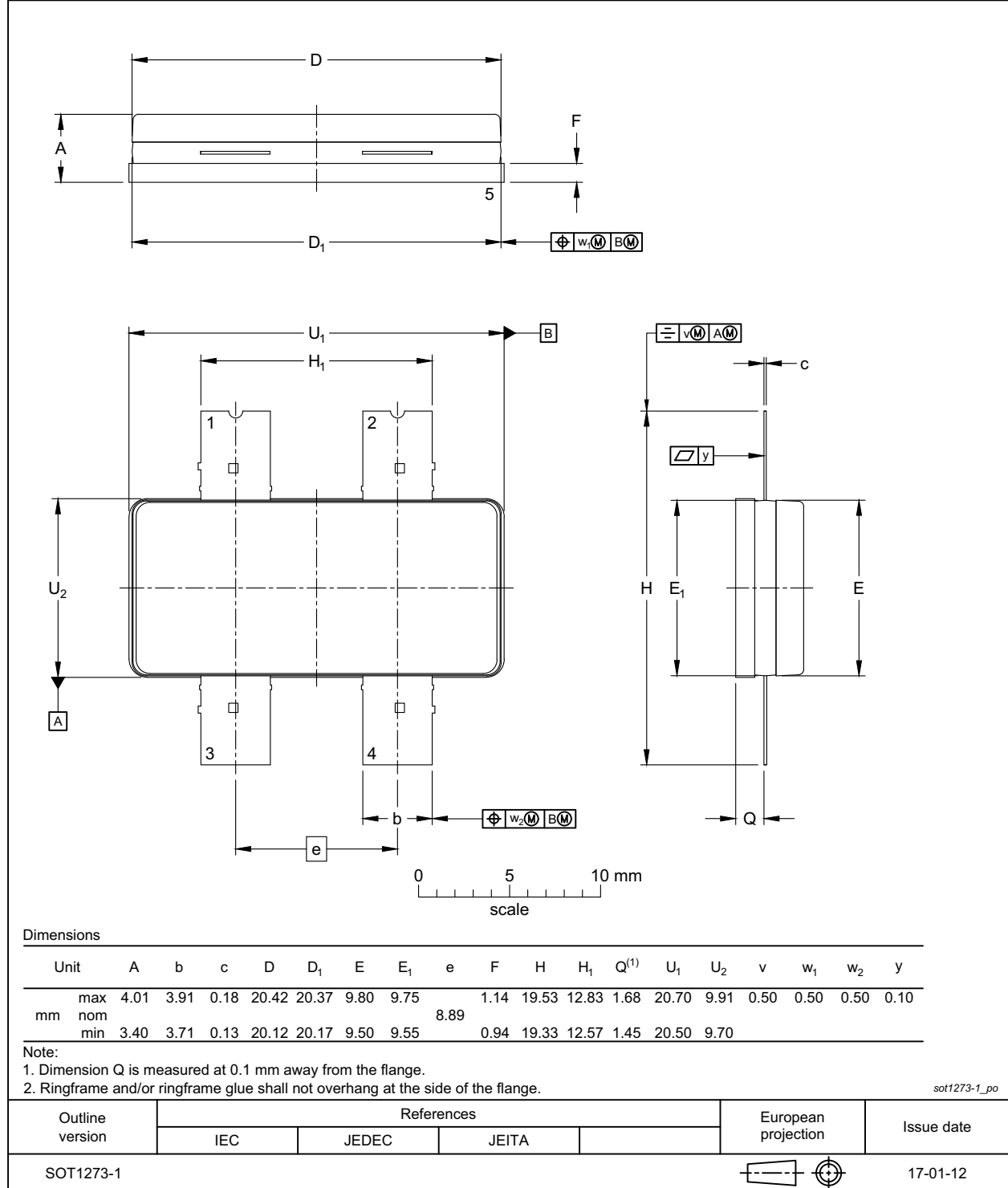


Fig 8. Package outline SOT1273-1

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
OBO	Output Back Off
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-505A v.1	20200306	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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