

N-channel 600 V, 0.195 Ω typ., 15 A MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

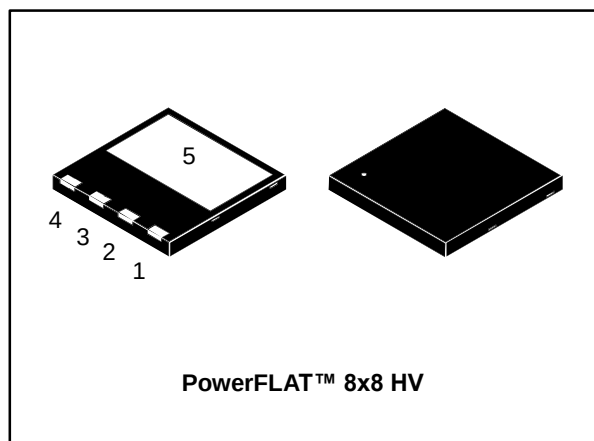
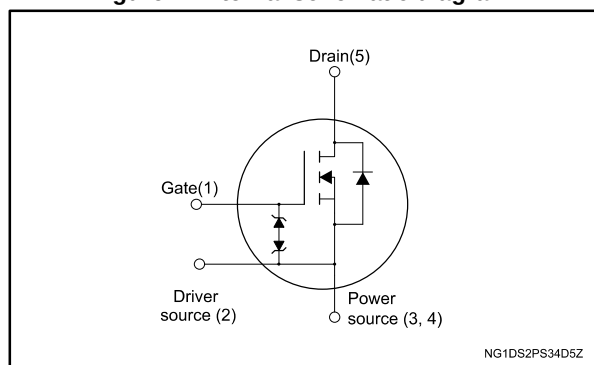


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max.	I _D
STL24N60DM2	650 V	0.220 Ω	15 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL24N60DM2	24N60DM2	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	15	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	9.5	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	60	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	125	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

(1) The value is limited by package

(2) Pulse width limited by safe operating area.

(3) $I_{SD} \leq 15\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD}=400\text{ V}$ (4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	

Notes:(1) When mounted on FR-4 board of inch^2 , 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{Jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	160	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	600			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V			1.5	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _{case} = 125 °C			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 9 A		0.195	0.220	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	1055	-	pF
C _{oss}	Output capacitance		-	56	-	
C _{rss}	Reverse transfer capacitance		-	2.4	-	
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	259	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	7	-	Ω
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 18 A, V _{GS} = 10 V (see Figure 15: "Gate charge test circuit")	-	29	-	nC
Q _{gs}	Gate-source charge		-	6	-	
Q _{gd}	Gate-drain charge		-	12	-	

Notes:

⁽¹⁾ C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 9 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform")	-	15	-	ns
t _r	Rise time		-	8.7	-	
t _{d(off)}	Turn-off delay time		-	60	-	
t _f	Fall time		-	15	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		15	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 18\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	155		ns
Q_{rr}	Reverse recovery charge		-	956		nC
I_{RRM}	Reverse recovery current		-	12.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 18\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	200		ns
Q_{rr}	Reverse recovery charge		-	1450		nC
I_{RRM}	Reverse recovery current		-	13		A

Notes:

⁽¹⁾The value is limited by package.

⁽²⁾Pulse width limited by safe operating area

⁽³⁾ Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

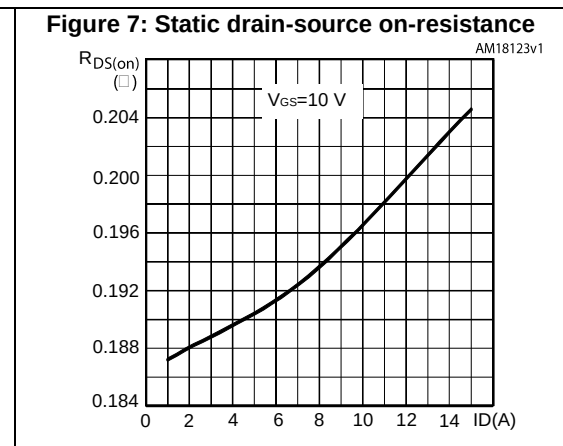
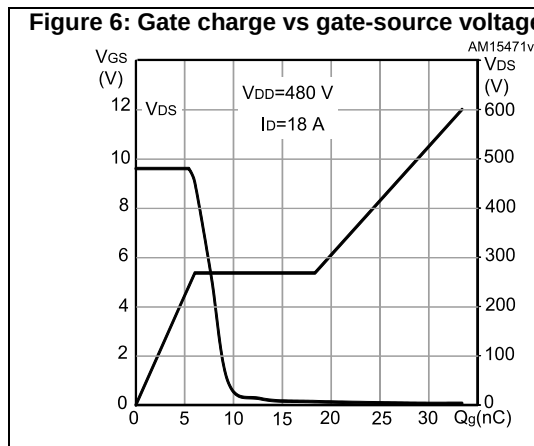
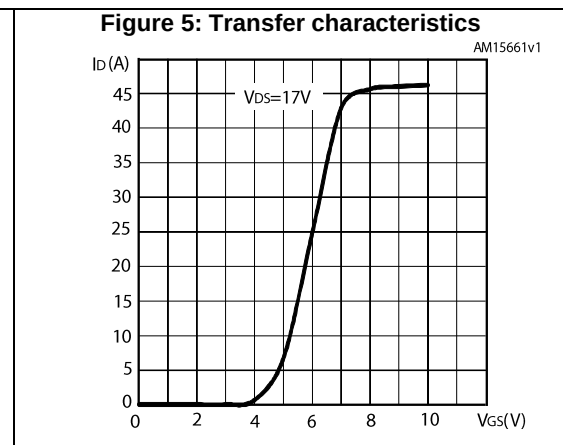
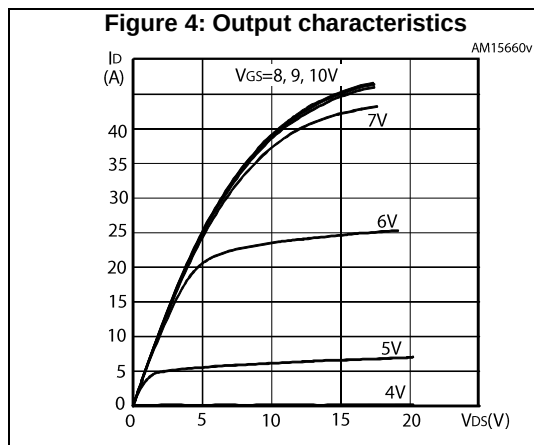
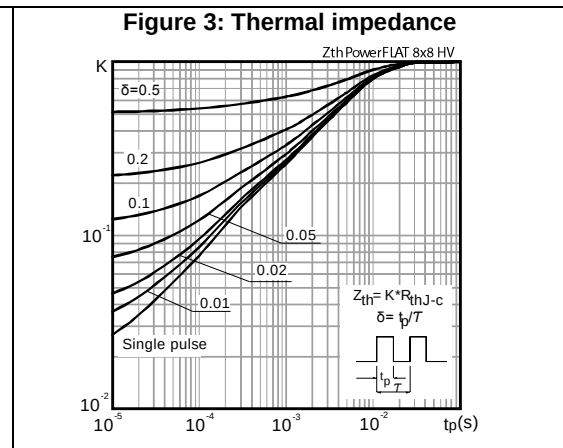
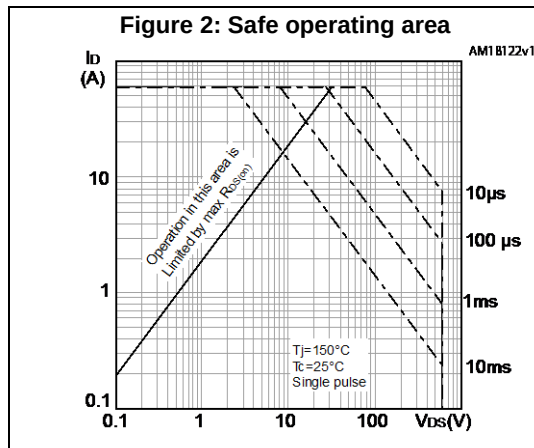


Figure 8: Capacitance variations

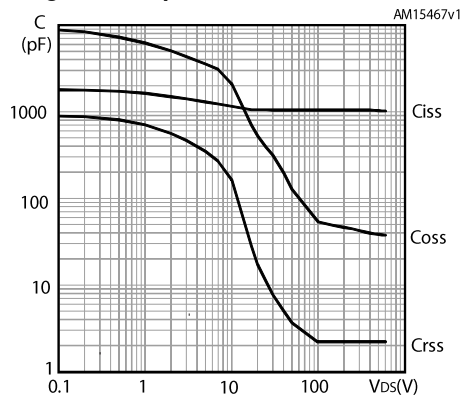


Figure 9: Normalized gate threshold voltage vs temperature

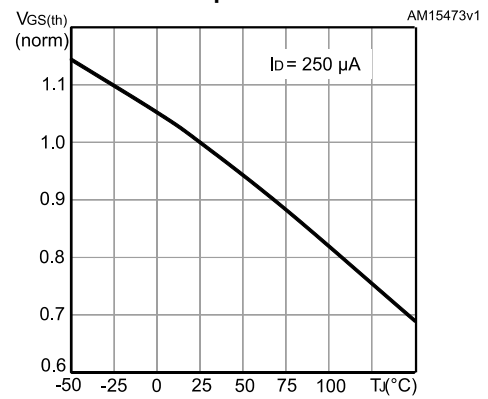


Figure 10: Normalized on-resistance vs temperature

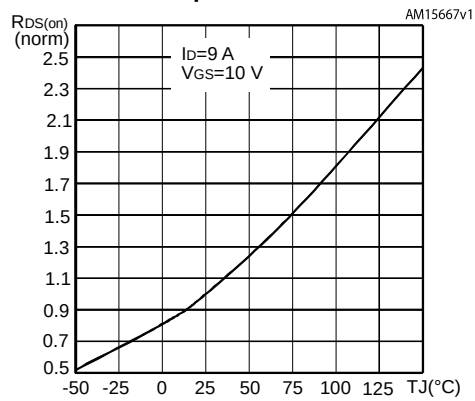


Figure 11: Normalized V(BR)DSS vs temperature

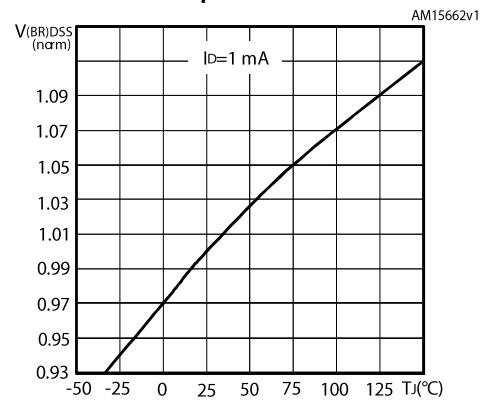


Figure 12: Output capacitance stored energy

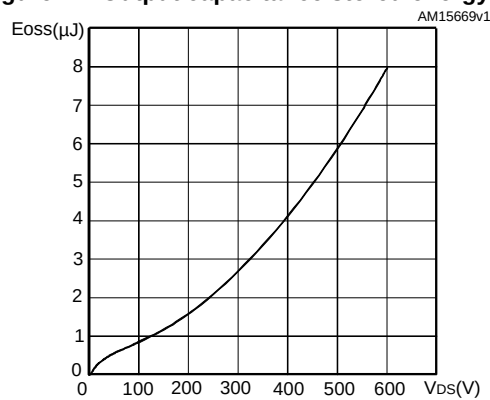
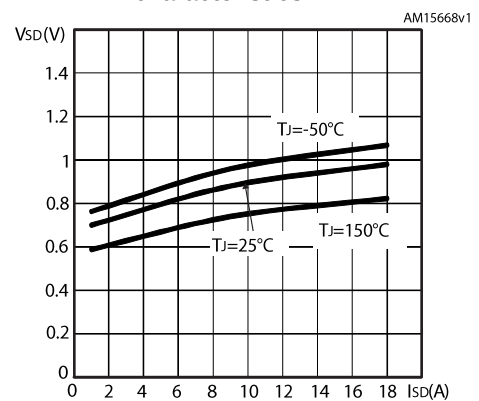


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Switching times test circuit for resistive load

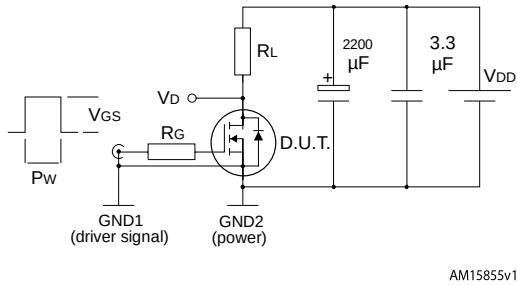


Figure 15: Gate charge test circuit

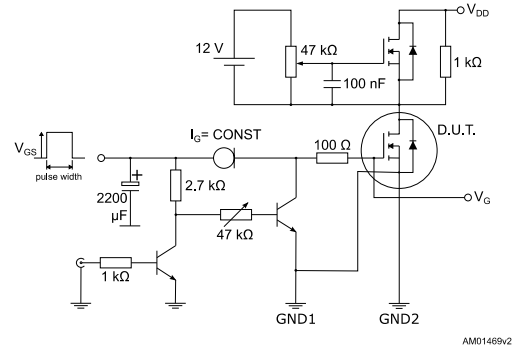


Figure 16: Test circuit for inductive load switching and diode recovery times

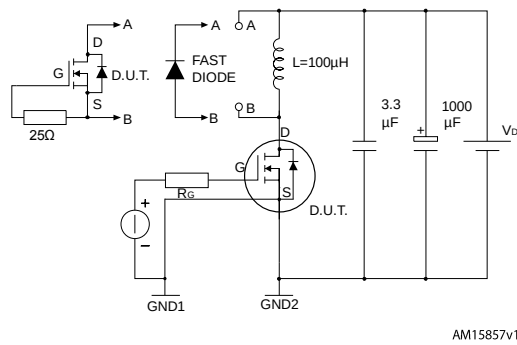


Figure 17: Unclamped inductive load test circuit

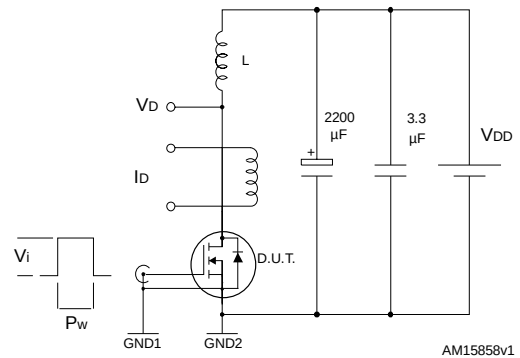


Figure 18: Unclamped inductive waveform

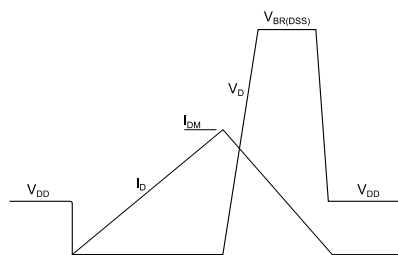
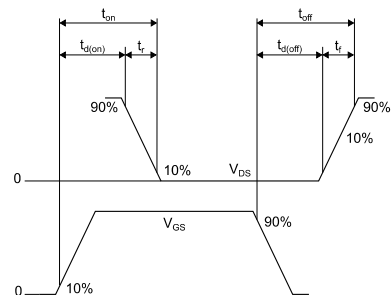


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT8x8 HV package information

Figure 20: PowerFLAT™ 8x8 HV package outline

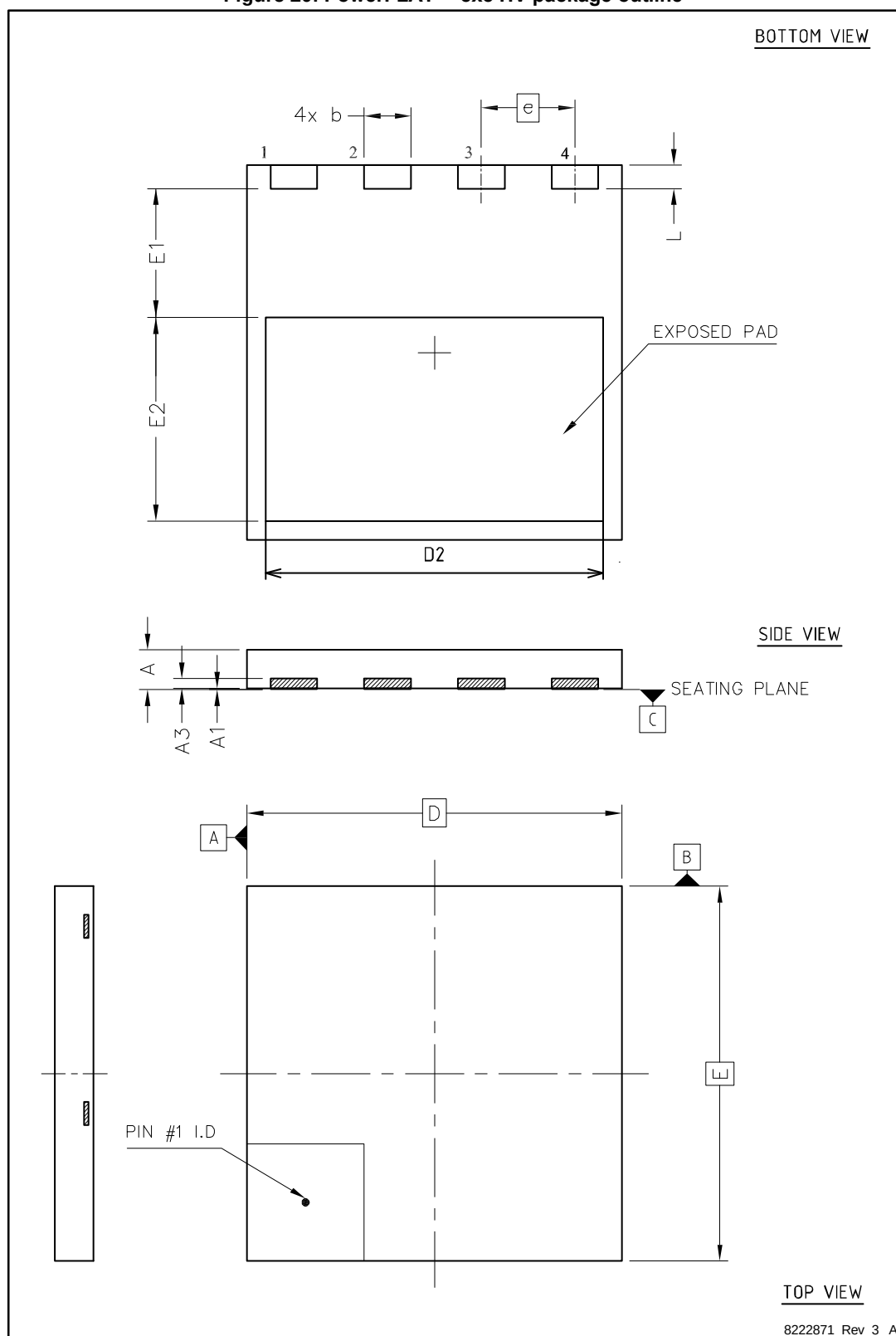
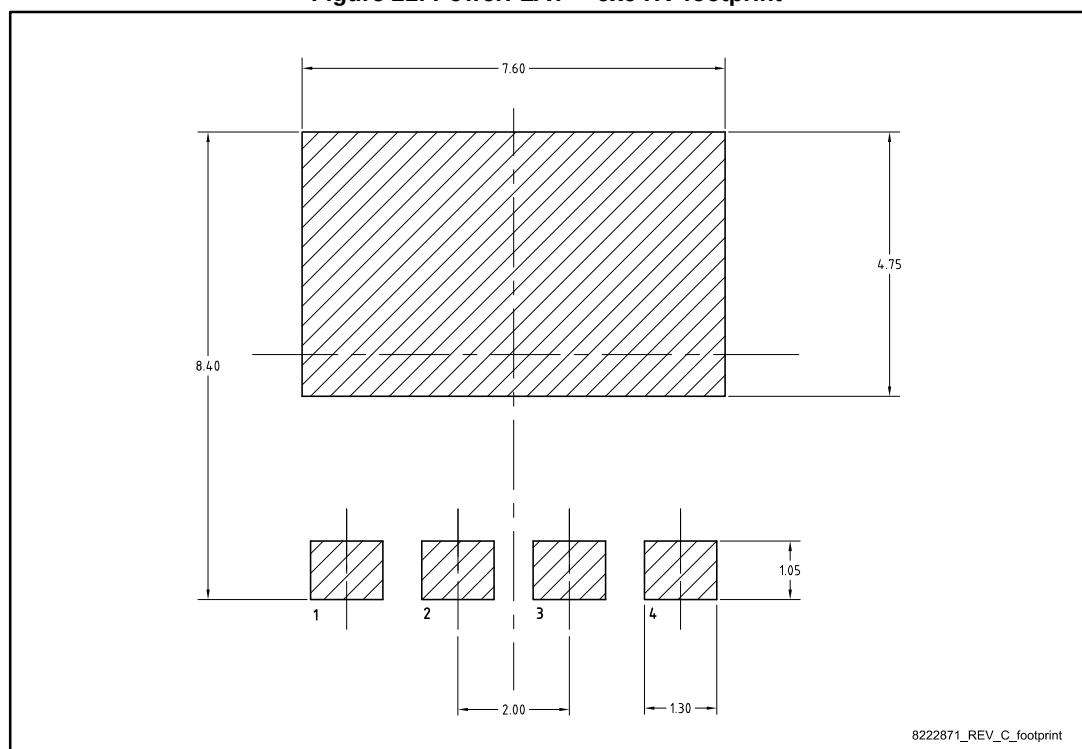


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

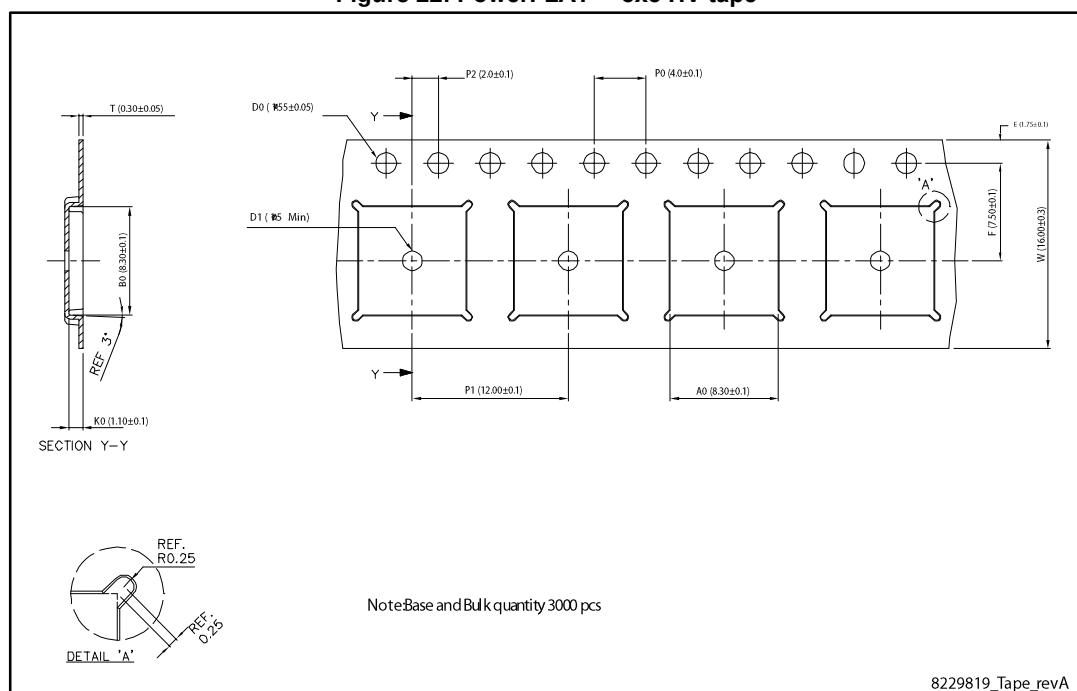
Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT8x8 HV packaging information

Figure 22: PowerFLAT™ 8x8 HV tape



All dimensions are in millimeters.

Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape

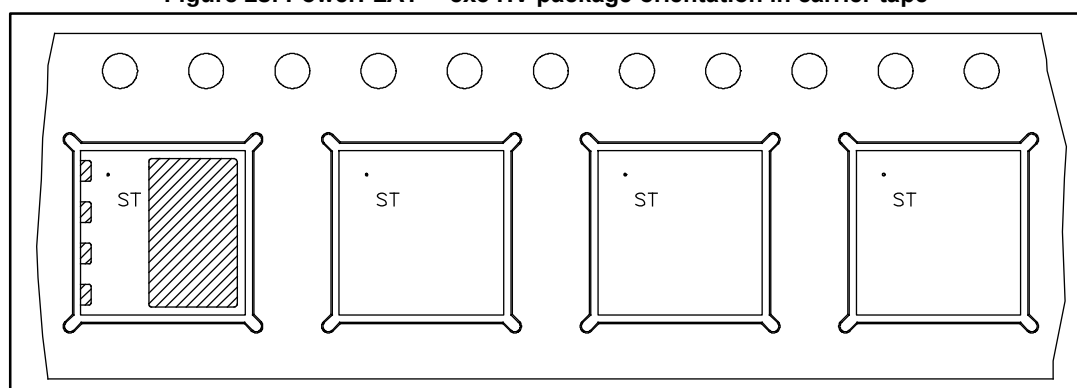
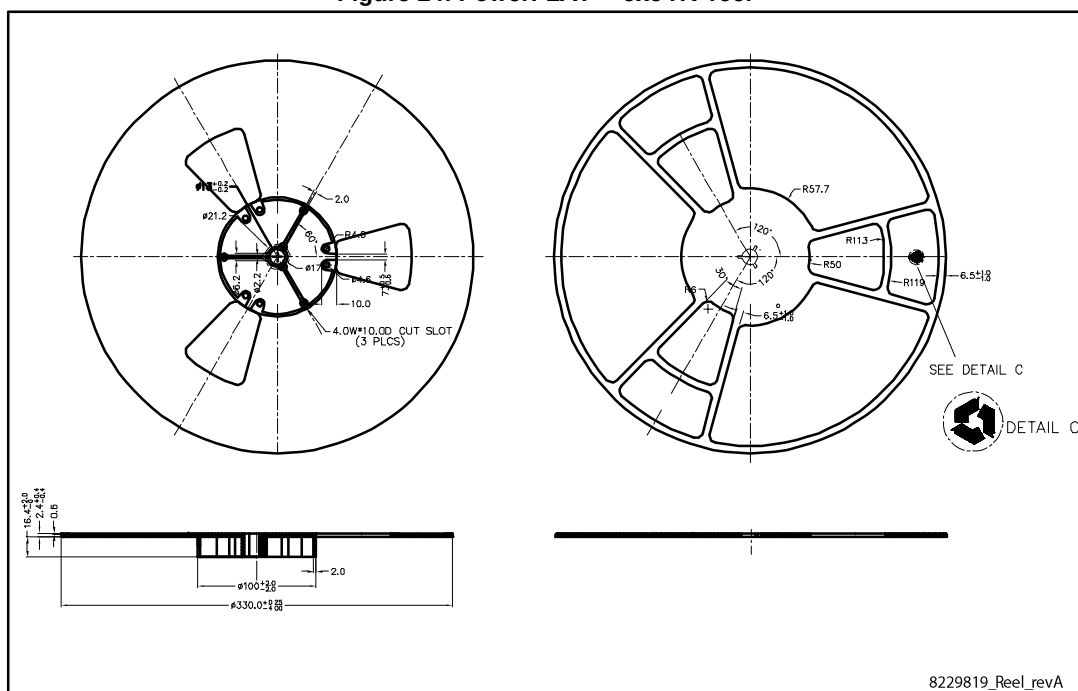


Figure 24: PowerFLAT™ 8x8 HV reel



All dimensions are in millimeters.

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
03-Mar-2014	1	First release.
21-Jan-2016	2	Modified: title, features, description and internal schematic in cover page Modified: <i>Section 3: "Test circuits"</i> Updated: <i>Section 4: "Package information"</i> Minor text changes
25-Jul-2016	3	Document status promoted from preliminary to production data.

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