BLM10D3740-35AB

LDMOS 3-stage integrated Doherty MMIC

AMPLEON

Rev. 1 — 14 December 2020

Product data sheet

1. Product profile

1.1 General description

The BLM10D3740-35AB is a 3-stage fully integrated asymmetrical Doherty MMIC solution using Ampleon's state of the art LDMOS technology. The carrier and peaking device, input splitter, output combiner and pre-match are integrated in a single package. This multiband device is perfectly suited as a final stage for small cells and massive MIMO applications in the frequency range from 3700 MHz to 4000 MHz. Available in PQFN outline.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 44 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V. Test signal: 1-carrier LTE 20 MHz; PAR = 7.6 dB.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
single carrier LTE	3900	28	5	33	39

1.2 Features and benefits

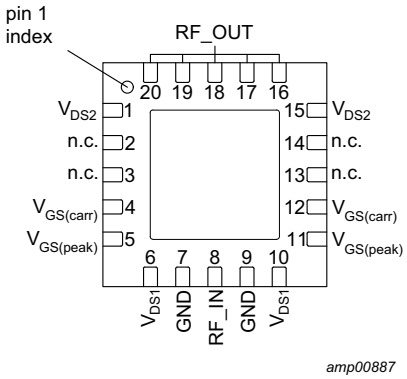
- Integrated input splitter
- Integrated output combiner
- 30 Ω output impedance thanks to integrated pre-match
- Very high efficiency thanks to asymmetry
- Designed for wideband operation (frequency 3700 MHz to 4000 MHz)
- Independent control of carrier and peaking bias
- Integrated ESD protection
- Source impedance 50 Ω; high power gain
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard 5G base stations in the 3700 MHz to 4000 MHz frequency range

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{DS2}	1	drain-source voltage of final stages
n.c.	2	not connected
n.c.	3	not connected
$V_{GS(carr)}$	4	gate-source voltage of carrier
$V_{GS(peak)}$	5	gate-source voltage of peaking
V_{DS1}	6	drain-source voltage of driver stages
GND	7	RF ground
RF_IN	8	RF input
GND	9	RF ground
V_{DS1}	10	drain-source voltage of driver stages
$V_{GS(peak)}$	11	gate-source voltage of peaking
$V_{GS(carr)}$	12	gate-source voltage of carrier
n.c.	13	not connected
n.c.	14	not connected
V_{DS2}	15	drain-source voltage of final stages
RF_OUT	16	RF output
RF_OUT	17	RF output
RF_OUT	18	RF output
RF_OUT	19	RF output
RF_OUT	20	RF output
GND	flange	RF ground

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3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM10D3740-35AB	PQFN20	plastic thermal enhanced quad flat package; no leads; 20 terminals; body 8.0 x 8.0 x 2.1 mm	SOT1462-1

4. Block diagram

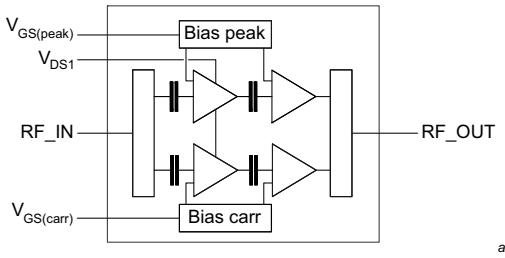

Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	200	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 2 W [1]	4	K/W
		T_{case} = 90 °C; P_L = 5 W [1]	3.2	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 7.6 dB.

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7. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 42 mA	1.65	2.0	2.6	V
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA

Table 7. RF Characteristics

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 42 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; $P_{L(AV)}$ = 5 W; f = 3850 MHz measured in an Ampleon production device interface board.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: single carrier pulsed CW [1]						
G_p	power gain	P_L = 5 W (37 dBm)	32.2	34.2	36.4	dB
η_D	drain efficiency	P_L = 5 W (37 dBm)	34	41	-	%
		$P_L = P_{L(3dB)}$	41	47	-	%
RL_{in}	input return loss		-	-	−10	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		44.7	45.2	-	dBm

[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 µs).

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8. Application information

Table 8. Typical performance

T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 44 mA (carrier); $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.5 V. Test signal: 1-carrier LTE; PAR = 7.6 dB at 0.01 % probability CCDF; unless otherwise specified, typical performance in an Ampleon f = 3700 MHz to 4000 MHz frequency band application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 3900 MHz [1]	-	45.4	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	at 3 dB compression point; f = 3900 MHz [2]	-	-26	-	°
η_D	drain efficiency	8 dB OBO ($P_{L(AV)}$ = 37 dBm); f = 3900 MHz	-	39	-	%
G_p	power gain	$P_{L(AV)}$ = 37 dBm; f = 3900 MHz	-	33.1	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 37 dBm; 2-tone CW; f = 3800 MHz	-	420	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 37 dBm; f = 3700 MHz to 4000 MHz	-	1.9	-	dB
$ACPR_{20M}$	adjacent channel power ratio (20 MHz)	$P_{L(AV)}$ = 37 dBm; f = 3900 MHz	-	-31	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	f = 3900 MHz [3]	-	0.07	-	dB/°C
$\Delta P_{L(3dB)}/\Delta T$	output power at 3 dB gain compression variation with temperature	f = 3900 MHz [1]	-	0.016	-	dBm/°C
K	Rollett stability factor	T_{case} = −30 °C; f = 0.1 GHz to 6.1 GHz [3]	-	>1	-	

[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 μs).

[2] 25 ms CW power sweep measurement.

[3] S-parameters.

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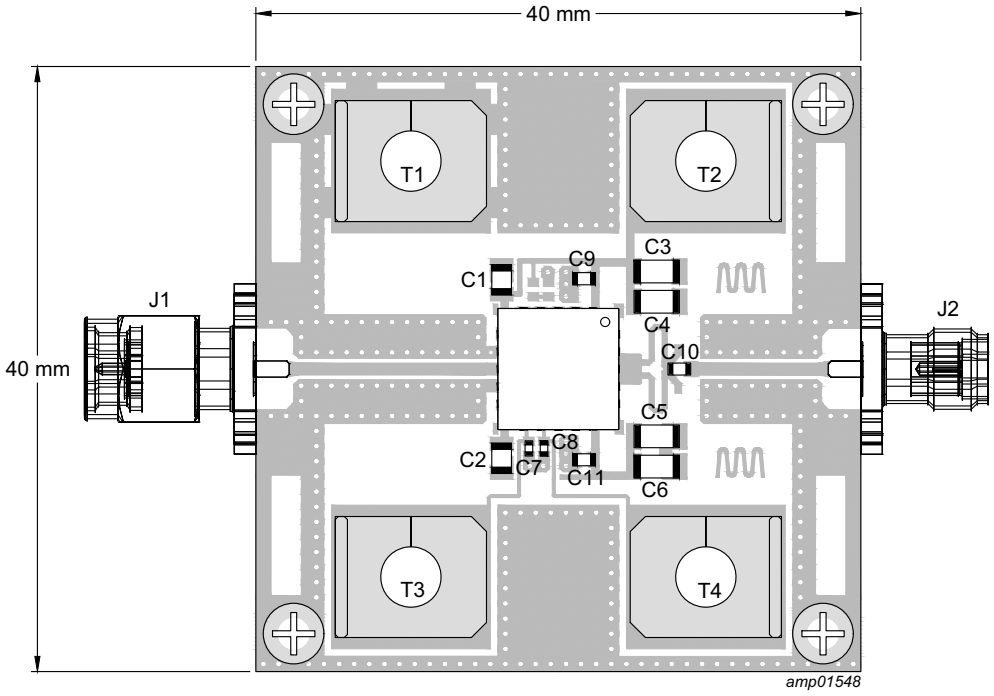

Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

Fig 3. Component layout

Table 9. Demo test circuit list of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	10 μF, 6.3 V	Murata: GRM21BR60J106KE01L
C3, C4, C5, C6	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: GRM31CR61H106KA12L
C7, C8	multilayer ceramic chip capacitor	4.7 μF, 6.3 V	Murata: GRM155R60J475ME47D
C9	multilayer ceramic chip capacitor	3.3 pF ± 0.1 %	Murata: GQM1875C2E3R3BB12
C10	multilayer ceramic chip capacitor	3 pF ± 0.1 %	Murata: GQM1875C2E3R0BB12
C11	multilayer ceramic chip capacitor	3 pF ± 0.1 %	Murata: GQM1875C2E3R0BB12
J1	SMA Coaxial panel connector male		Huber & Suhner: 13_SMA-50-0-2/111_N
J2	SMA Coaxial panel connector female		Huber & Suhner: 23_SMA-50-0-2/111_N
T1, T2, T3, T4	PCB Terminal	6.35 mm × 0.81 mm, 4.1 mm	TE connectivity

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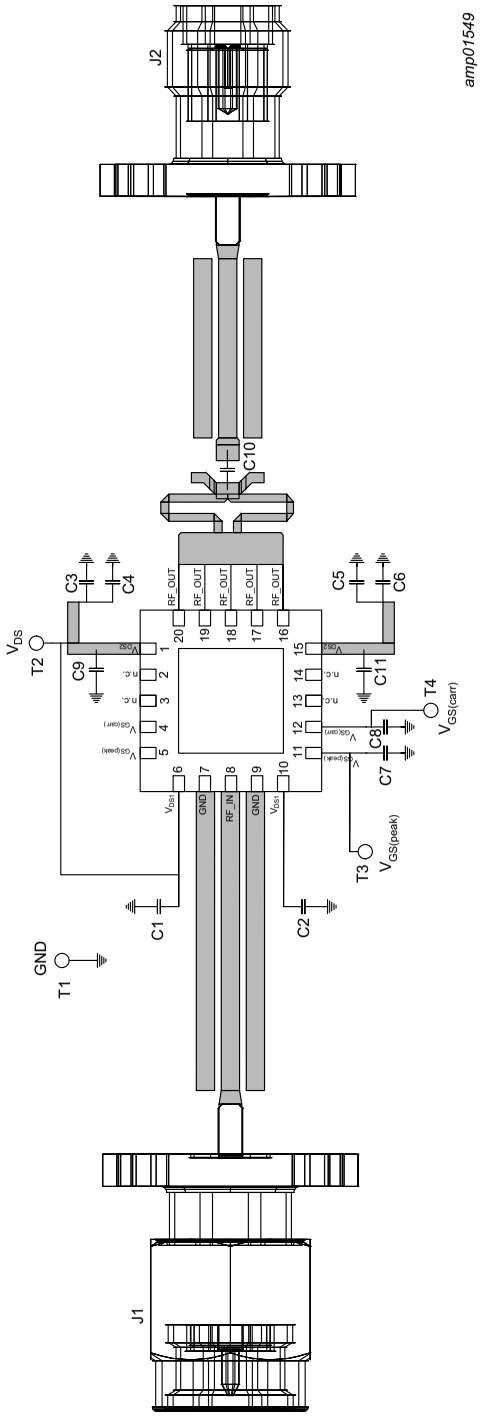

Fig 4. Electrical schematic

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8.1 Ruggedness in a Doherty operation

The BLM10D3740-35AB is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 45 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; P_i corresponding to $P_{L(3dB)} - 5$ dB under Z_S = 50 Ω load; f = 3800 MHz (1-carrier W-CDMA; PAR = 9.9 dB); T_{case} = 25 °C.

8.2 Impedance information

Table 10. Typical impedance for optimum Doherty operation

Measured load-pull data; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 42 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; t_p = 100 µs; δ = 10 %.

f	tuned for optimum Doherty operation				
	Z_L	$P_{L(3dB)}$	$G_{p(max)}$	η_{add} [1]	η_{add} [2]
(MHz)	(Ω)	(dBm)	(dB)	(%)	(%)
3600	28.06 – j2.10	45.90	34.41	48.24	39.00
3700	23.04 – j5.66	45.88	35.68	49.89	42.17
3800	22.77 – j7.56	45.82	35.98	51.62	43.40
3900	22.76 – j7.54	45.61	35.02	52.61	42.71
4000	24.82 – j5.25	45.26	32.87	51.26	38.20
4100	19.20 – j4.72	44.79	29.92	49.13	32.16

[1] at $P_{L(3dB)}$.

[2] at 37 dBm.

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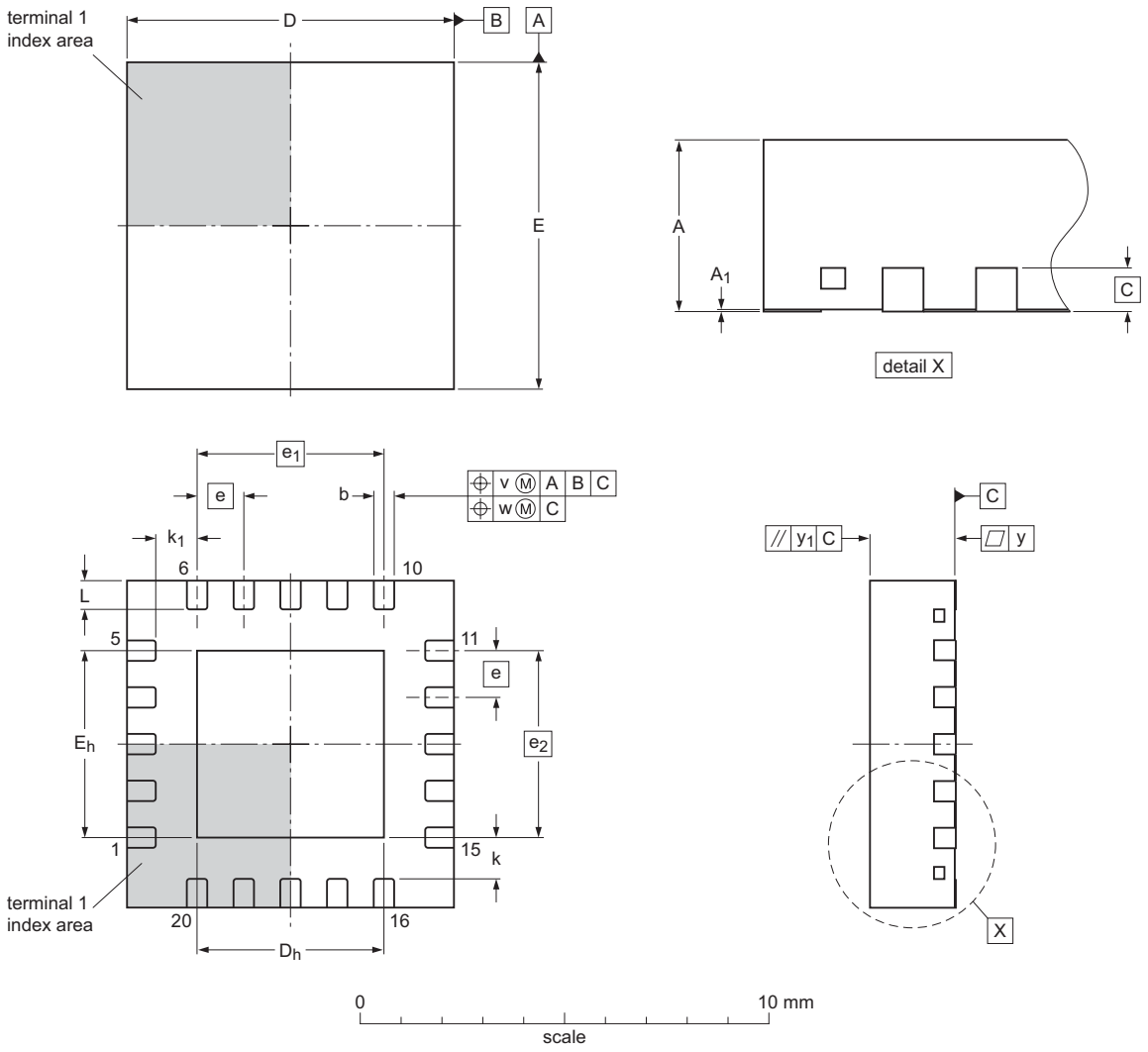
9. Package outline

PQFN20: plastic thermal enhanced quad flat package; no leads; 20 terminals; body 8.0 x 8.0 x 2.1 mm **SOT1462-1**



Dimensions

Unit		A(1)	A1	b	C	D(1)	Dh	E(1)	Eh	e	e1	e2	k	k1	L	v	w	y	y1
	max	2.20	0.05	0.60		8.1	4.72	8.1	4.72						0.8				
mm	nom	2.10		0.50	0.508	8.0	4.62	8.0	4.62	1.15	4.6	4.6			0.7	0.1	0.05	0.1	0.1
	min	2.00	0.00	0.40		7.9	4.52	7.9	4.52				0.99	0.99	0.6				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1462-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1462-1						~~15-10-12~~ 17-06-23

Fig 5. Package outline SOT1462-1 (PQFN20)

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10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1B [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1B is granted to any part that passes after exposure to an ESD pulse of 500 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MIMO	Multiple Input Multiple Output
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM10D3740-35AB v.1	20201214	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 14 December 2020
Document identifier: BLM10D3740-35AB