

Features

- Low On-resistance, $R_{on}=1.7\Omega$ when $A=5V$
- 1.8V Logic Compatible Control Pin
- A Overrides VCC to Achieve True Isolation Even When Supply Is Dead
- High Off-Isolation: $-100dB @ 100KHz$
- Low Channel-to-Channel Crosstalk: $-97dB @ 100KHz$
- High Bandwidth ($-3dB @ 700MHz$) Suitable For USB2.0 High-Speed Routing
- Low Quiescent Current ($<2\mu A$) With Very Wide Supply Range ($1.5V \sim 5.5V$)

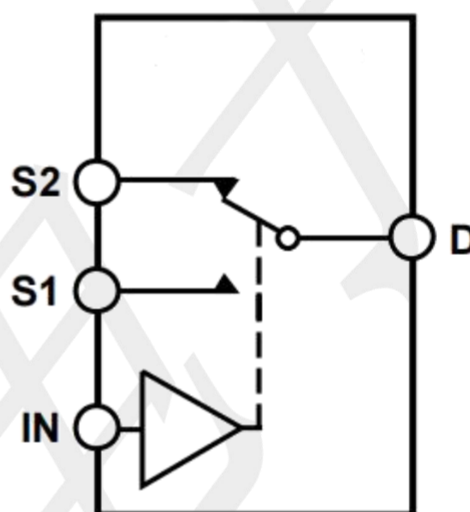
General Description

The is a low voltage single-pole,double-throw (SPDT) analog switch intending for use in chopping,modem, signal gating, and signal multiplexing for analog-to-digital and digital -to-analog conversion systems.

Applications

- Cell phones and TWS headset
- Audio, Video, UART, USB2.0 Signal and Supply Routing

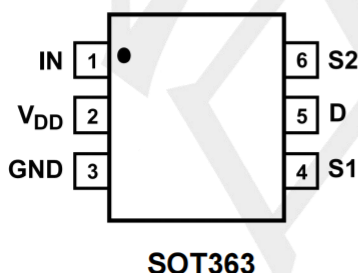
Logic Diagram



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	IN	Select input
2	VDD	Supply voltage
3	GND	Ground (0 V)
4	S1	Independent input or output
5	D	Common output or input
6	S2	Independent input or output

Pin Configuratio



Function Table

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

Note:1: HIGH voltage level;0: LOW voltage level.

Absolute Maximum Ratings

(Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.3 ~ +6.5	V
Switch Voltage	V _S	-0.3 ~ +6.5	V
Input Voltage	V _{IN}	-0.3 ~ +6.5	V
Continuous Current Through D, S1, S2		±128	mA
Peak Current Through D, S1, S2 (pulsed at 1ms 50% duty cycle)		±200	mA
Storage Temperature Range	T _{STG}	-55 ~ +150	°C
Operating Junction Temperature	T _J	150	°C
Junction to Ambient	R _{θJA}	350	°C/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Recommend operating ratings

(Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Operating	V _{CC}	1.5 ~ 5.5	V
Control Input Voltage	V _{SEL}	-0.3 ~ 5.5	V
Input Signal Voltage	V _A	-0.3 ~ 5.5	V
Operating Temperature	T _A	-40 ~ +85	°C

Electrical Characteristics (TA =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V _{IH}	VCC=3.3V ~ 5.5V	1.6	--	--	V
		VCC=1.5V ~ 3.3V	1.4	--	--	V
Low-Level Input Voltage	V _{IL}	VCC=3.3V ~ 5.5V	--	--	0.6	V
		VCC=1.5V ~ 3.3V	--	--	0.4	V
Supply quiescent current	I _{CC}	I _A =0, V _{SEL} =0 or V _{SEL} =VCC	--	--	1.0	uA
Increase in ICC per input	I _{CC} T	I _A =0, VCC=4.5V V _{SEL} >1.8 or V _{SEL} <0.5	--	--	1.0	uA
Off state leakage from D to S1 (or S2)	I _A	V _A = 5.5V , V _{B0(or B1)} = 0V	--	--	±2.0	uA
On-Resistance	R _{ON1}	V _A =0 ~ 0.5V, I _A =30mA	--	3.6	3.9	Ω
	R _{ON2}	V _A =0.5 ~ 2.0V, I _A =30mA	--	3.0	3.5	Ω
	R _{ON3}	V _A =2.0 ~ 4.0V, I _A =30mA	--	2.5	3.5	Ω
	R _{ON4}	V _A =4.0 ~ 5.5V, I _A =30mA	--	1.7	1.8	Ω
On-Resistance Flatness	R _{FLAT1}	V _A =0 ~ 0.5V, I _A =30mA	--	1.6	--	Ω
	R _{FLAT2}	V _A =0.5 ~ 2.0V, I _A =30mA	--	0.7	--	Ω
	R _{FLAT3}	V _A =2.0 ~ 4.0V, I _A =30mA	--	0.5	--	Ω
	R _{FLAT4}	V _A =4.0 ~ 5.5V, I _A =30mA	--	0.3	--	Ω
On-Resistance Matching Between Channels	Δ R _{ON}	V _A =0~5.5V, I _A =30mA	--	0.1	0.2	Ω

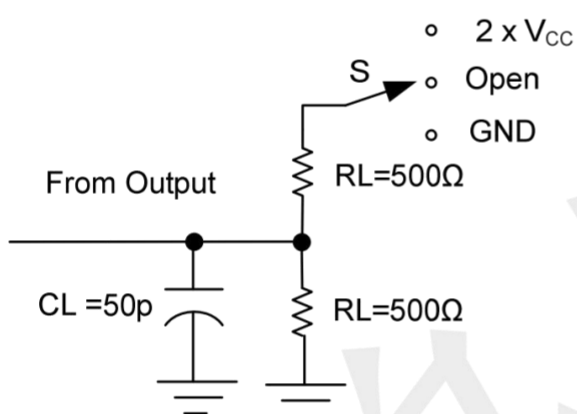
AC Electronics Characteristics (Ta=25oC, VCC=3.3V, unless otherwise noted)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Turn-On Time	T _{ON}	V _A =1.5V, C _L =35pF, R _L =50Ω	--	200	--	ns
Turn-Off Time	T _{OFF}	V _A =1.5V, C _L =35pF, R _L =50Ω	--	200	--	ns
Break-Before-Make time	T _{BBM}	V _A =1.5V, C _L =35pF, R _L =50Ω	--	500	--	ns
-3dB Bandwidth	BW	R _L =50Ω, C _L =0pF	--	700	--	MHz
Off isolation	OIRR	F=1KHz, R _L =50Ω	--	-81	--	dB
		F=10KHz, R _L =50Ω	--	-80	--	dB
Crosstalk	Xtalk	F=1KHz, R _L =50Ω	--	-83	--	dB
		F=10KHz, R _L =50Ω	--	-82	--	dB
Total Harmonic Distortion	THD	F=20Hz to 20KHz V _A =600mVp-p @R _L =32Ω	--	-80	--	dB

Capacitance ($T_a=25^{\circ}\text{C}$ unless otherwise noted)

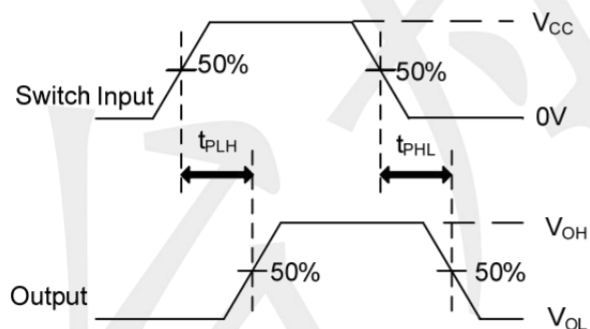
PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Off capacitance	C_{OFF}	$F=100\text{KHz}$, $V_{CC}=3.3$	--	5.0	--	pF
On capacitance	C_{ON}	$F=100\text{KHz}$, $V_{CC}=3.3$	--	7.0	--	pF

TEST CIRCUIT AND WAVEFORMS



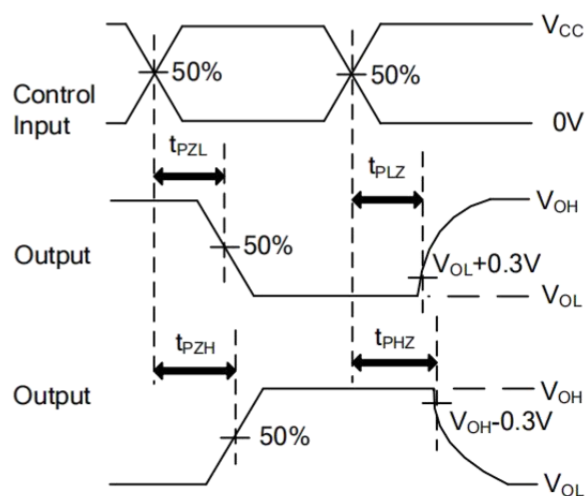
TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

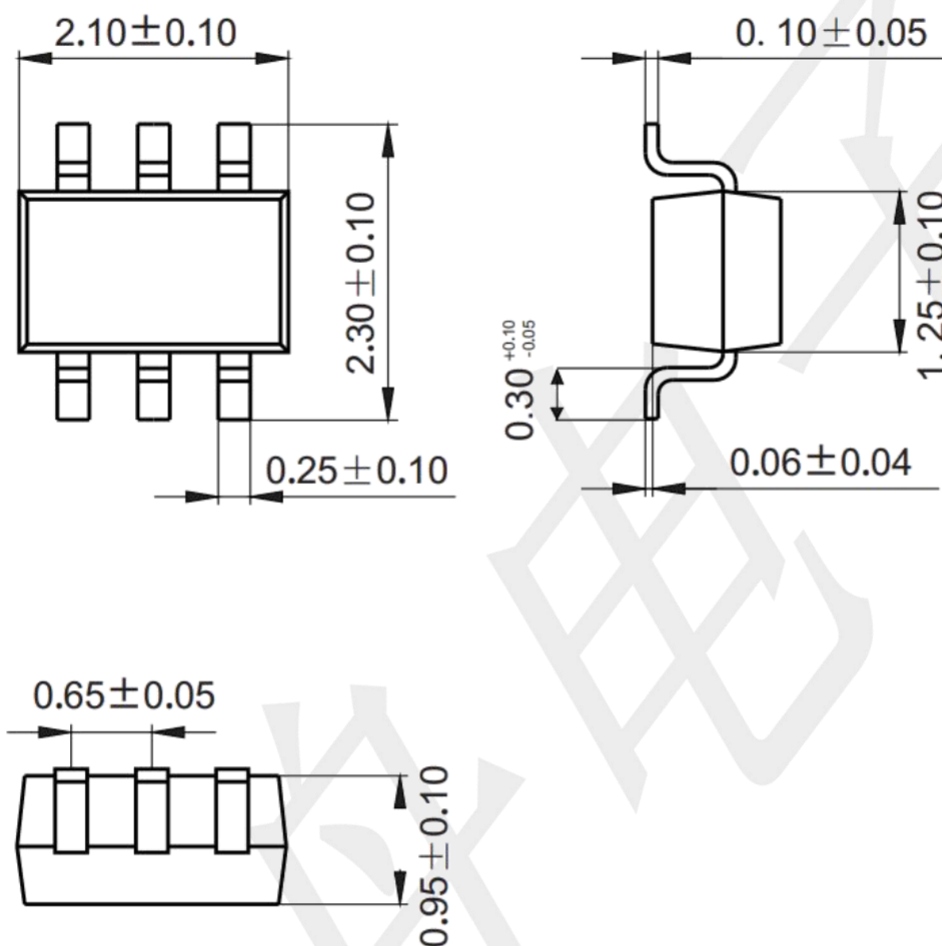
Note: C_L includes probe and jig capacitance.
 $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r \leq 2.5\text{ns}$, $t_f \leq 2.5\text{ns}$.



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

Package information

SOT363 (Unit: mm)



Mounting Pad Layout (unit: mm)

