VersaClock® 6E 5P49V60, 5P49V5965 and 5P49V6975 Evaluation Board

This evaluation board is designed to help the customer evaluate the 5P49V60, 5P49V6965 and 5P49V6975 devices. When the board is connected to a PC running Renesas Timing Commander™ Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performance. The 5P49V6975 has an integrated crystal. The 5P49V60 and 5P49V6965 uses an external crystal. The devices are pin compatible and can use the same board.

Contents

Figures

1. Board Overview

Use Figure 1 and Table 1 to identify power supply jacks, USB connector, and the input and output clock SMA connectors.

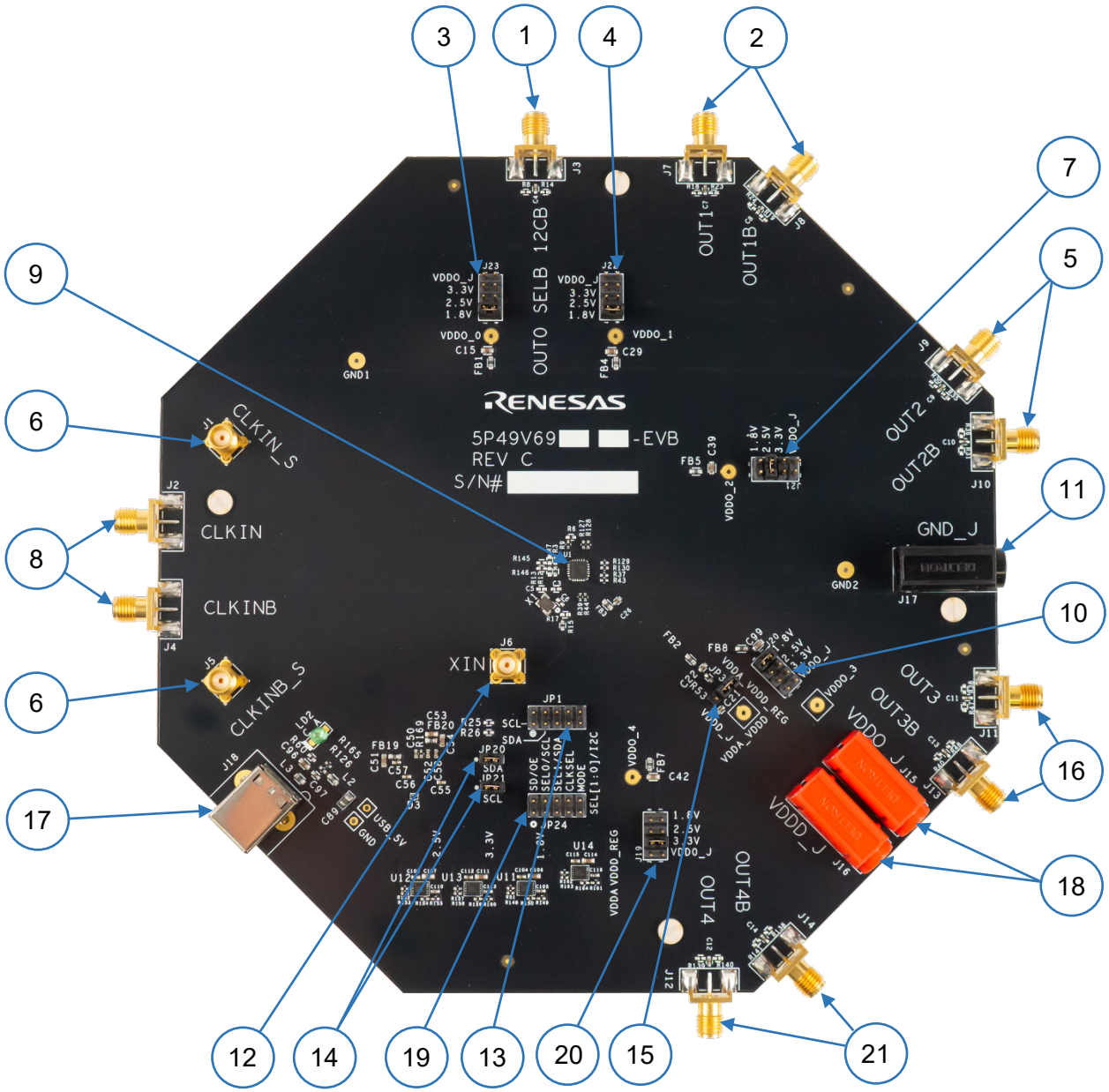


Figure 1. 5P49V6965 Evaluation Board

Table 1. Evaluation Board Pins and Functions

Label Number	Name	On-Board Connector Label	Function
1	Output 0	J3	Single-ended LVCMOS clock output
2	Output 1	J7, J8	Differential clock output
3	VDDO_0	J23	Power supply voltage selector for output 0
4	VDDO_1	J22	Power supply voltage selector for output 1
5	Output 2	J9, J10	Differential clock output
6	CLKIN Sense	J1, J5	Differential input clock, sense output
7	VDDO_2	J21	Power supply voltage selector for output 2
8	CLKIN Input	J2, J4	Differential clock input
9	5P49V6965	U1	Evaluation device
10	VDDO_3	J20	Power supply voltage selector for output 3
11	Ground Jack	J17	Ground jack for external power supply
12	XIN	J6	Input for overdriving XIN pin
13	Aardvark Connector	JP1	For Aardvark connection
14	I^2C Control Jumpers	JP20, JP21	Two jumpers to disconnect I^2C from the FTDI USB-to-I2C interface, to allow SEL0/1 (hardware configuration select) switching
15	VDDA/D	JP3	Power supply selector for VDDA and VDDD
16	Output 3	J11, J13	Differential clock output
17	USB Interface	J18	Used for connection with a PC and for interaction with the Renesas Timing Commander software.
18	VDD Jacks	J15, J16	VDD jacks for external power supply
19	Config Header	JP24	SD/OE SEL0/SCL SEL1/SDA CLKSEL MODE
20	VDDO_4	J19	Power supply voltage selector for output 4
21	Output 4	J12, J14	Differential clock output

2. Board Power Supply

The voltage for each of the four VDDO pins can be selected with jumpers. Select one of the on-board LDO supplies or the supply jack J15. A jumper connects the VDDO pin to a power source of choice.

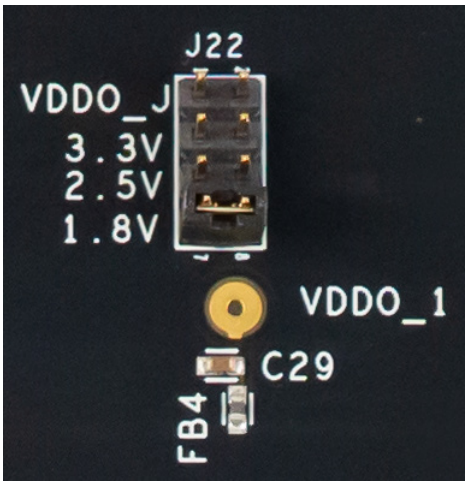


Figure 2. VDDO_1 Voltage Selector

In Figure 2, the voltage for VDDO_1 is chosen to be 1.8V. The 3.3V, 2.5V and 1.8V are from on board regulators that get their power from the USB connector. The VDD Jacks are for connecting to a bench power supply, useful for supply current measurement.

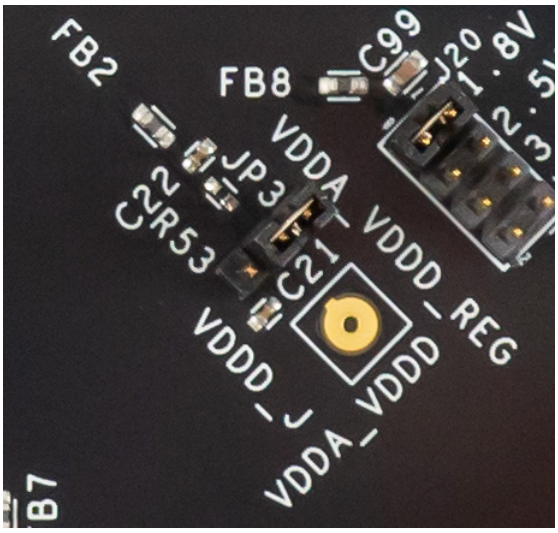


Figure 3. VDDA/D Power Source Selector

JP3 selects the power source for the VDDA and VDDD pins between an on-board 3.3V regulator and the VDDD_J Jack for a bench power supply. In Figure 3, the source for VDDA and VDDD is chosen to be the on-board 3.3V regulator.

3. Connecting the Board to a Computer

The evaluation board can be connected to a computer with the USB connector. The on-board USB-to-I2C bridge (FTDI chip) does the data communication and the +5V in the USB bus powers the on-board regulators. Using a bench power supply with the VDD jacks is optional. The board can fully function with just the USB cable to a computer.

The Timing Commander software can control the 5P49V60/6965/6975 device on the board. Timing Commander is compatible with both the on-board USB-to-I2C bridge and the Aardvark adapter. Timing Commander displays a block diagram where you can enter the configuration. Next, you can program that configuration into the 5P49V6965 on the board where Timing Commander defines the proper hex-code sequence to program into the device.

The jumpers JP20 and JP21 configure the I^2C configuration.

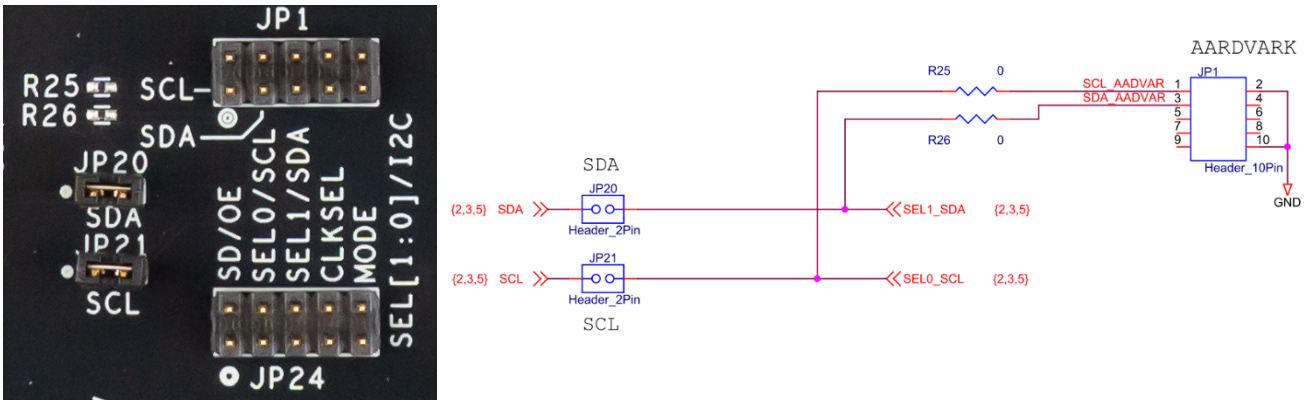


Figure 4. Configure I^2C Operation

Labels “SDA” and “SCL” connect to the USB-to-I2C bridge chip. When using an Aardvark or when operating the SEL0/1 switches, jumpers JP20 and JP21 need to be removed to disconnect the USB-to-I2C bridge. Labels “SEL1_SDA” and “SEL0_SCL” are the SEL1/SDA and SEL0/SCL pins on the 5P49V60/6965/6975 device.

Table 2. Configure I^2C Operation

	JP20	JP21
Use on-board USB-to-I2C bridge.	Yes	Yes
Use Aardvark or other adapter connected to JP1. The adapter has its own pull-ups enabled.	No	No
Use Aardvark or other adapter connected to JP1. The adapter does not have pull-ups or has them disabled. Add jumpers to JP24 to enable on-board pull-ups for SEL0_SCL and SEL1_SDA.	No	No
Operate the SEL0 and SEL1 switches.	No	No

4. U1 Switch Operation

Figure 5 shows the JP24 configuration header and schematic.

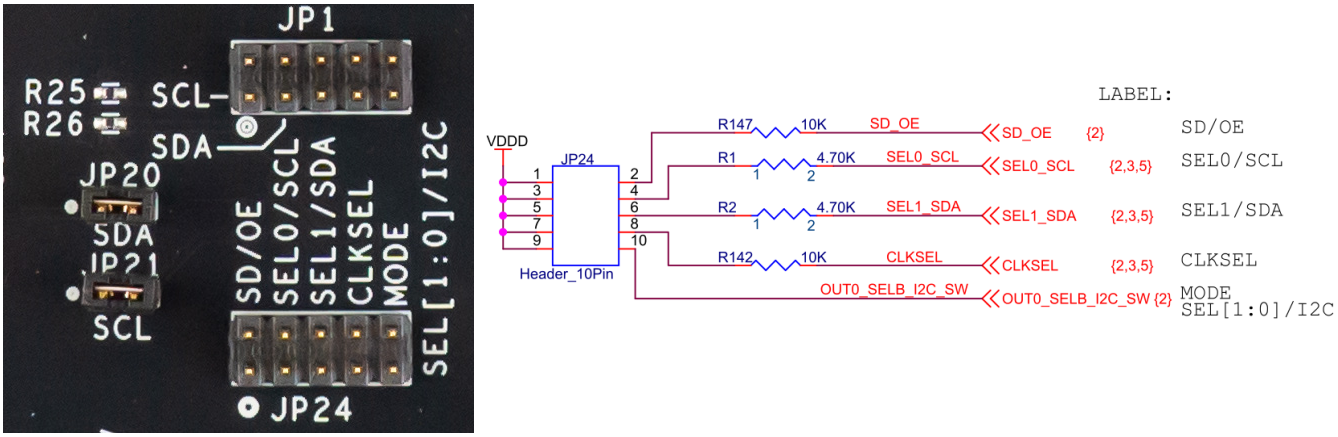


Figure 5. JP24 Configuration Header

The jumpers connect to pins on the 5P49V60/6965/6975 device.

- **OE**: Connects to the SD/OE pin for output enable or shut-down operation.
- **SEL0**: Connects to the SEL0/SCL pin. The main purpose of this switch is to operate SEL0 when the device has started in hardware select mode. This switch can also be used to add an extra pull-up (4.7kΩ) on the SCL line for I^2C operation.
- **SEL1**: Connects to the SEL1/SDA pin. The main purpose of this switch is to operate SEL1 when the device has started in hardware select mode. This switch can also be used to add an extra pull-up (4.7kΩ) on the SDA line for I^2C operation.
- **CLKSEL**: Connects to the CLKSEL pin for selecting between crystal input or CLKIN differential clock input.
- **Mode**: Pulls on the OUT0_SEL_I2CB pin on the device to select the operation mode at power-up. The state of the OUT0_SEL_I2CB pin is latched at power up. The operation mode effectively sets the function of the SEL0/SCL and SEL1/SDA pins. In Hardware Select (OUT0_SEL_I2CB pulled high) mode the two pins have the SEL0 and SEL1 function for selecting a preprogrammed configuration.

5. Operating Modes

The 5P49V60/6965/6975 can start-up in two different operating modes: **I^2C** mode or **Hardware Select** mode. The evaluation board is shipped with a “blank” 5P49V60/6965/6975 device and without configurations preprogrammed into OTP. Without configurations pre-programmed, the Hardware Select mode cannot be used. The blank device will start with a default or “test” configuration where output 0 and output 1 are enabled. Output 0 will be 25MHz and output 1 will be 100MHz with LVCMOSD logic. You can program a configuration into the device and into volatile registers with Timing Commander to test a configuration. This works without “burning” the permanent OTP memory and most users of this evaluation board will never burn OTP. In this way, the board can be used repeatedly to test configurations. Burning configurations into OTP is only useful when studying the Hardware Select mode and the transition from one configuration to another.

Important: Burning configurations into OTP is permanent and cannot be undone.

6. On-Board Crystal

The 5P49V60 and 5P49V6965 evaluation board comes installed with a 25MHz crystal. If the evaluation board is assembled with a 5P49V6975, no crystal is assembled because the crystal is integrated in the device. The crystal pins on the 5P49V6975 are NC (not connected).

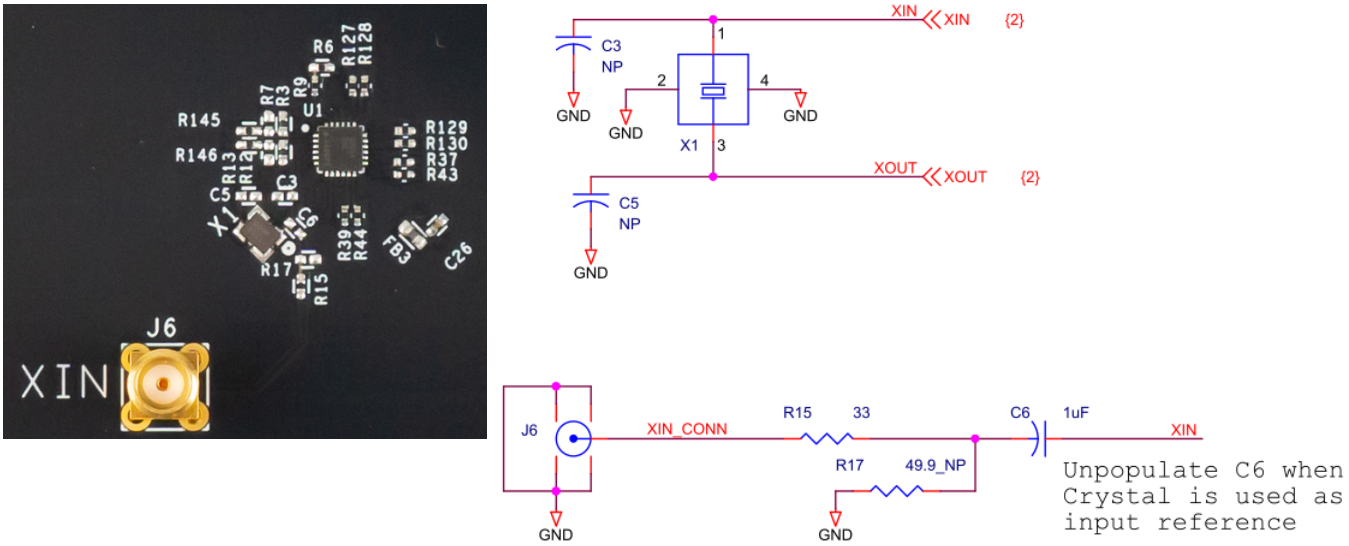


Figure 6. Crystal Circuit

The board is shipped with a small 25MHz SMD crystal installed. The crystal can be replaced with a different frequency if needed.

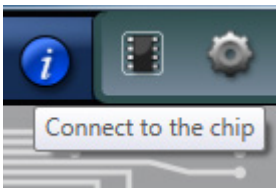
Note: Output 1 with the default or “test” mode will only work when using a 25MHz crystal.

Another useful modification can be to remove the 25MHz crystal and assemble C6 to connect the SMA connector J6. Now a clock from a generator or other source can be used to drive the XIN pin. Also assemble R17 when termination of the external clock is needed. For XIN amplitude requirements, refer to the device datasheet. The amplitude on XIN should not exceed 1.2Vpp and Renesas recommends using 1.0Vpp for most tests. When doing phase noise measurements of the output clocks, use an extremely low noise clock for XIN. The best phase noise at the outputs is achieved when using a crystal. Only the best of low noise RF signal generators connected to XIN can result in the same phase noise performance.

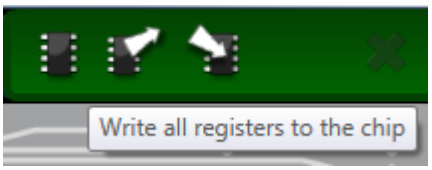
7. Configuration and Setup

Use the following steps to setup the board using I^2C and to start the configuration of the board.

1. Ensure no jumper on JP24 MODE; select I^2C mode. Add jumpers for SEL0_SCL and SEL1_SDA on JP24 for I^2C pull-ups.
2. Connect J18 to a USB port of the PC using the supplied I^2C cable.
3. Launch VersaClock 6E Timing Commander Software (refer to VersaClock 6E Timing Commander User Guide)
4. Following the Getting Started steps in the Timing Commander software. An I^2C connection is established between the GUI software and the VersaClock 6E chip.
5. Select “Open Settings File” if you have existing settings, or “New Settings File” and select 5P49V60, 5P49V6965 or 5P49V6975 depending on your evaluation board. In the same screen, browse for a personality file to be used with the evaluation board by clicking on the button at the bottom right.
6. Click on the gear icon and ensure that the correct connection type is selected (on-board I^2C via the FTDI interface or Aardvark via the 10-pin header JP1). Connect to the EVB by clicking on the microchip icon located at the top right of the Timing Commander screen.



7. Once connected, new options will be available on a green background indicating that the EVB has successfully connected with the board. Write settings to the chip by clicking on the write all registers to the chip option.



8. All intended outputs should now be available for measurement.

8. Board Schematics

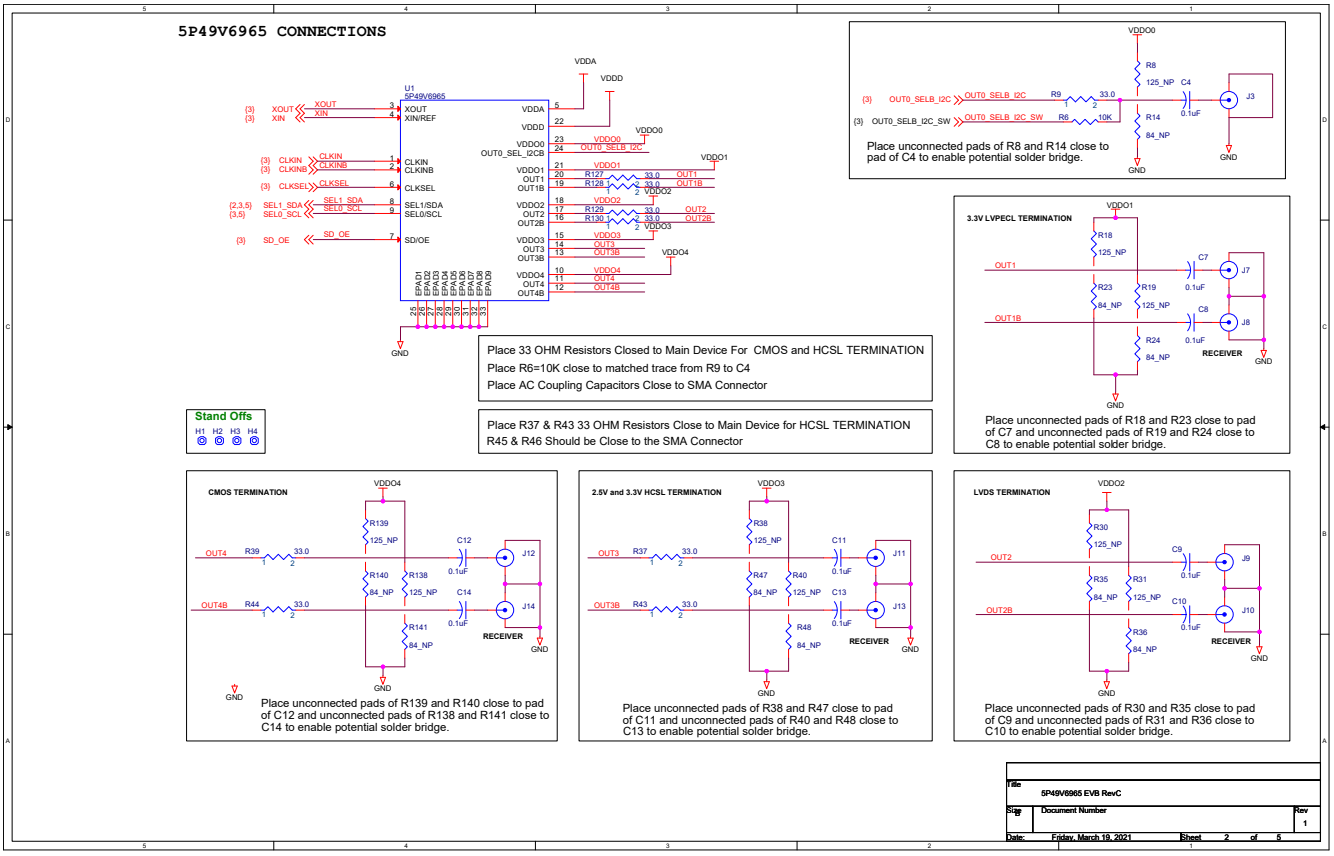


Figure 7. Evaluation Board Schematics – Page 1

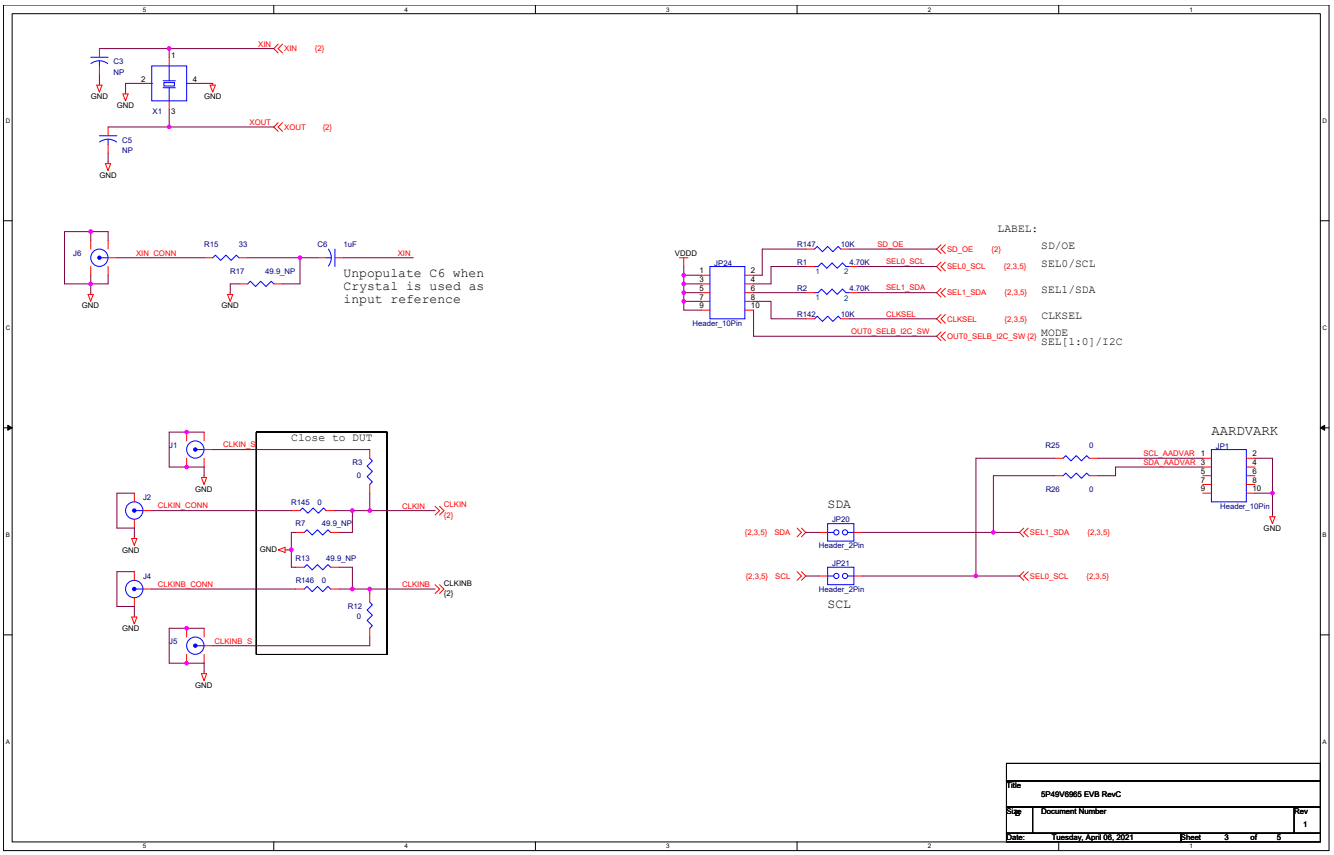


Figure 8. Evaluation Board Schematics – Page 2

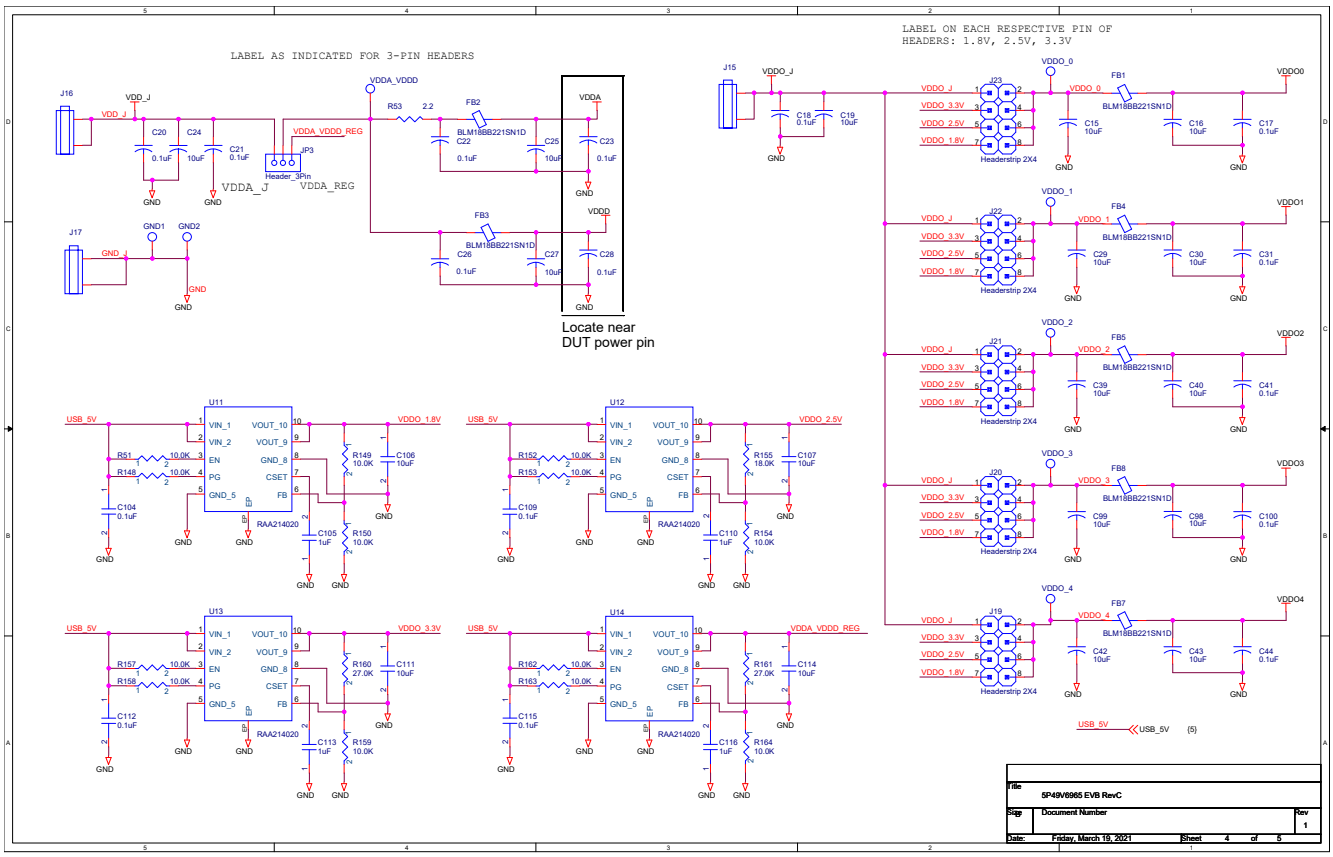


Figure 9. Evaluation Board Schematics – Page 3

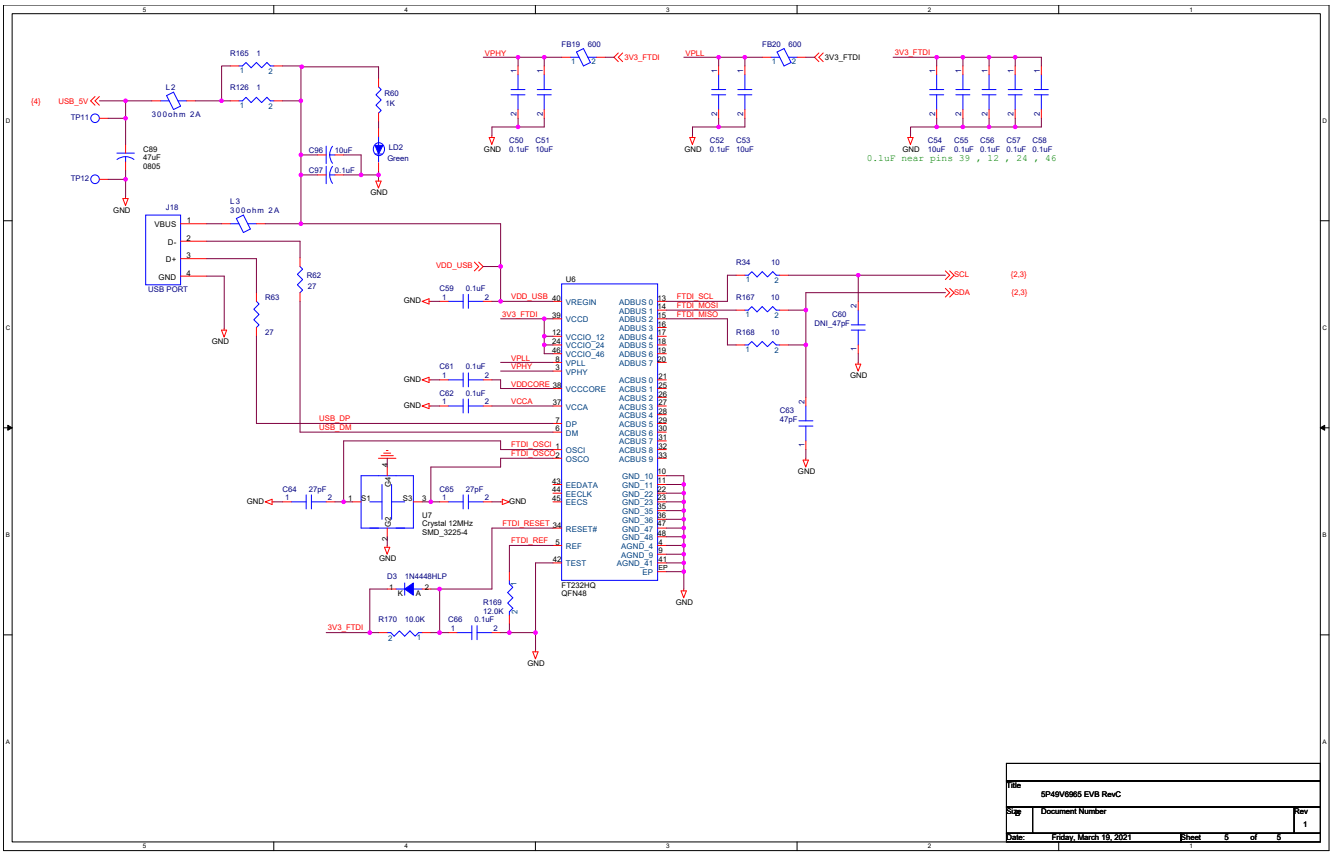


Figure 10. Evaluation Board Schematics – Page 4

9. Signal Termination Options

Termination options for OUT1–4 for the evaluation board are displayed in Figure 11. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not-populating) some resistors. DC or AC coupling of these outputs is also supported.

Table 3 through Table 6 tabulate component installations to support LVPECL, HCSL, LVCMOS and LVDS signal types for OUT1–4 on the device's EVB. Note that by doing so, the output signals will be measured and terminated by test equipment with a 50Ω internal termination.

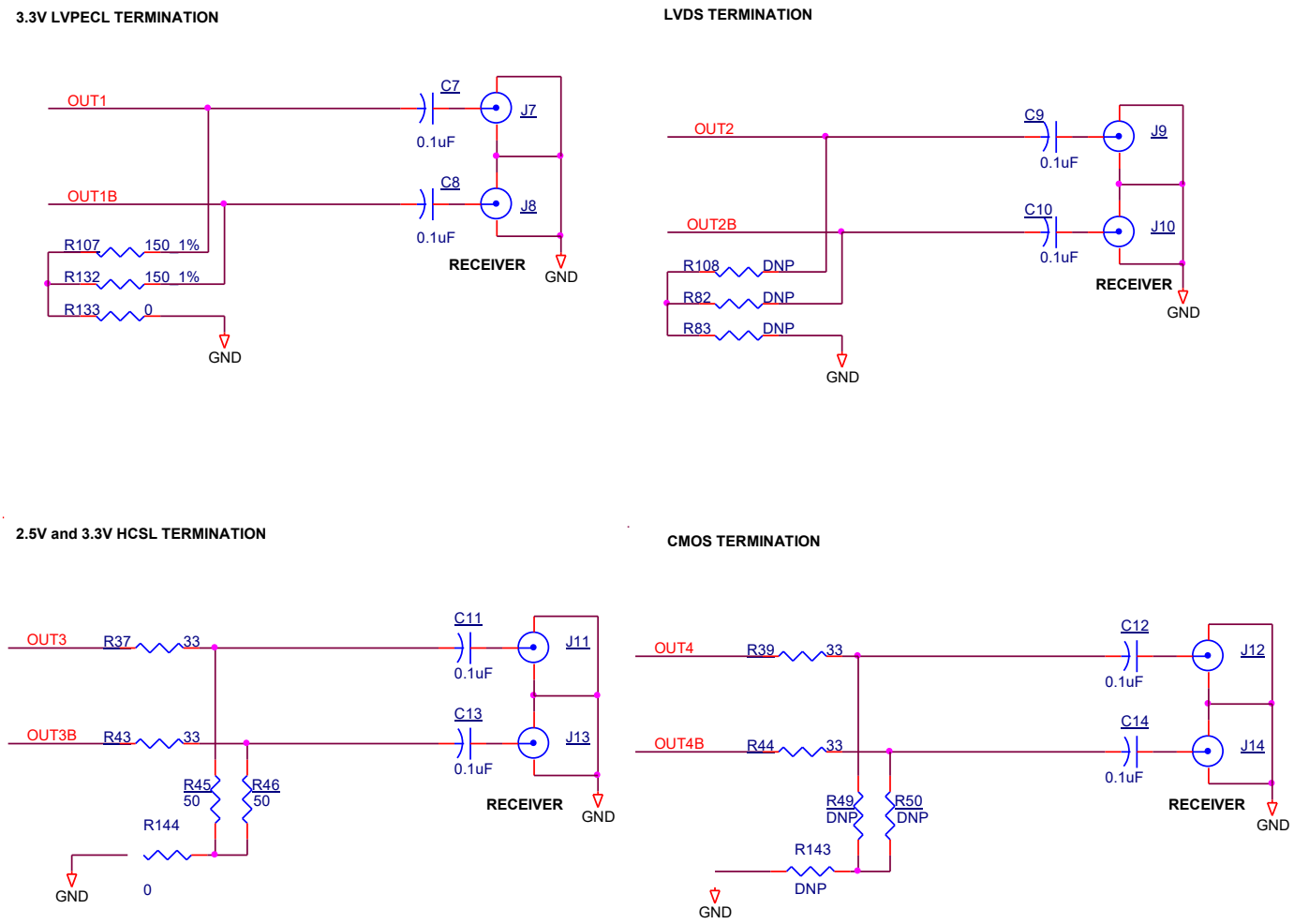


Figure 11. Output Termination Options

Table 3. Termination Options for OUT1

Signal Type	Series Resistors: R127, R128	150Ω Pull-down: R107, R132, R133	Series Capacitor: C7, C8
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

Table 4. Termination Options for OUT2

Signal Type	Series Resistors: R129, R130	150Ω Pull-down: R108, R82, R83	Series Capacitor: C9, C10
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

Table 5. Termination Options for OUT3

Signal Type	Series Resistors: R37, R43	150Ω Pull-down: R45, R46, R144	Series Capacitor: C11, C13
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

Table 6. Termination Options for OUT4

Signal Type	Series Resistors: R39, R44	150Ω Pull-down: R49, R50, R143	Series Capacitor: C12, C14
LVPECL	0Ω	Installed (see Figure 11)	0.1µF
HCSL	33Ω	Not installed	0Ω (short)
LVCMOS	33Ω	Not installed	0.1µF
LVDS	0Ω	Not installed	0.1µF

10. Ordering Information

Part Number	Description
5P49V60-EVK	5P49V60 Evaluation Board
5P49V6965-EVK	5P49V6965 Evaluation Board
5P49V6975-EVK	5P49V6975 Evaluation Board

11. Revision History

Revision	Date	Description
1.02	Dec 18, 2023	▪ Updated board images and schematics. ▪ Updated to the latest document template.
-	Feb 12, 2018	Added references to 5P49V60.
-	Dec 15, 2017	Initial release.

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