BROADCOM®

Data Sheet

HCPL-4504/J454/0454, HCNW4504

High CMR, High-Speed Optocouplers

Description

The Broadcom® HCPL-4504 and HCPL-0454 contain a GaAsP LED while the Broadcom HCPL-J454 and HCNW4504 contain an AlGaAs LED. The LED is optically coupled to an integrated high-gain photodetector.

The HCPL-4504 series has short propagation delays and high CTR. The HCPL-4504 series also has a guaranteed propagation delay difference ($t_{PLH} - t_{PHL}$). These features make the HCPL-4504 series an excellent solution to IPM inverter dead time and other switching problems. The CTR, propagation delay, and CMR are specified both for TTL and IPM conditions, which are provided for ease of application. These single channel, diode-transistor optocouplers are available in 8-Pin DIP, SO-8, and Widebody package configurations. An insulating layer between an LED and an integrated photodetector provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base collector capacitance.

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD.

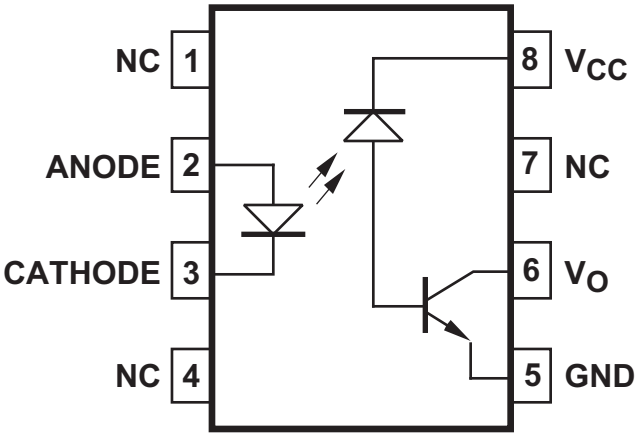
Features

- Short propagation delays for TTL and IPM applications
- 15 kV/µs minimum common mode transient immunity at V_{CM} = 1500V for TTL/load drive
- High CTR at T_A = 25°C
  - >25% for HCPL-4504/0454
  - >23% for HCNW4504
  - >19% for HCPL-J454
- Electrical specifications for common IPM applications
- TTL compatible
- Open collector output
- Safety approval:
  - UL recognized
    - 3750 Vrms/1 min. for HCPL-4504/0454/J454
    - 5000 Vrms/1 min. for HCPL-4504 Option 020 and HCNW4504
  - CSA approved
  - IEC/EN/DIN EN 60747-5-2 approved
    - V_{IORM} = 560 Vpeak for HCPL-0454 Option 060
    - V_{IORM} = 630 Vpeak for HCPL-4504 Option 060
    - V_{IORM} = 891 Vpeak for HCPL-J454
    - V_{IORM} = 1414 Vpeak for HCNW4504

Applications

- Inverter circuits and Intelligent Power Module (IPM) interfacing: high common mode transient immunity (> 10 kV/µs for an IPM load/drive) and ($t_{PLH} - t_{PHL}$) specified (see Power Inverter Dead Time and Propagation Delay Specifications)
- Line receivers: Short propagation delays and low input-output capacitance
- High-speed logic ground isolation: TTL/TTL, TTL/CMOS, TTL/LSTTL
- Replaces pulse transformers: Saves board space and weight
- Analog signal ground isolation: Integrated photodetector provides improved linearity over phototransistors

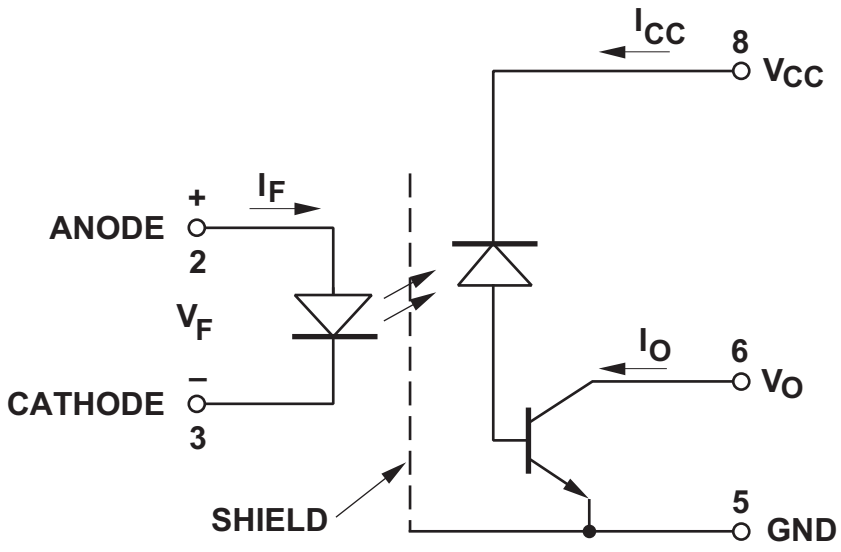
Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

Schematic



Ordering Information

HCPL-0454, HCPL-4504 and HCPL-J454 are UL Recognized with 3750 Vrms for 1 minute per UL1577.

HCNW4504 is UL Recognized with 5000 Vrms for 1 minute per UL1577. HCPL-0454, HCPL-4504, HCPL-J454 and HCNW4504 are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape and Reel	UL 1577 5000 Vrms/1 Minute Rating	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	Non-RoHS Compliant							
HCPL-4504	-000E	no option	300-mil DIP 8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-J454	-000E	no option	300-mil DIP 8					X	50 per tube
	-300E	#300		X	X			X	50 per tube
	-400E	N/A		X	X			X	50 per tube
	-500E	#500		X	X	X		X	1000 per reel
	-600E	N/A		X	X	X		X	750 per reel
HCPL-0454	-000E	no option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	#560		X		X		X	1500 per reel
HCNW4504	-000E	no option	400-mil Widebody DIP-8				X	X	42 per tube
	-300E	#300		X	X		X	X	42 per tube
	-500E	#500		X	X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-4504-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval and RoHS compliant.

Example 2:

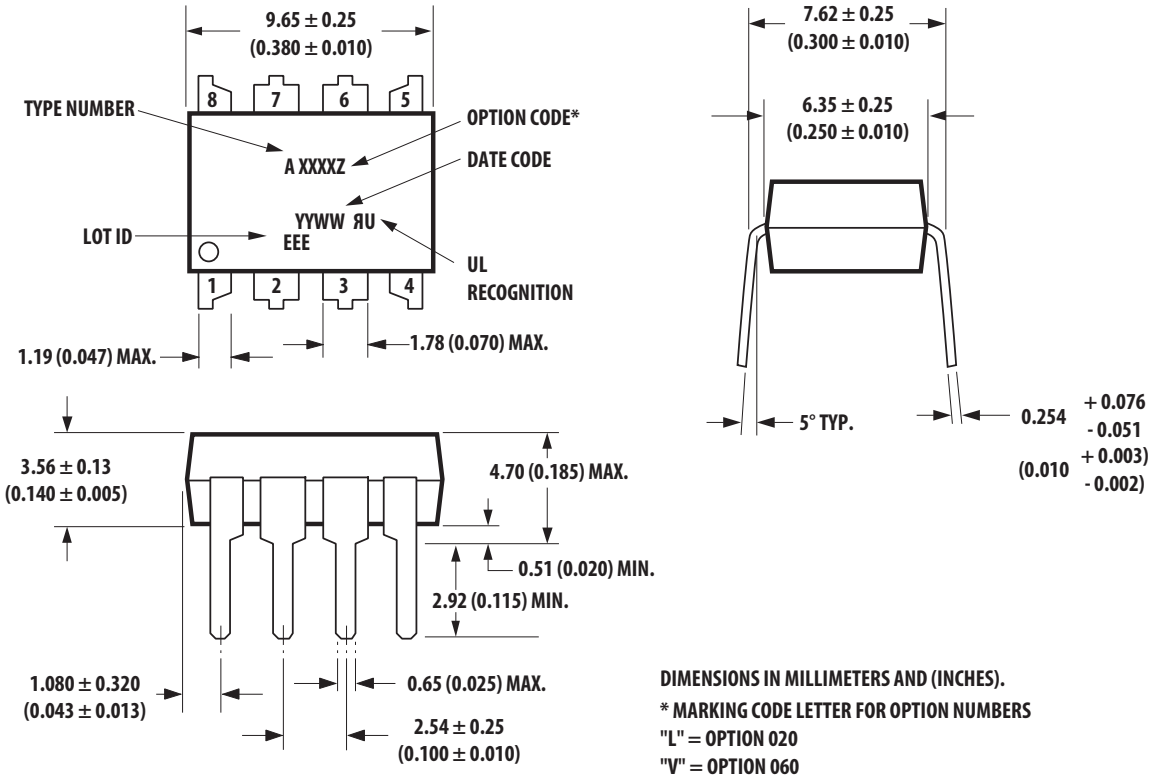
HCPL-4504 to order product of 300-mil DIP package in Tube packaging and non RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

NOTE: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '-XXXE.'

Package Outline Drawings

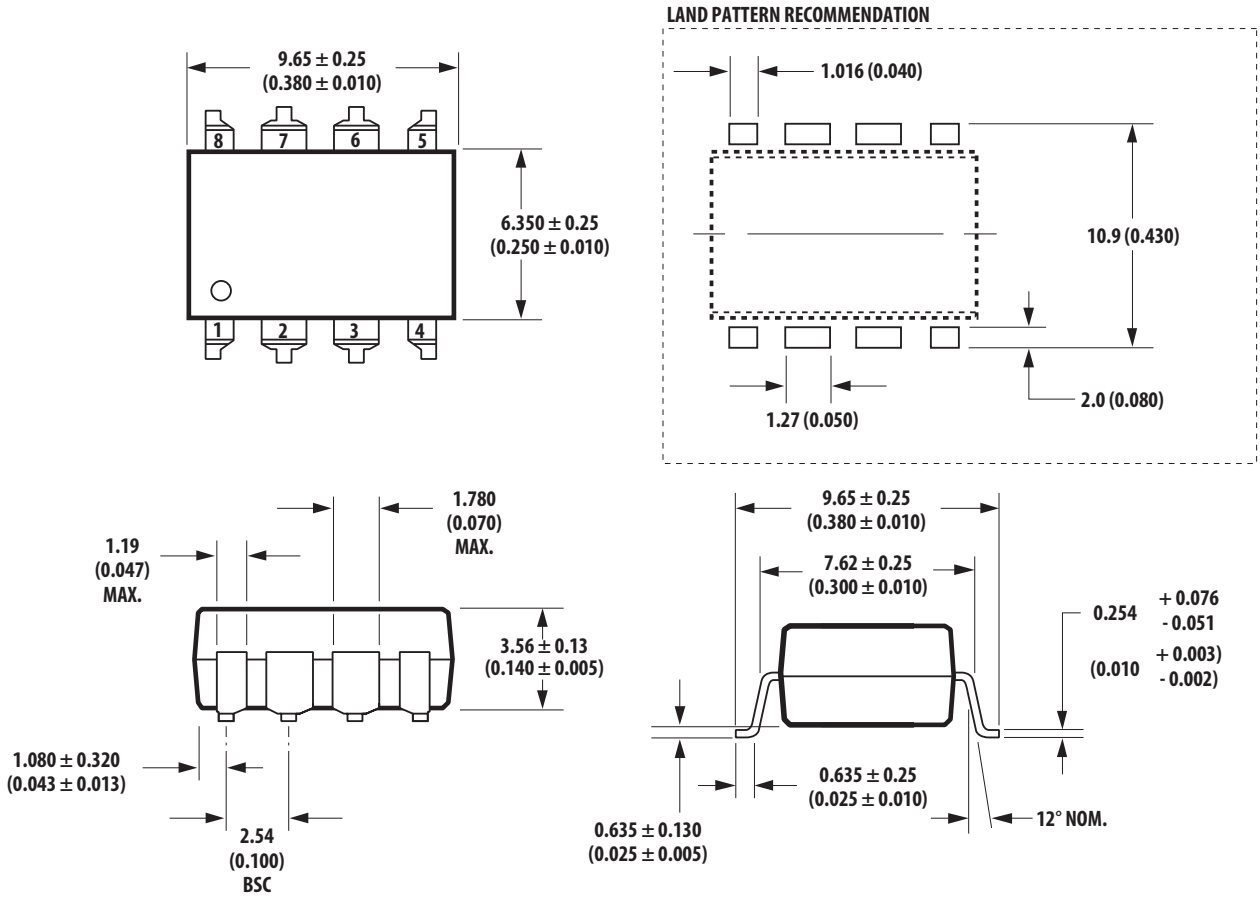
HCPL-4504 Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).
*** MARKING CODE LETTER FOR OPTION NUMBERS**
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCPL-4504 Gull Wing Surface Mount Option 300 Outline Drawing

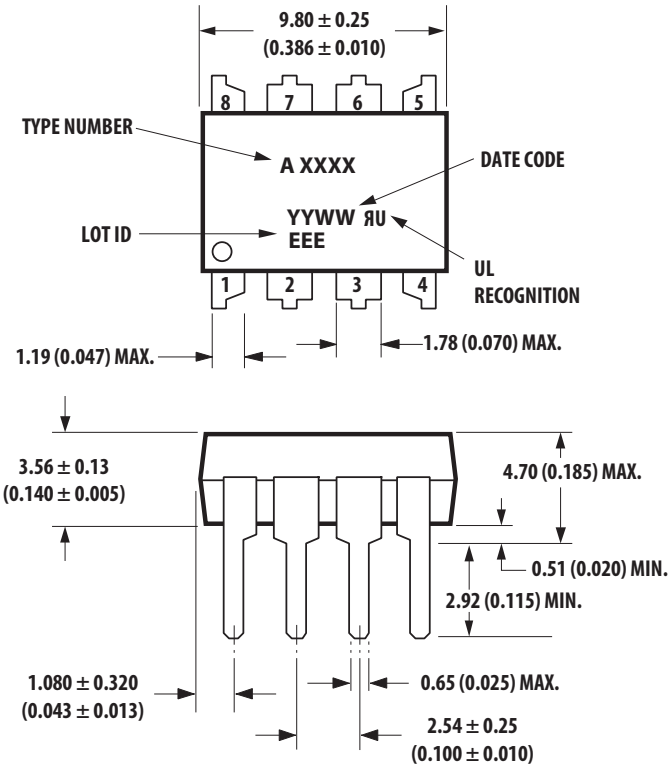


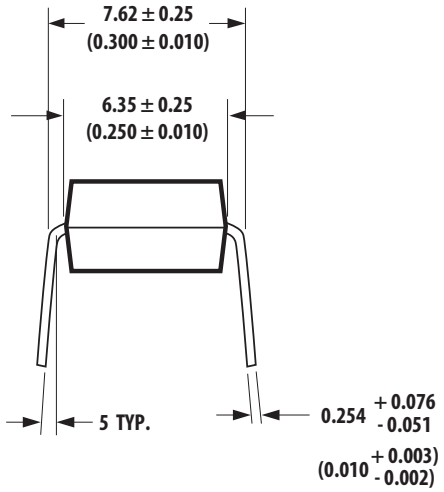
DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCPL-J454 Outline Drawing



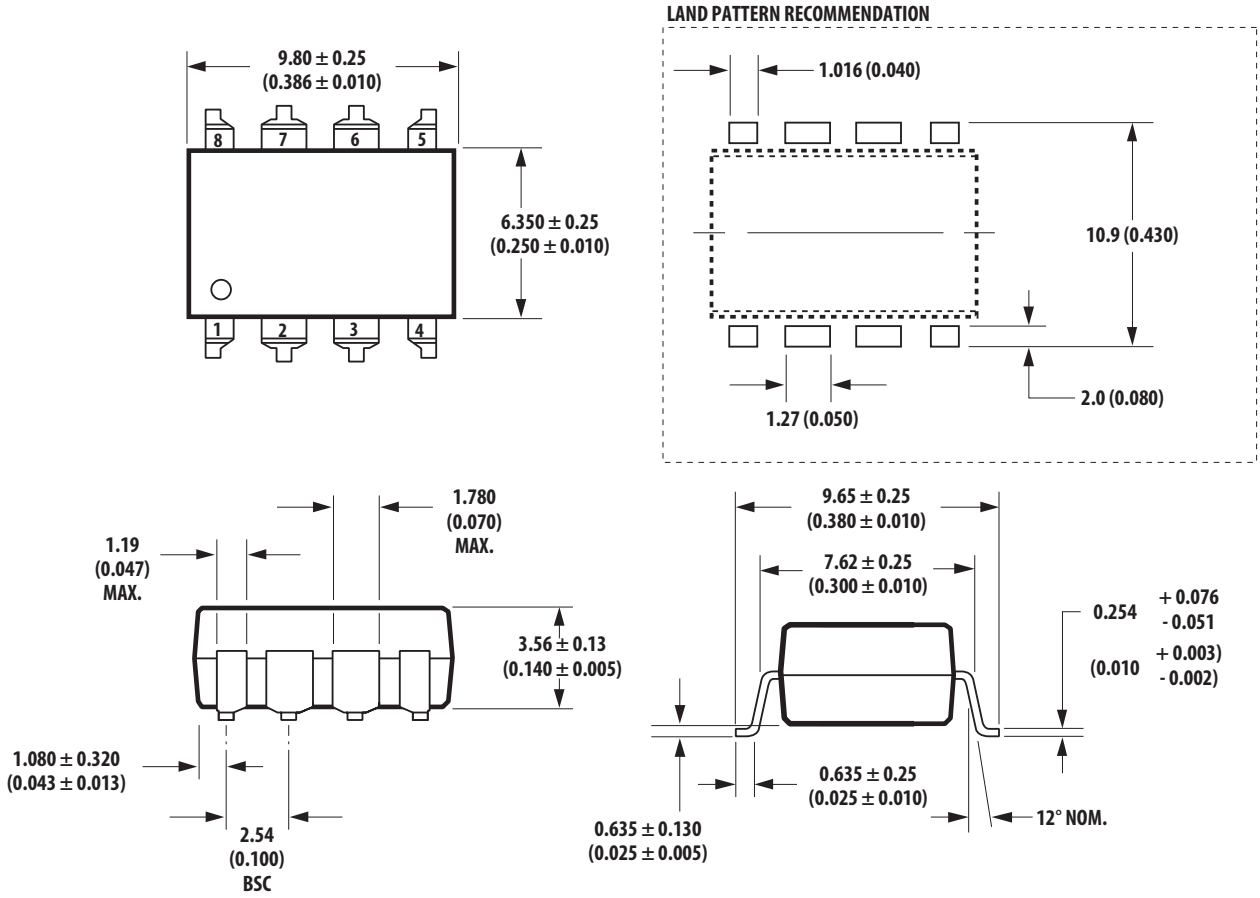


DIMENSIONS IN MILLIMETERS AND (INCHES).

OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

HCPL-J454 Gull Wing Surface Mount Option 300 Outline Drawing

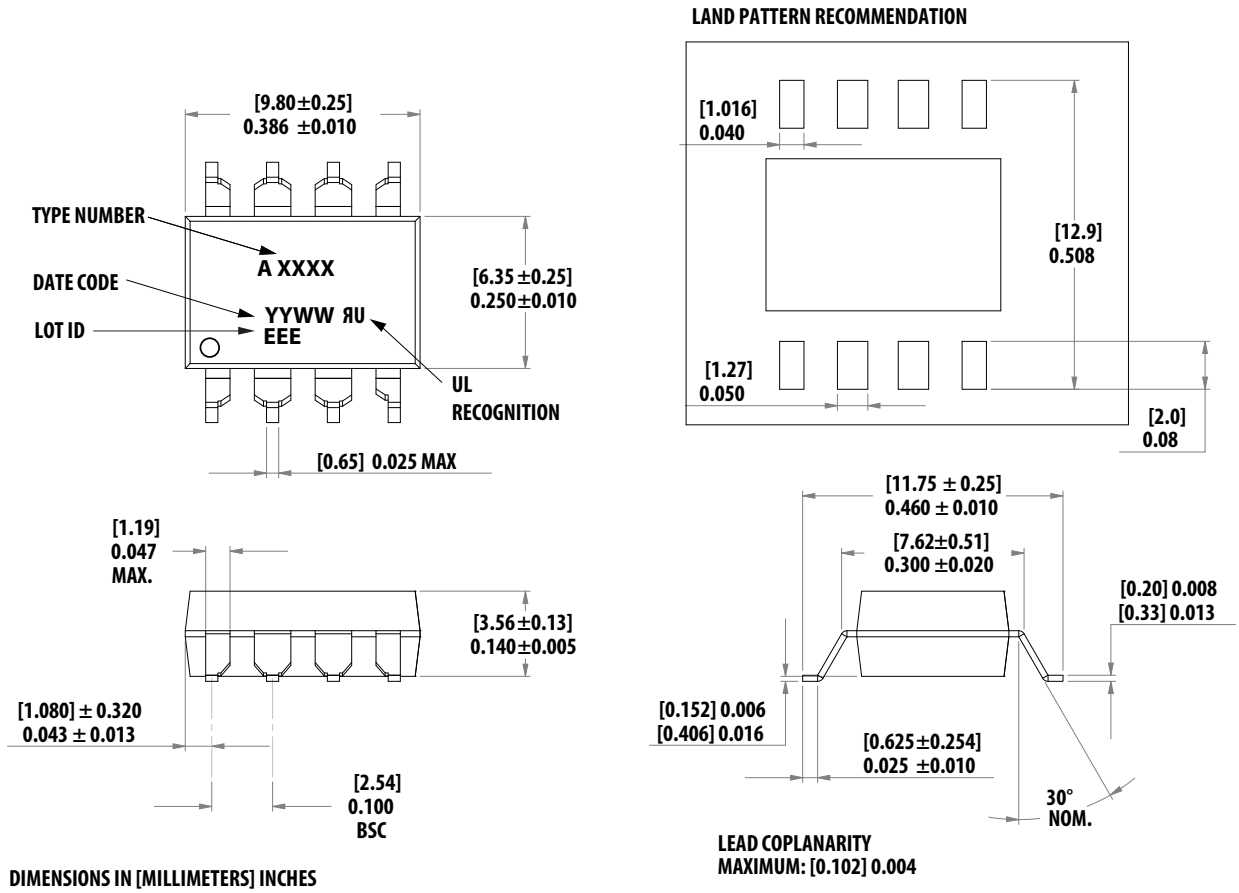


DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

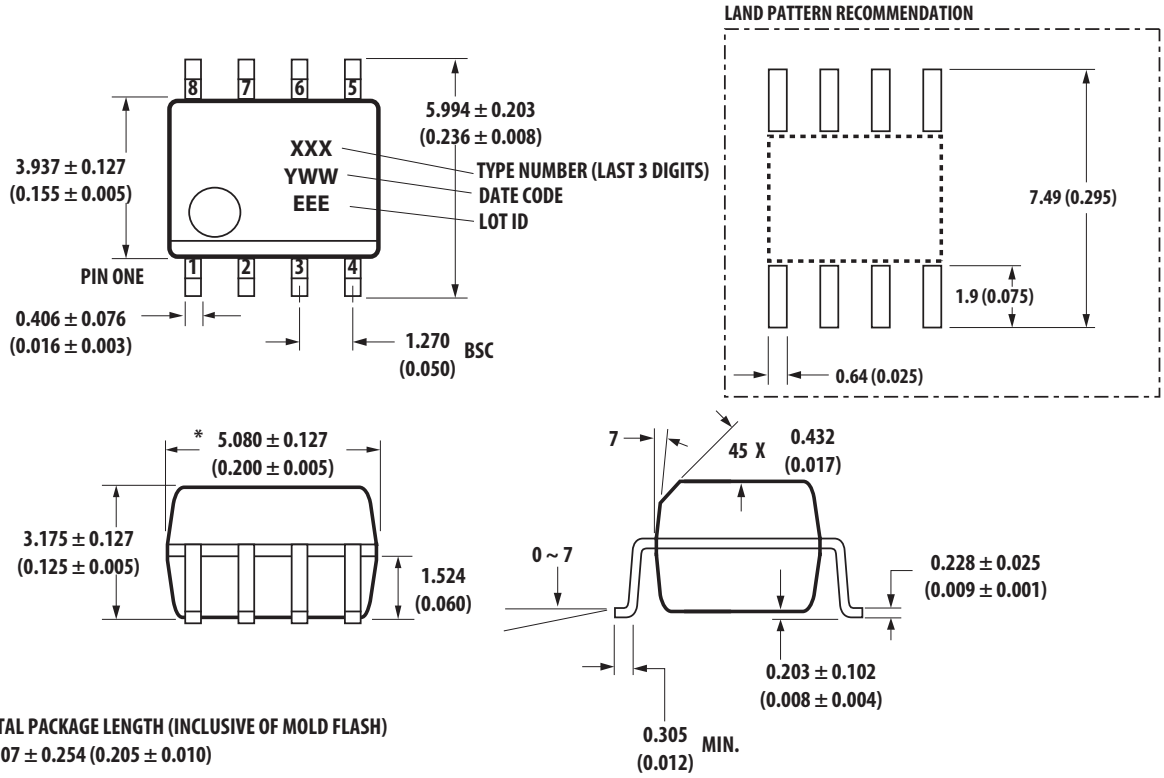
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

HCPL-J454-400E/600E Widelead Gullwing Surface Mount Outline Drawing



DIMENSIONS IN [MILLIMETERS] INCHES
OPTION NUMBERS 400 AND 600 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

HCPL-0454 Outline Drawing (8-Pin Small Outline Package)

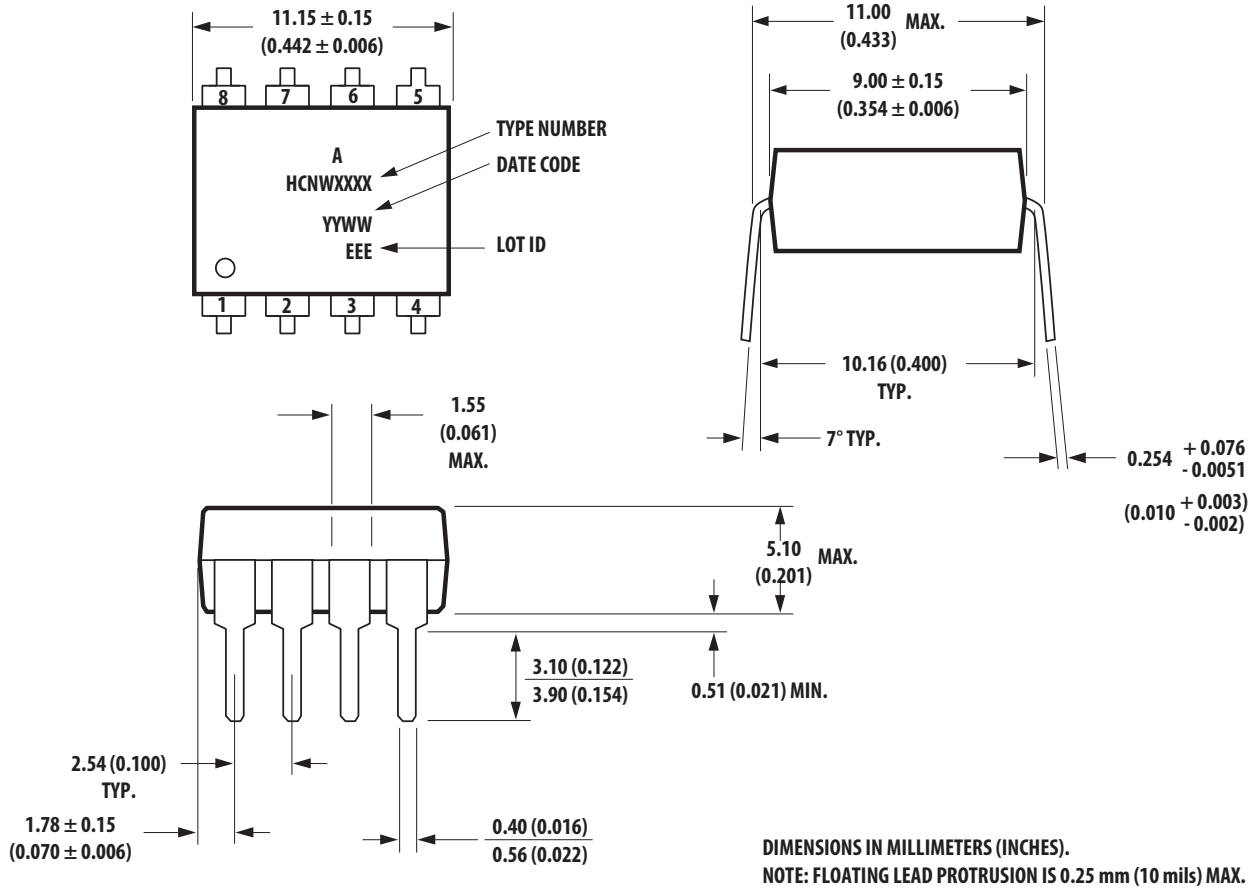


* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

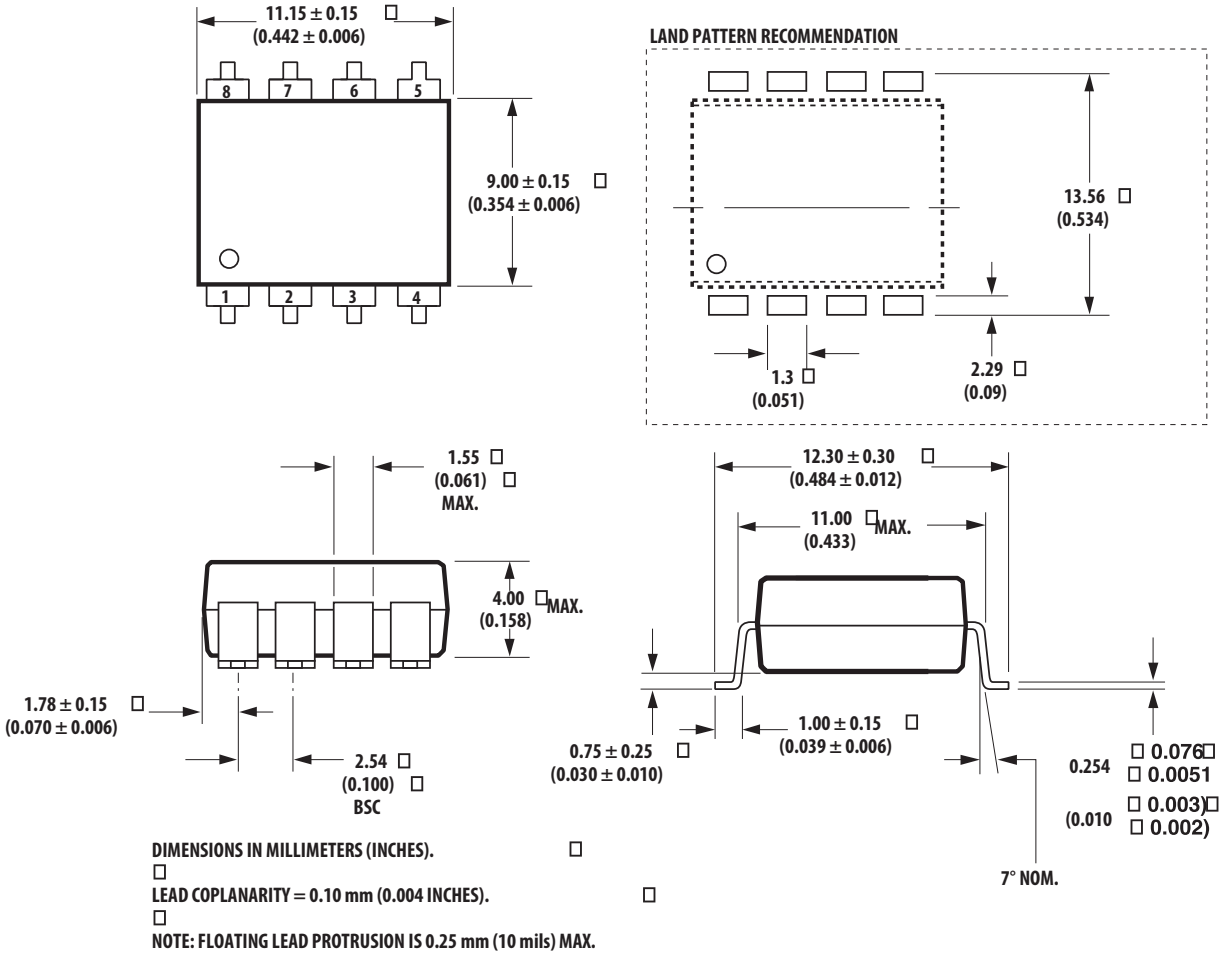
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

HCNW4504 Outline Drawing (8-Pin Widebody Package)



DIMENSIONS IN MILLIMETERS (INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCNW4504 Gull Wing Surface Mount Option 300 Outline Drawing

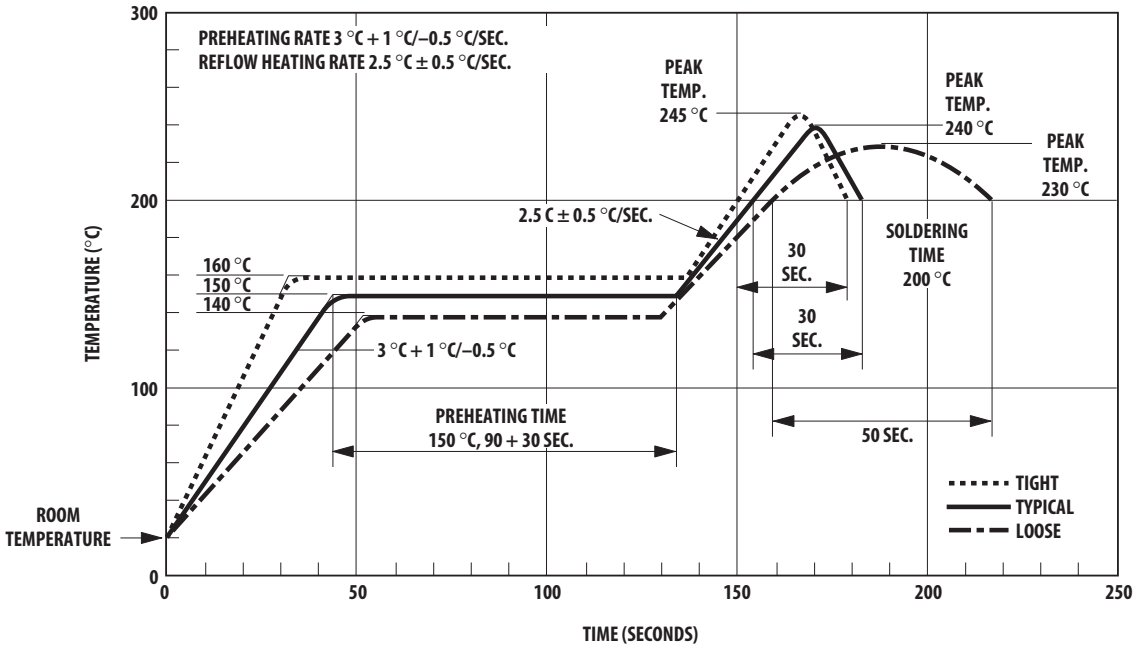


DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

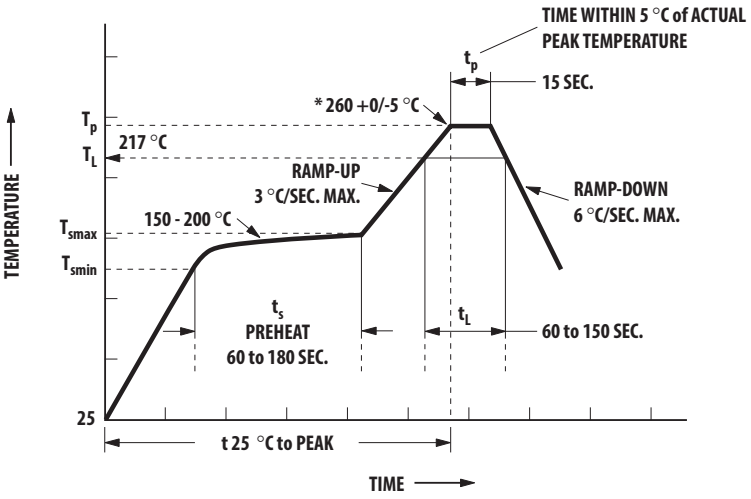
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Temperature Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

NOTE: NON-HALIDE FLUX SHOULD BE USED.

* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS 245 °C

Regulatory Information

The devices contained in this data sheet have been approved by the following agencies:

Agency/Standard		HCPL-4504	HCPL-J454	HCPL-0454	HCNW4504
Underwriters Laboratories (UL) Recognized under UL1577, Component Recognition Program, Category FPQU2, File E55361	UL1577	3750 Vrms /1 minute, Option 020 5000 Vrms/ 1 minute	3750 Vrms /1 minute	3750 Vrms/ 1 minute	5000 Vrms/ 1 minute
Canadian Standards Association (CSA) File CA88324	Component Acceptance Notice #5	3750 Vrms/ 1 minute, Option 020 5000 Vrms/ 1 minute	3750 Vrms /1 minute	3750 Vrms/ 1 minute	5000 Vrms/ 1 minute
IEC/EN/DIN EN 60747-5-2 Approved under: IEC 60747-5-2:1997 + A1:2002 EN 60747-5-2:2001 + A1:2002 DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01		Option 060 V_{IORM} = 630V peak	V_{IORM} = 891V peak	Option 060 V_{IORM} = 560V peak	V_{IORM} = 1414V peak

Insulation and Safety Related Specifications

Parameter	Symbol	Value					Units	Conditions
		HCPL-4504	HCPL- J454 -400E/-600E	HCPL-J454 All Other Options	HCPL-0454	HCNW 4504		
Minimum External Air Gap (External Clearance)	L(101)	7.1	8.0	7.4	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	8.0	8.0	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.8	0.5	0.5	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and the photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage		N/A	N/A	N/A	N/A	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 175	≥ 175	≥ 175	≥ 175	≥ 200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements.

However, when mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, consider the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads. There are techniques, such as grooves and ribs, that may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances also change depending on factors, such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics

Description	Symbol	HCPL-0454 Option 060	HCPL-4504 Option 060	HCPL-J454	HCNW4504	Units
Installation Classification per DIN VDE 0110/1.89, Table 1						
for rated mains voltage ≤150 Vrms		I-IV	I-IV	I-IV	I-IV	
for rated mains voltage ≤ 300 Vrms		I-III	I-IV	I-IV	I-IV	
for rated mains voltage ≤ 450 Vrms			I-III	I-III	I-IV	
for rated mains voltage ≤ 600 Vrms				I-III	I-IV	
for rated mains voltage ≤ 1000 Vrms					I-III	
Climatic Classification		55/100/21	55/100/21	55/100/21	55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	2	2	
Maximum Working Insulation Voltage	V_{IORM}	560	630	891	1414	Vpeak
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1s, Partial Discharge < 5 pC	V_{PR}	1050	1181	1670	2652	Vpeak
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test, t_m = 60s, Partial Discharge < 5 pC	V_{PR}	840	945	1336	2121	Vpeak
Highest Allowable Overvoltage[a] (Transient Overvoltage, t_{ini} = 10s)	V_{IOTM}	4000	6000	6000	8000	Vpeak
Safety Limiting Values – Maximum values allowed in the event of a failure, also see Thermal Derating curve						
Case Temperature	T_S	150	175	175	150	°C
Input Current	$I_{S,INPUT}$	150	230	400	400	mA
Output Power	$P_{S,OUTPUT}$	600	600	600	700	mW
Insulation Resistance at T_S, V_{IO} = 500V	RS	≥ 10^9	≥ 10^9	≥ 10^9	≥ 10^9	Ω

a. Refer to the optocoupler section of the Designer's Catalog, under regulatory information (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE:

- These optocouplers are suitable for “safe electrical isolation” only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.
- Insulation Characteristics are per IEC/EN/DIN EN 60747-5-2.
- Surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Notes
Storage Temperature	T_S		–55	125	°C	
Operating Temperature	T_A	HCPL-4504 HCPL-0454 HCPL-J454	–55	100	°C	
		HCNW4504	–55	85		
Average Forward Input Current	$I_{F(AVG)}$			25	mA	a
Peak Forward Input Current (50% duty cycle, 1-ms pulse width)	$I_{F(PEAK)}$	HCPL-4504 HCPL-0454	—	50	mA	b
		HCPL-J454 HCNW4504	—	40		
Peak Transient Input Current (≤ 1-µs pulse width, 300 pps)	$I_{F(TRANS)}$	HCPL-4504 HCPL-0454	—	1	A	
		HCPL-J454 HCNW4504	—	0.1		
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4504 HCPL-0454	—	5	V	
		HCPL-J454 HCNW4504	—	3		
Input Power Dissipation	P_{IN}	HCPL-4504 HCPL-0454	—	45	mW	c
		HCPL-J454 HCNW4504	—	40		
Average Output Current (Pin 6)	$I_{O(AVG)}$		—	8	mA	
Peak Output Current	$I_{O(PEAK)}$		—	16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		–0.5	30	V	
Output Voltage (Pin 6-5)	V_O		–0.5	20	V	
Output Power Dissipation	PO		—	100	mW	d
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10s	T_{LS}	HCPL-4504 HCPL-J454	—	260	°C	
Up to seating plane, 10s		HCNW4504	—	260		
Reflow Temperature Profile	T_{RP}	HCPL-4504 Option 300, Option 500, Option 400E, and Option 600E	See Package Outline Drawings			

a. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C (SO-8).

b. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C (SO-8).

c. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C (SO-8).

d. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (8-Pin DIP).
Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C (SO-8).

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 12.

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Units	Test Conditions			Figure	Notes
Current Transfer Ratio	CTR	HCPL-4504 HCPL-0454	25	32	60	%	T_A = 25°C	V_O = 0.4V	I_F = 16 mA, V_{CC} = 4.5V	1, 2, 4	b
			21	34	—			VO = 0.5V			
		HCPL-J454	19	37	60		T_A = 25°C	VO = 0.4V			
			13	39	—			VO = 0.5V			
		HCNW4504	23	29	60		T_A = 25°C	V_O = 0.4V			
			19	31	63			V_O = 0.5V			
Current Transfer Ratio	CTR	HCPL-4504 HCPL-0454	26	35	65	%	T_A = 25°C	V_O = 0.4V	I_F = 12 mA, V_{CC} = 4.5V	1, 2, 4	b
			22	37	—			V_O = 0.5V			
		HCPL-J454	21	43	65		T_A = 25°C	V_O = 0.4V			
			16	45	—			V_O = 0.5V			
		HCNW4504	25	33	65		T_A = 25°C	V_O = 0.4V			
			21	35	68		VO = 0.5V				
Logic Low Output Voltage	V_{OL}	HCPL-4504 HCPL-0454	—	0.2	0.4	V	T_A = 25°C	I_O = 4.0 mA	I_F = 16 mA, V_{CC} = 4.5V		
			—		0.5			I_O = 3.3 mA			
		HCPL-J454	—	0.2	0.4		T_A = 25°C	I_O = 3.6 mA			
			—	0.5	—			I_O = 3.0 mA			
		HCNW4504	—	0.2	0.4		T_A = 25°C	I_O = 3.6 mA			
			—	0.5	—			I_O = 3.0 mA			
Logic High Output Current	I_{OH}		—	0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5V, I_F = 0 mA		5	
			—	0.01	1		T_A = 25°C	V_O = V_{CC} = 15V			
			—	—	50						
Logic Low Supply Current	I_{CCL}	HCPL-4504 HCPL-0454 HCNW4504	—	50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15V			12	
		HCPL-J454	—	—	70						
Logic High Supply Current	I_{CCH}		—	0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_O = Open		12	
			—	—	2			V_{CC} = 15V			
Input Forward Voltage	V_F	HCPL-4504 HCPL-0454	—	1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
			—	—	1.8						
		HCPL-J454 HCNW4504	1.45	1.59	1.85		T_A = 25°C	I_F = 16mA			
			1.35		1.95						
Input Reverse Breakdown Voltage	BV_R	HCPL-4504 HCPL-0454	5			V	I_R = 10 µA				
		HCPL-J454 HCNW4504	3				I_R = 100 µA				

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Units	Test Conditions	Figure	Notes
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	HCPL-4504 HCPL-0454	—	–1.6		mV/°C	I_F = 16 mA		
		HCPL-J454 HCNW4504	—	–1.4					
Input Capacitance	C_{IN}	HCPL-4504 HCPL-0454	—	60	—	pF	f = 1 MHz, V_F = 0V		
		HCPL-J454 HCNW4504	—	—	70				

a. All typicals at T_A = 25°C.

b. Current Transfer Ratio in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.

AC Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Units	Test Conditions		Figure	Notes
Propagation Delay Time to Logic Low at Output	t_{PHL}		—	0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	6, 8. 9	b
			—	0.2	0.5					
	t_{PHL}		0.2	0.5	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5V	6, 10, 11, 12, 13, 14	c
		HCPL-J454	0.05		1.0					
		Others	0.1							
Propagation Time to Logic High at Output Delay	t_{PLH}		—	0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THLH} = 1.5V	6. 8. 9	b
			—	0.3	0.7					
	t_{PLH}		0.3	0.8	1.1	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0V, R_L = 20 kΩ, C_L = 100 pF, V_{THLH} = 2.0 V	6, 10, 11, 12, 13, 14	c
			0.2	0.8	1.4					
Propagation Delay Difference Between Any 2 Parts	t_{PLH} – t_{PHL}		–0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	6, 10, 11, 12, 13, 14	d
			–0.7	0.3	1.3					
Common Mode Transient Immunity at Logic High	$\|CM_H\|$		15	30	—	kV/µs	TA = 25°C, VCM = 1500 V_{P-P}	V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 0 mA	7	b, e
	$\|CM_H\|$		15	30	—	kV/µs		V_{CC} = 15.0V, R_L = 20 kΩ, C_L = 100 pF, I_F = 0 mA	7	c, f
Level Output Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$		15	30	—	kV/µs	T_A = 25°C, V_{CM} = 1500 V_{P-P}	V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 16 mA	7	b, e
	$\|CM_L\|$	HCPL-J454	15	30	—	kV/µs		V_{CC} = 15.0V, R_L = 20 kΩ, C_L = 100 pF, I_F = 12 mA	7	c, f
		Others	10	—	—					
	$\|CM_L\|$		15	30	—	kV/µs		V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 16 mA	7	c, f

a. All typicals at T_A = 25°C.

b. The 1.9-kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6-kΩ pull-up resistor.

c. The R_L = 20 kΩ, C_L = 100 pF load represents an Intelligent Power Module (IPM) load.

d. The difference between t_{PLH} and t_{PHL} between any two devices (same part number) under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications.)

e. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (that is, V_O > 2.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to ensure that the output will remain in a Logic Low state (that is, V_O < 0.8 V).

f. Under Intelligent Power Module (IPM) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to ensure that the output will remain in a Logic High state (that is, V_O > 3.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to ensure that the output will remain in a Logic Low state (that is, V_O < 1.0V).

Package Characteristics

Over recommended temperature (T_A = 0°C to 25°C) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Units	Test Conditions	Figure	Notes
Input-Output Momentary Withstand Voltage[b]	V_{ISO}	HCPL-4504	3750	—	—	V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		c, d, e
		HCPL-0454							
		HCPL-J454	3750						c, e, f
		HCPL-4504 Option 020	5000						c, g, h
		HCNW4504	5000						c, e, h
Input-Output Resistance	R_{I-O}	HCPL-4504 HCPL-0454 HCPL-J454	—	10^{12}	—	Ω	V_{I-O} = 500 Vdc		c
		HCNW4504	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}	HCPL-4504 HCPL-0454	—	0.6	—	pF	f = 1 MHz		c
		HCPL-J454		0.8					
		HCNW4504		0.5	0.6				

a. All typicals at T_A = 25°C.

b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or Broadcom Application Note 1074, “Optocoupler Input-Output Endurance Voltage.”

c. The device is considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

d. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).

e. This test is performed before the 100% production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.

f. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).

g. Refer to the Option 020 data sheet for more information.

h. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (leakage detection current limit, I_{I-O} ≤ 5 µA).

Figure 1: DC and Pulsed Transfer Characteristics

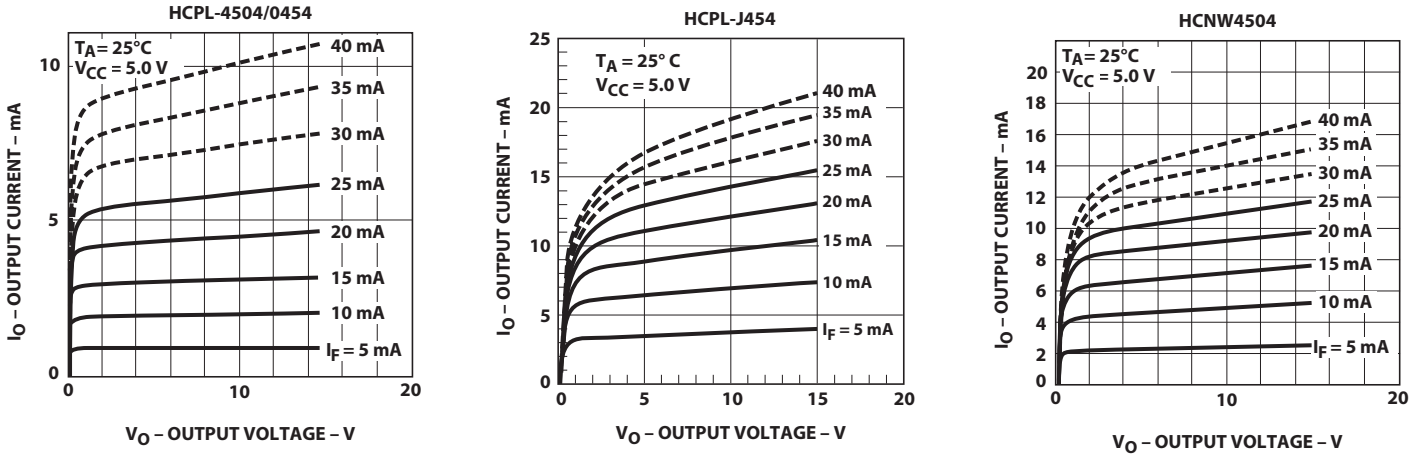


Figure 2: Current Transfer Ratio vs. Input Current

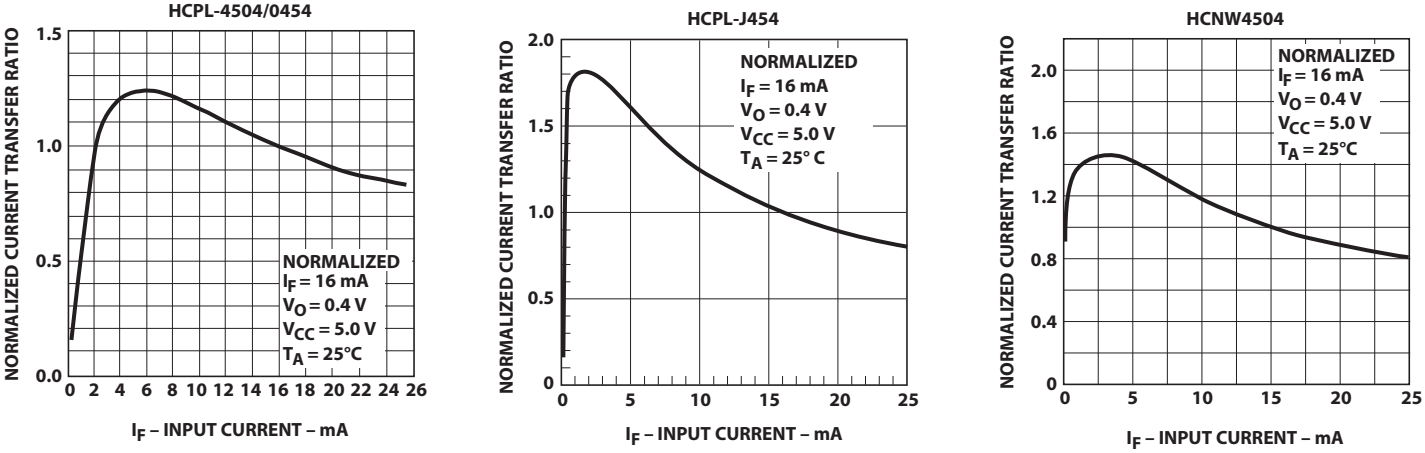


Figure 3: Input Current vs. Forward Voltage

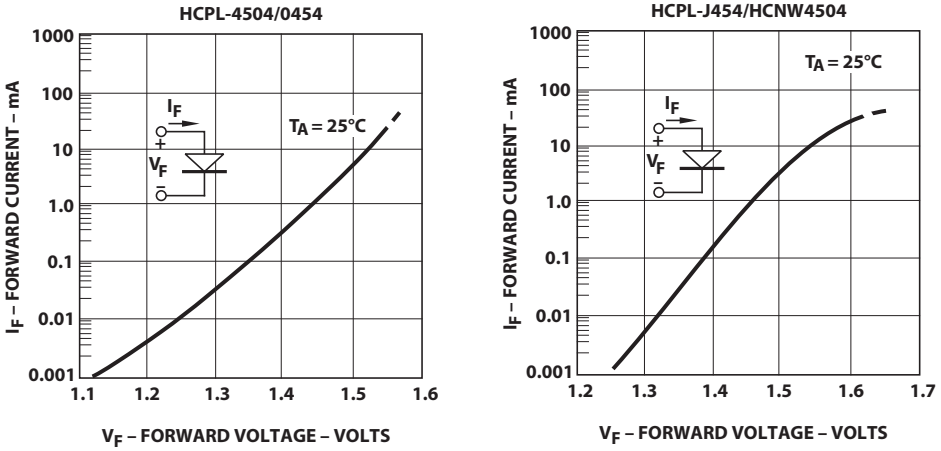


Figure 4: Current Transfer Ratio vs. Temperature

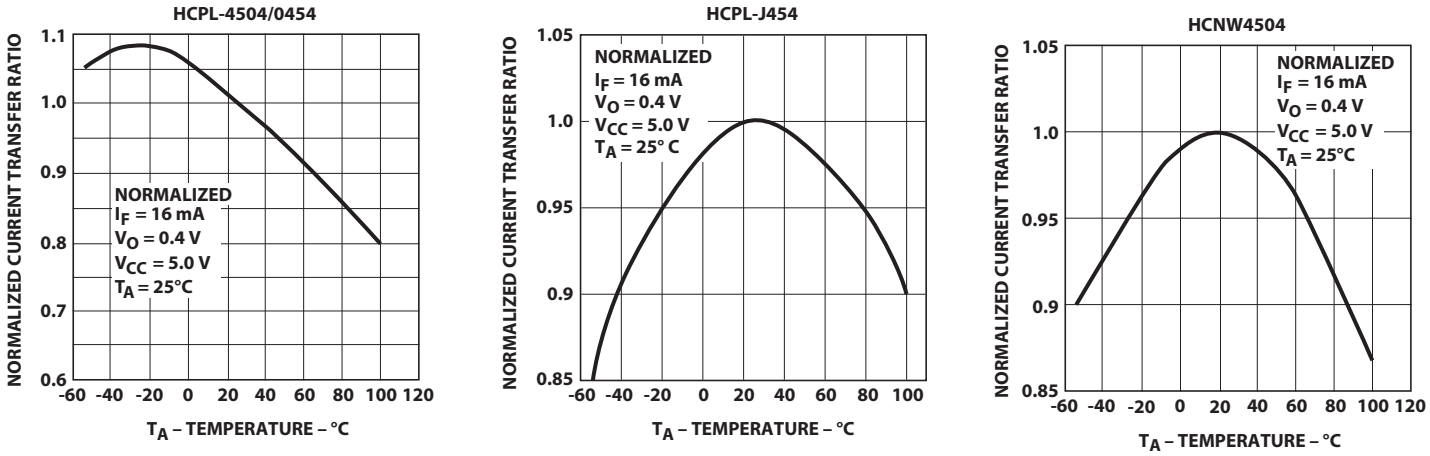


Figure 5: Logic High Output Current vs. Temperature

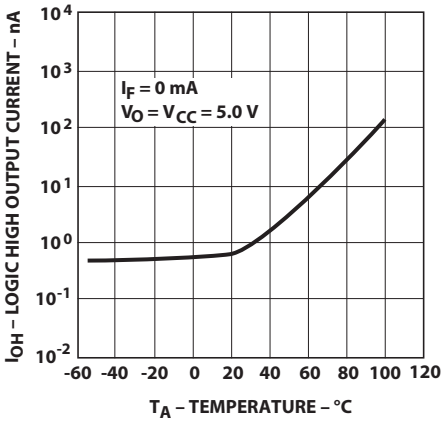


Figure 6: Switching Test Circuit

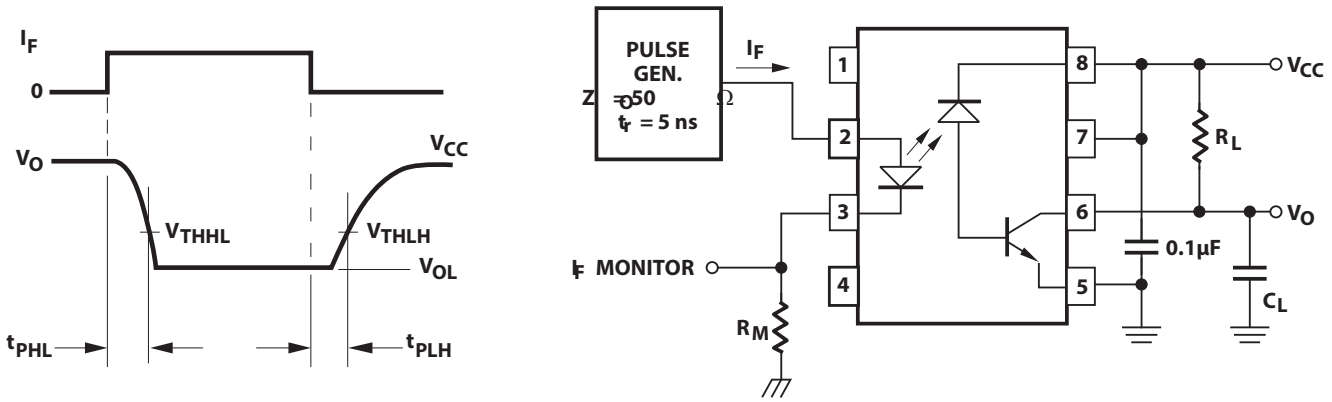


Figure 7: Test Circuit for Transient Immunity and Typical Waveforms

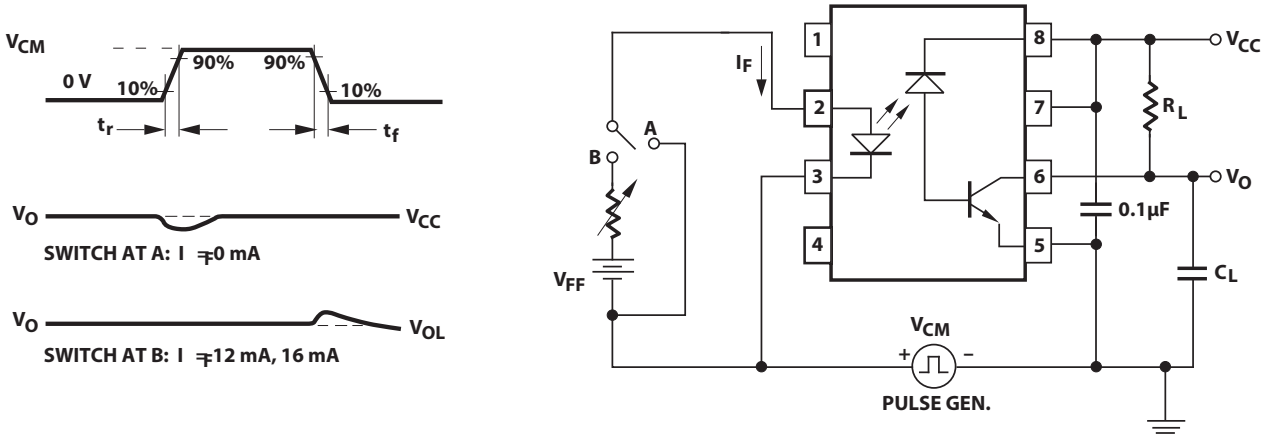


Figure 8: Propagation Delay Time vs. Temperature

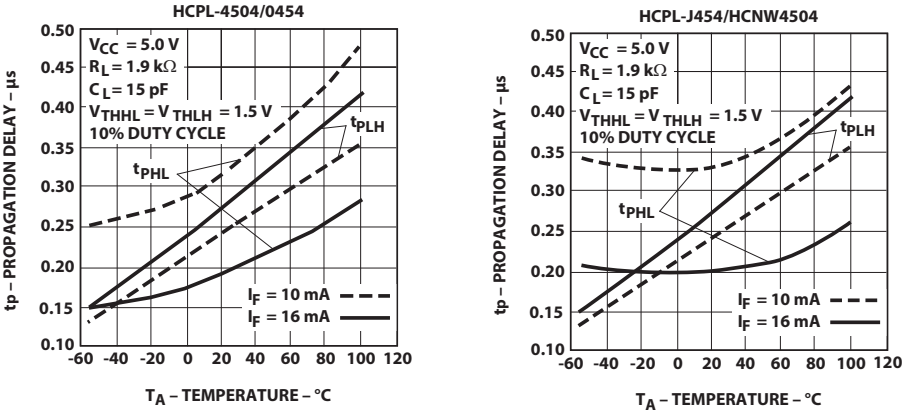


Figure 9: Propagation Delay Time vs. Load Resistance

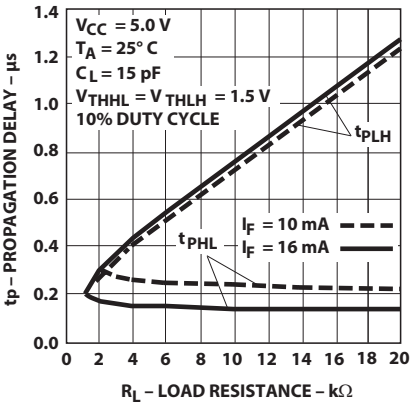


Figure 10: Propagation Delay Time vs. Load Resistance

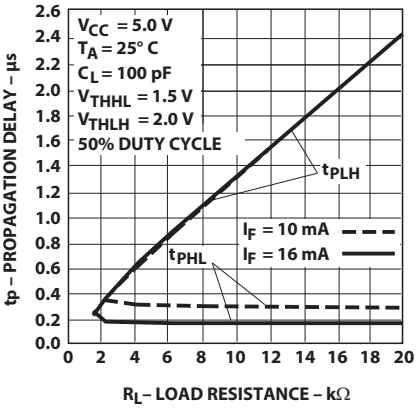


Figure 11: Propagation Delay Time vs. Temperature

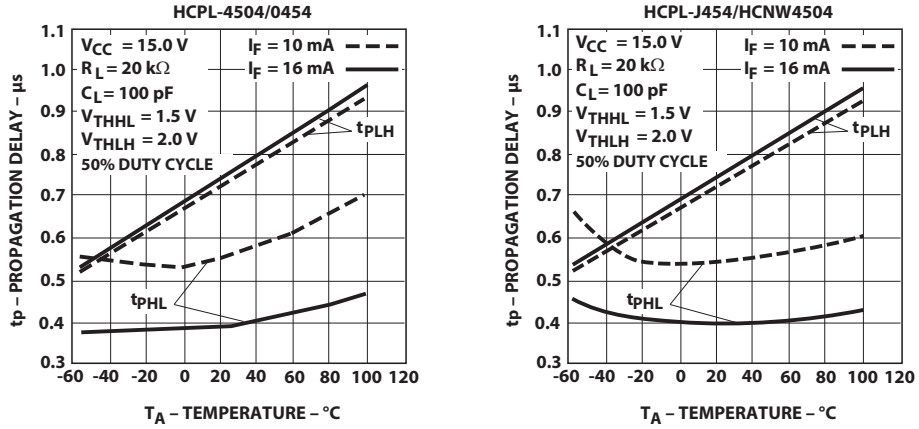


Figure 12: Propagation Delay Time vs. Load Resistance

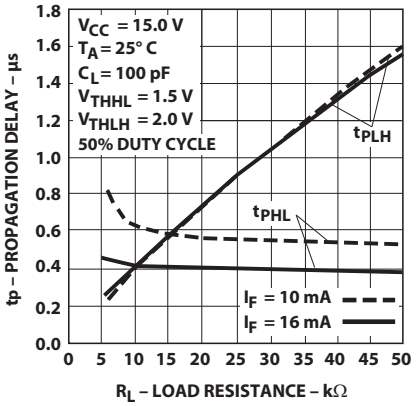


Figure 13: Propagation Delay Time vs. Load Capacitance

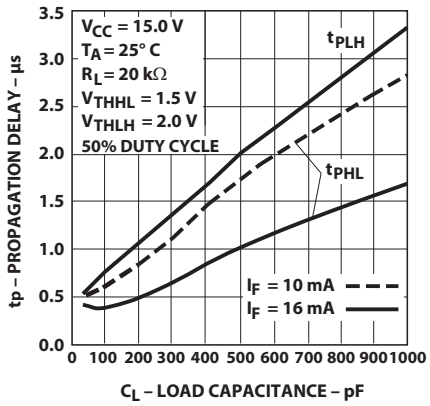


Figure 14: Propagation Delay Time vs. Supply Voltage

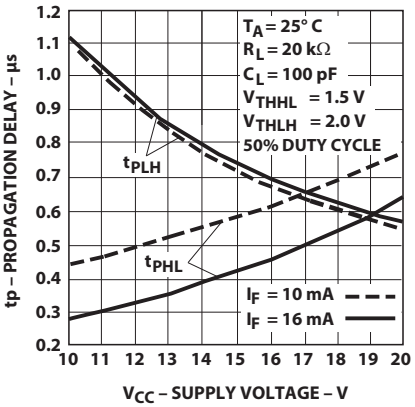


Figure 15: Thermal Derating Curve, Dependence of Safety Limiting Valve with Case Temperature per IEC/EN/DIN EN 60747-5-2

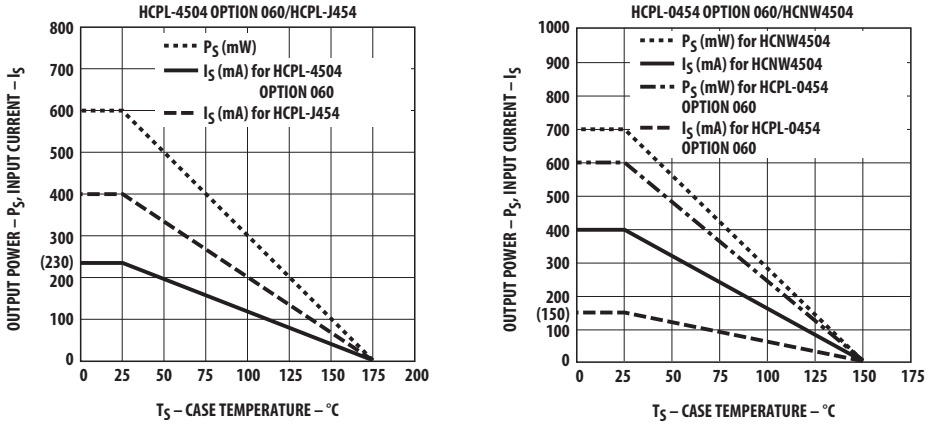


Figure 16: Typical Power Inverter

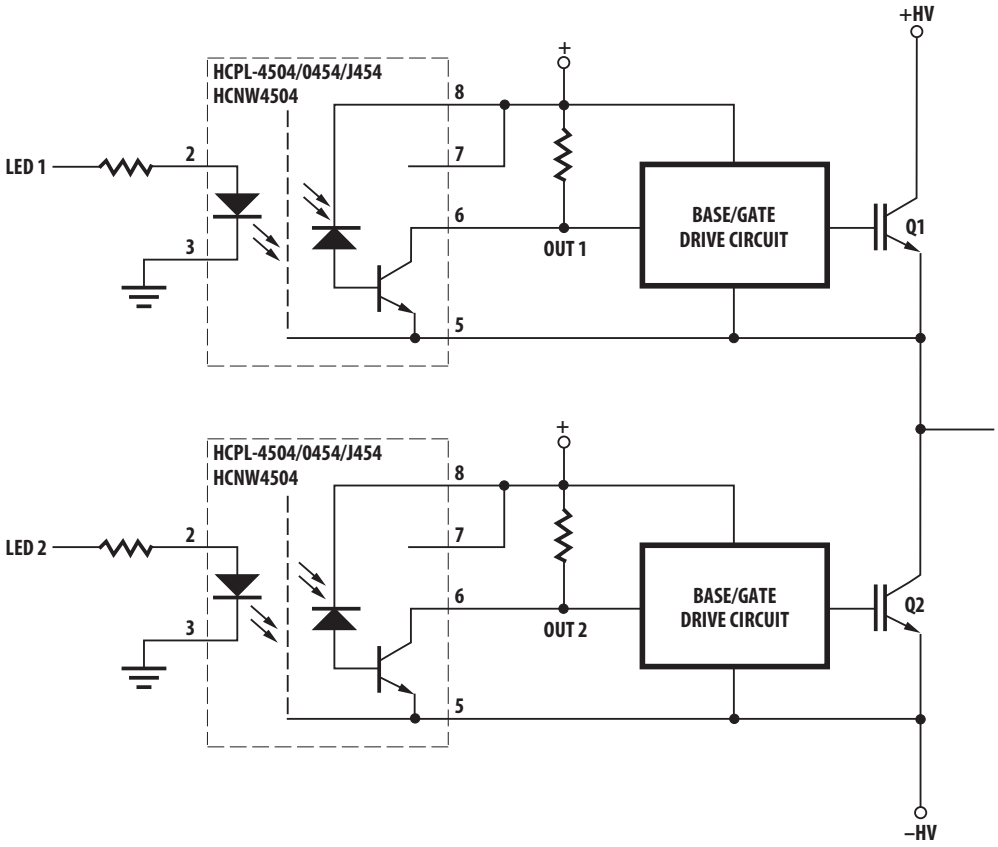
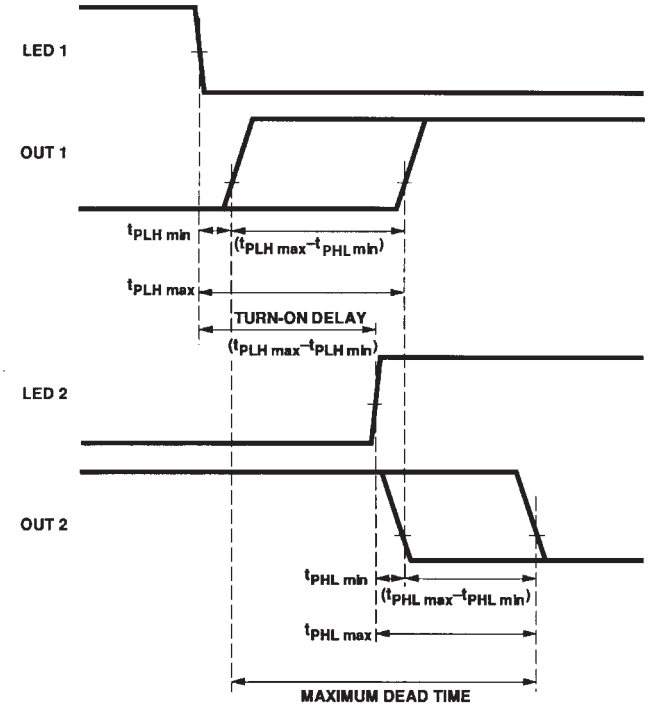


Figure 17: LED Delay and Dead Time Diagram



Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-4504/0454/J454 and HCNW4504 include a specification intended to help designers minimize “dead time” in their power inverter designs. The new “propagation delay difference” specification ($t_{PLH} – t_{PHL}$) is useful for determining not only how much optocoupler switching delay is needed to prevent “shoot-through” current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 17), it is essential that they never conduct at the same time. Extremely large currents flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This “shoot-through” current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of “dead time” at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turnoff (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled “LED1”, “LED2”, “OUT1”, and “OUT2” are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an overcurrent condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay (t_{PHLmin}) never turns on before an optocoupler with the very slowest turn-off propagation delay (t_{PLHmax}) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than ($t_{PLHmax} – t_{PHLmin}$), which also happens to be the maximum data sheet value for the propagation delay difference specification, ($t_{PLH} – t_{PHL}$). The HCPL-4504/0454/J454 and HCNW4504 specify a maximum ($t_{PLH} – t_{PHL}$) of 1.3 µs over an operating temperature range of 0°C to 70°C.

Although $(t_{PLH} – t_{PHL})_{max}$ tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to $(t_{PLH} – t_{PHL})_{max}$, the minimum dead time is zero (that is, there is zero time between the turn-off of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to $(t_{PLH} – t_{PHL})_{max}$, it can be seen in Figure 17 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turnoff delay,

$[(t_{PLHmax} – t_{PLHmin}) + (t_{PHLmax} – t_{PHLmin})]$.

This expression can be rearranged to obtain

$[(t_{PLHmax} – t_{PHLmin}) – (t_{PHLmin} – t_{PHLmax})]$,

and further rearranged to obtain

$[(t_{PLH} – t_{PHL})_{max} – (t_{PLH} – t_{PHL})_{min}]$,

which is the maximum minus the minimum data sheet values of ($t_{PLH} – t_{PHL}$). The difference between the maximum and minimum values depends directly on the total spread in propagation delays and sets the limit on how good the worst-case dead time can be for a given design. Therefore, optocouplers with tight propagation delay specifications (and not just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The HCPL-4504/0454/J454 and HCNW4504 specify a minimum ($t_{PLH} – t_{PHL}$) of –0.7 µs over an operating temperature range of 0°C to 70°C, resulting in a maximum dead time of 2.0 µs when the LED turn-on delay is equal to $(t_{PLH} – t_{PHL})_{max}$, or 1.3 µs.

It is important to maintain accurate LED turn-on delays because delays shorter than $(t_{PLH} – t_{PHL})_{max}$ may allow shoot-through currents, while longer delays will increase the worst-case dead time.

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