

STD2N62K3-VB Datasheet

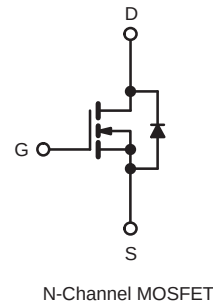
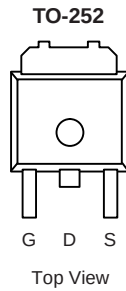
Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	2.1
Q_g (Max.) (nC)	48	
Q_{gs} (nC)	12	
Q_{gd} (nC)	19	
Configuration	Single	

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC


RoHS*
 COMPLIANT


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ^e	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
Continuous Drain Current		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	18	
Linear Derating Factor		0.48	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	325	mJ
Repetitive Avalanche Current ^a	I_{AR}	4	A
Repetitive Avalanche Energy ^a	E_{AR}	6	mJ
Maximum Power Dissipation	P_D	60	W
Peak Diode Recovery dV/dt ^c	dV/dt	2.8	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^d		300	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 24\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 3.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 3.2\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.1	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	670	-	mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.1 A ^b	-	2.1	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3.1 A		3.9	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1417	-	pF
Output Capacitance	C _{oss}			-	177	-	
Reverse Transfer Capacitance	C _{rss}			-	7.0	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	1912	-	
Effective Output Capacitance	C _{oss eff.}		V _{DS} = 520 V, f = 1.0 MHz	-	48	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 3.2 A, V _{DS} = 400 V see fig. 6 and 13 ^b	-	-	48	nC
Gate-Source Charge	Q _{gs}			-	-	12	
Gate-Drain Charge	Q _{gd}			-	-	19	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 325 V, I _D = 3.2 A R _G = 9.1 Ω, R _D = 62 Ω, see fig. 10 ^b		-	14	-	ns
Rise Time	t _r			-	20	-	
Turn-Off Delay Time	t _{d(off)}			-	34	-	
Fall Time	t _f			-	18	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	21	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 3.2 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 3.2 A, dI/dt = 100 A/μs ^b		-	493	739	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	2.1	3.2	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
 c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 d. $t = 60\text{ s}$, $f = 60\text{ Hz}$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

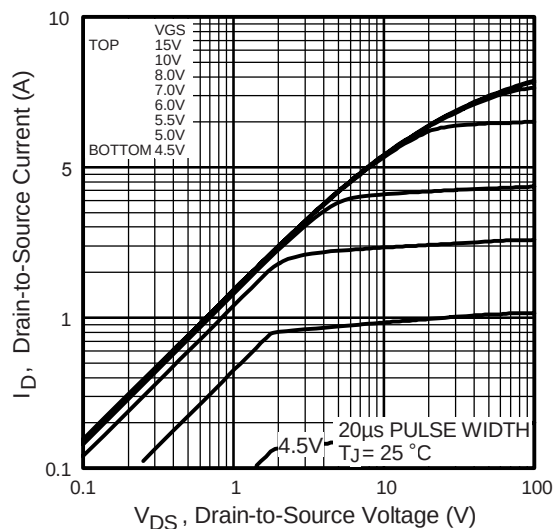


Fig. 1 - Typical Output Characteristics

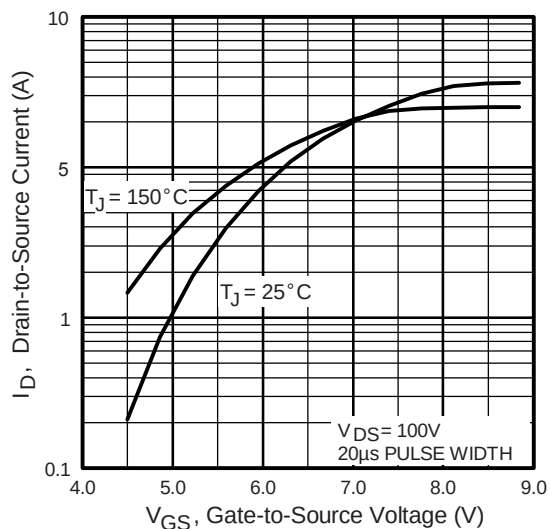


Fig. 3 - Typical Transfer Characteristics

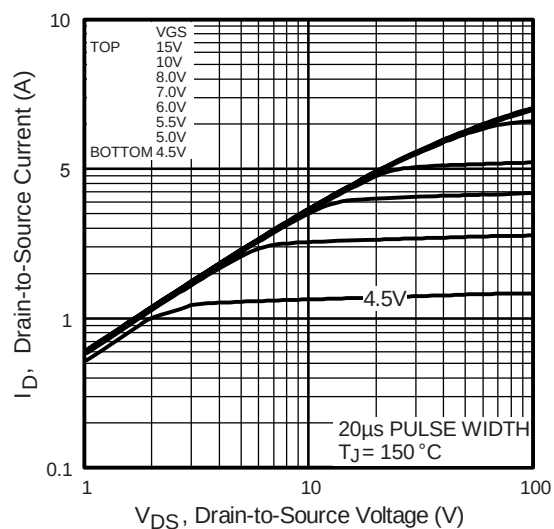


Fig. 2 - Typical Output Characteristics

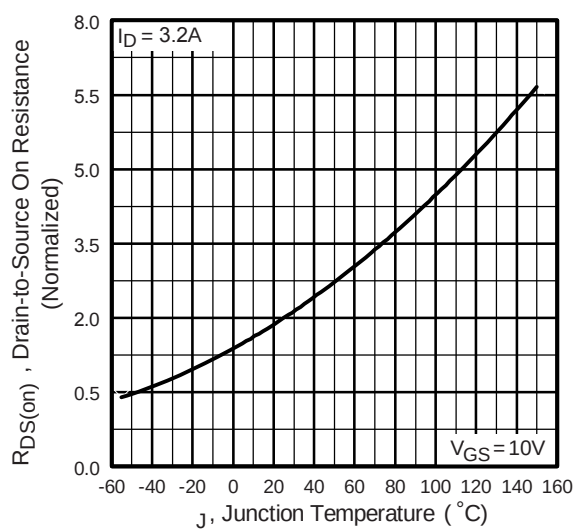


Fig. 4 - Normalized On-Resistance vs. Temperature

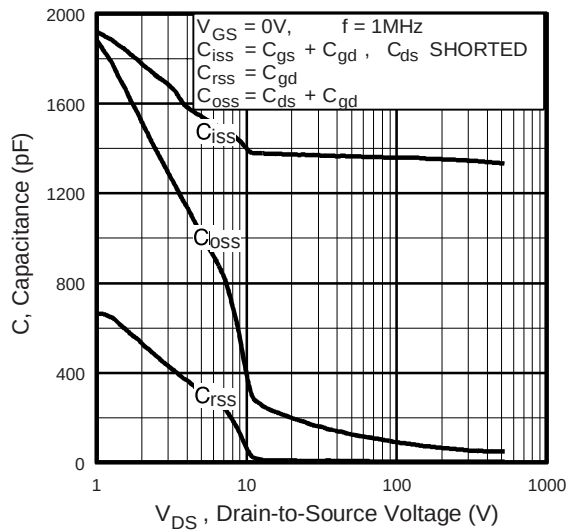


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

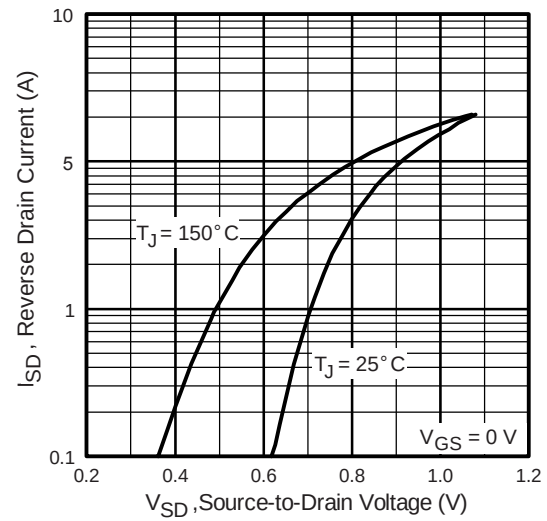


Fig. 7 - Typical Source-Drain Diode Forward Voltage

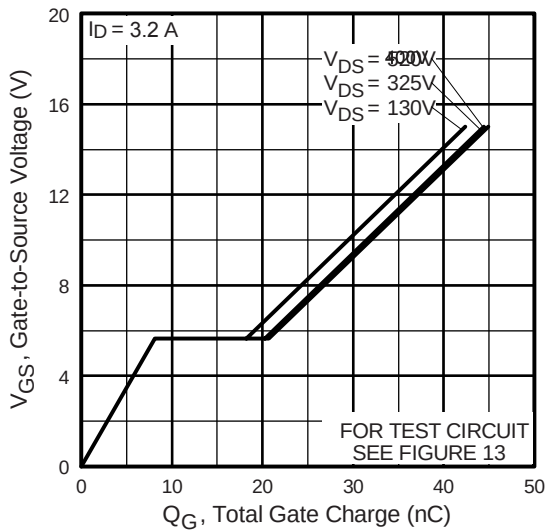


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

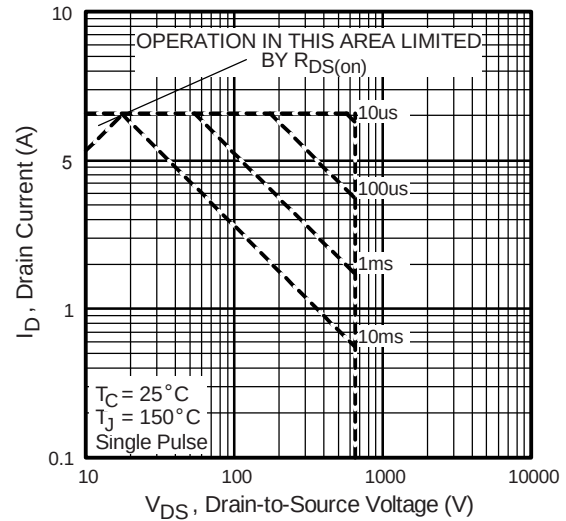


Fig. 8 - Maximum Safe Operating Area

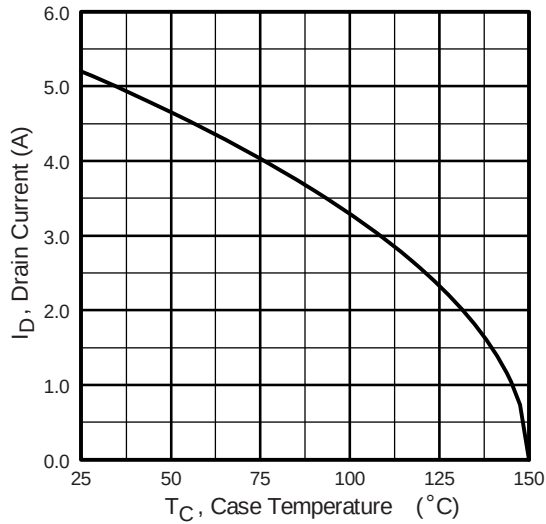


Fig. 9 - Maximum Drain Current vs. Case Temperature

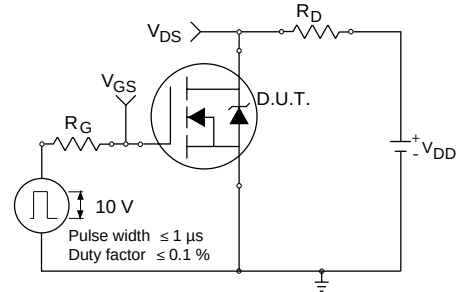


Fig. 10a - Switching Time Test Circuit

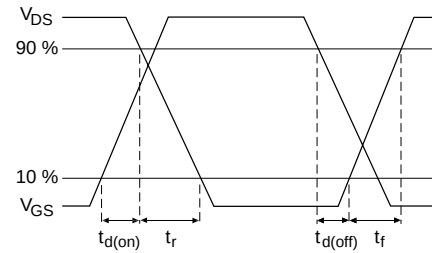


Fig. 10b - Switching Time Waveforms

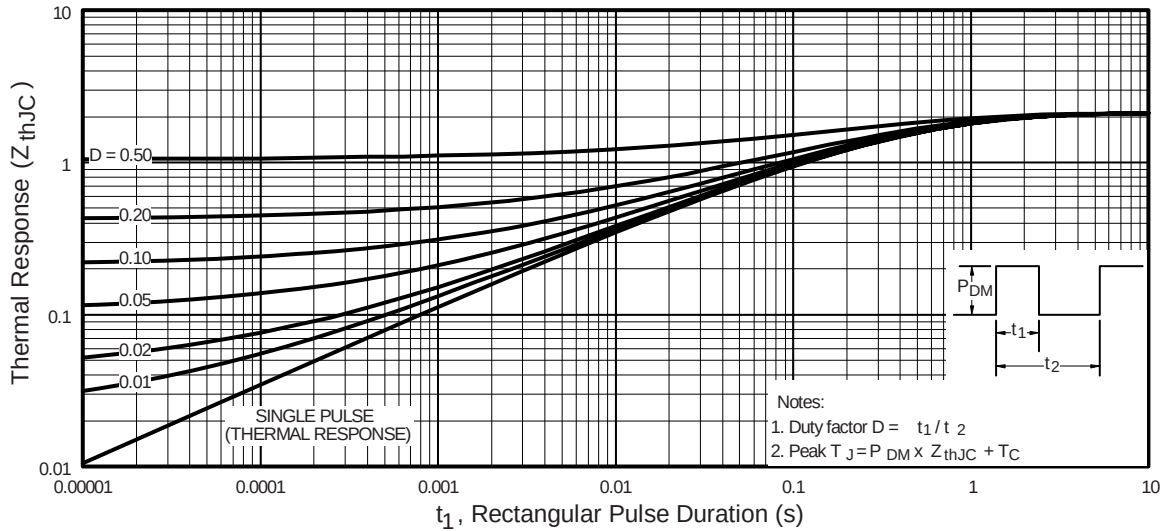


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

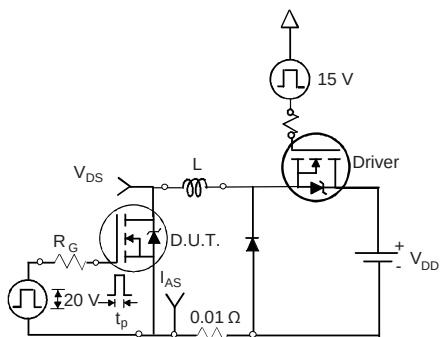


Fig. 12a - Unclamped Inductive Test Circuit

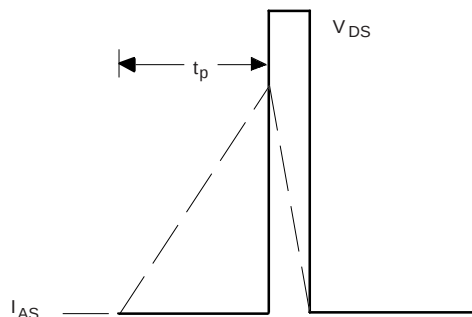


Fig. 12b - Unclamped Inductive Waveforms

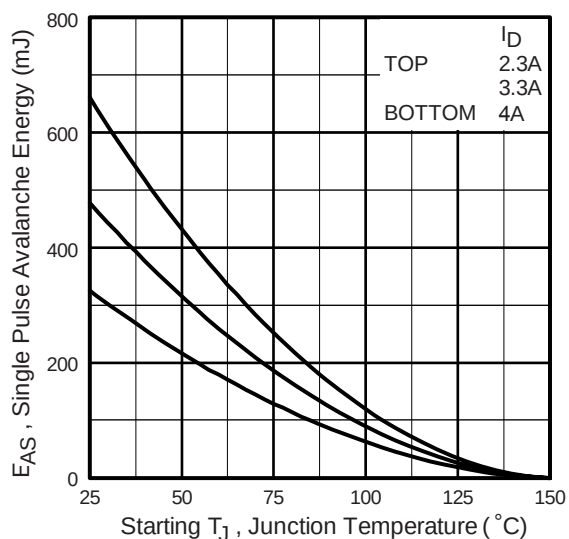


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

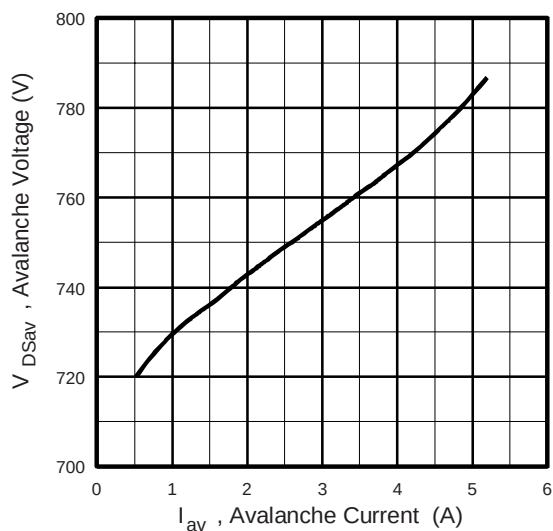


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

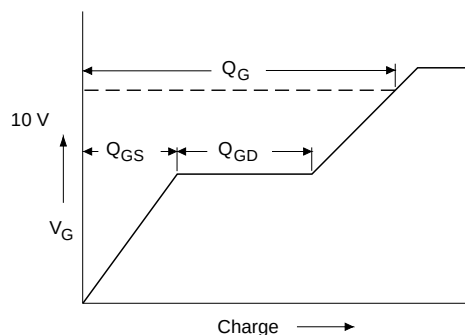


Fig. 13a - Basic Gate Charge Waveform

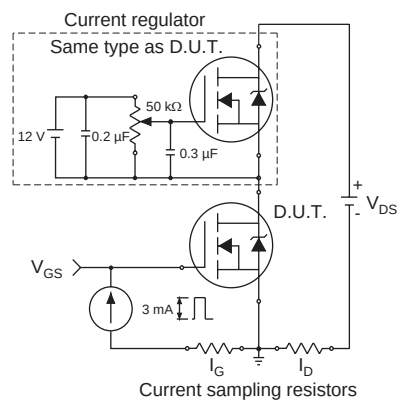
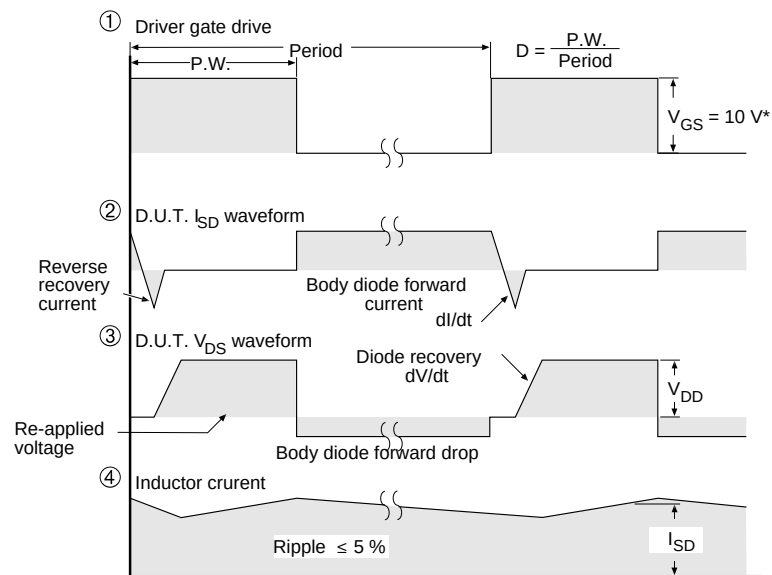
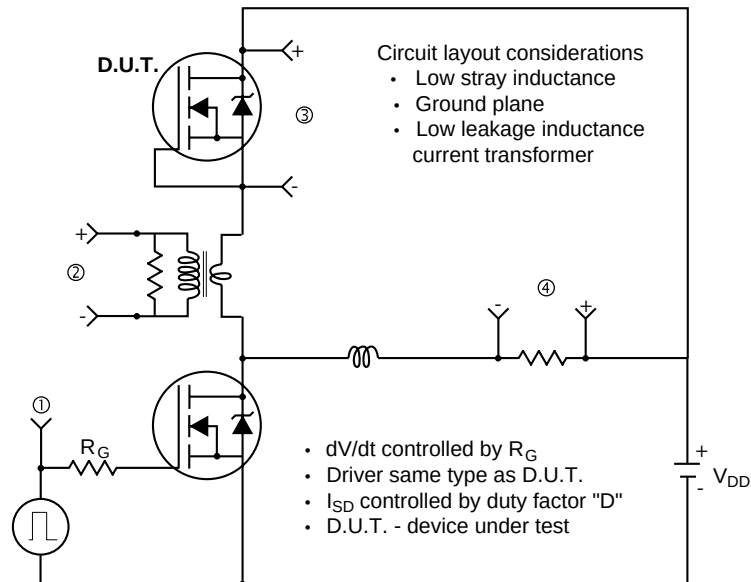


Fig. 13b - Gate Charge Test Circuit

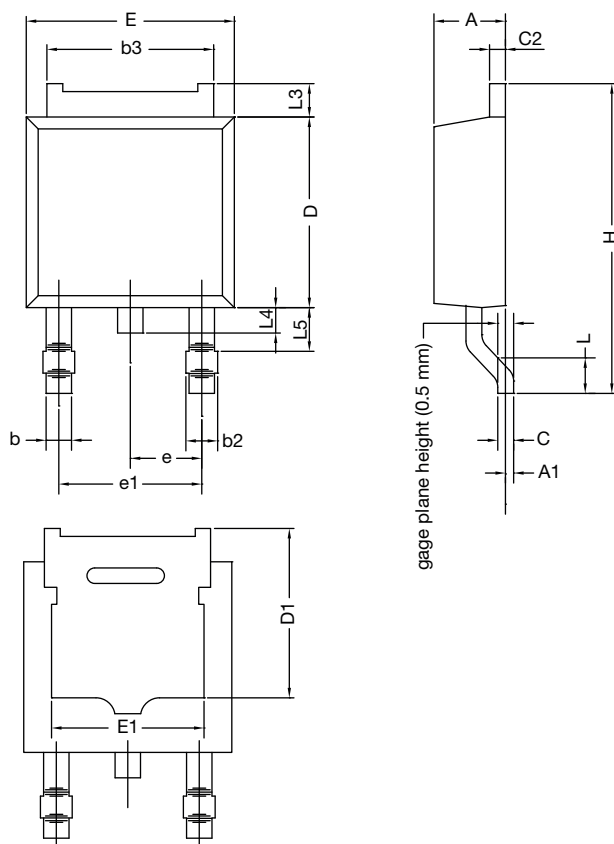
Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 14 - For N-Channel

TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

Note

- Dimension L3 is for reference only.

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