

SI7960DP-VB Datasheet

Dual N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.032
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.038
Q_g typ. (nC)	7.1
I_D (A)	17
Configuration	Dual

FEATURES

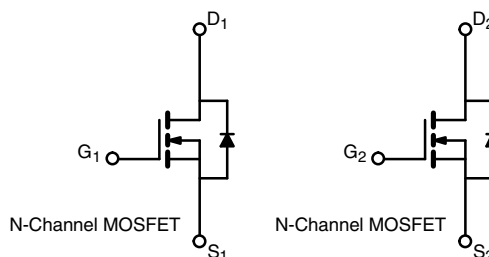
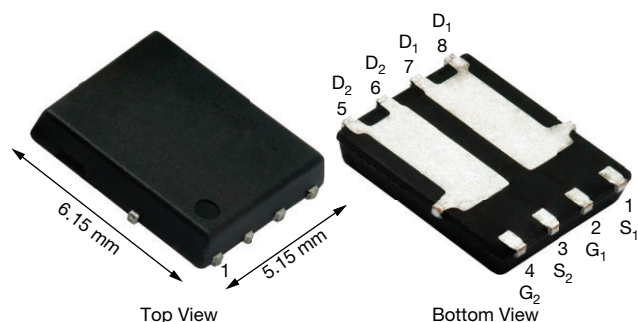
- Trench power MOSFET
- PWM optimized
- 100 % R_g and UIS tested

APPLICATIONS

- System power DC/DC



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed drain current	I_{DM}	40	A
Source-drain current diode current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	
Maximum power dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient ^{b, f}	R_{thJA}	26	35	°C/W
Maximum junction-to-case (drain)	R_{thJC}	4	5.5	

Notes

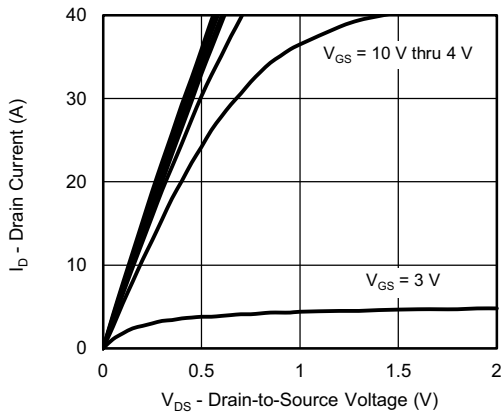
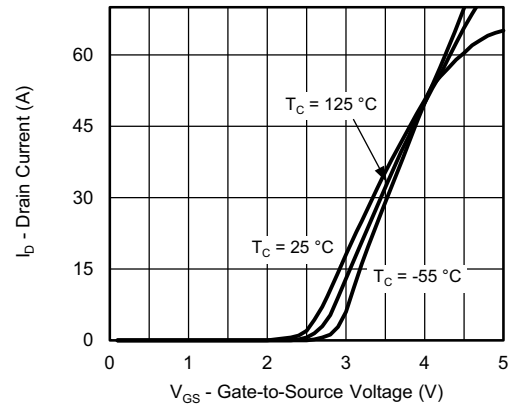
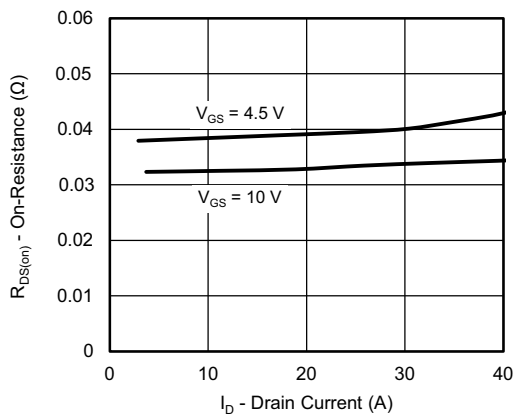
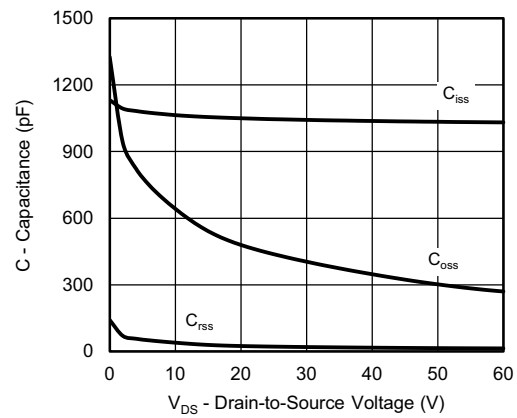
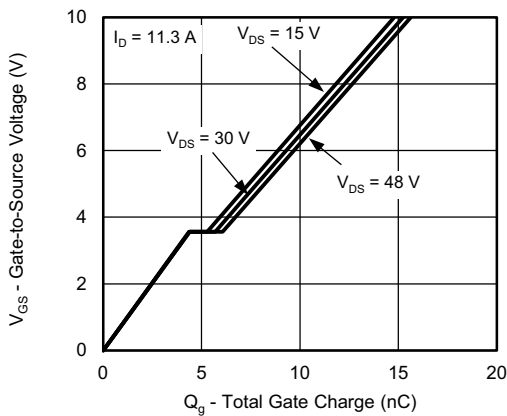
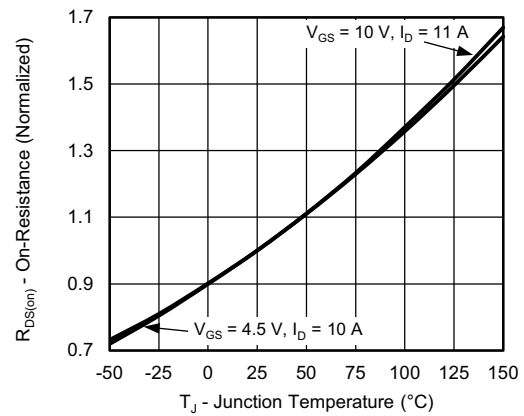
- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- The DFN 5x6 package is a leadless package. The end of the lead terminal is exposed copper(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 80 °C/W

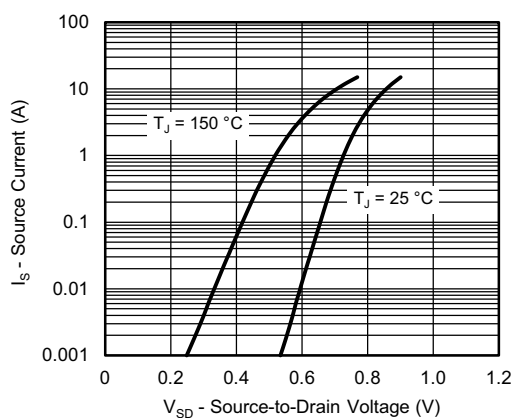
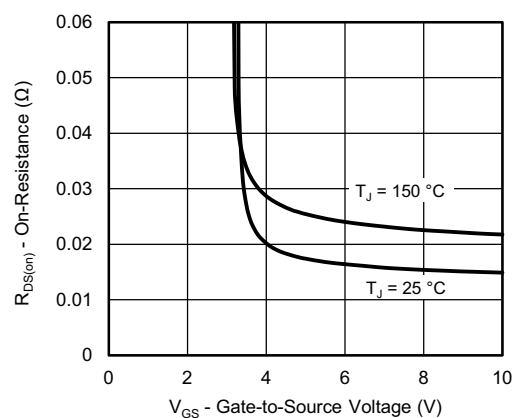
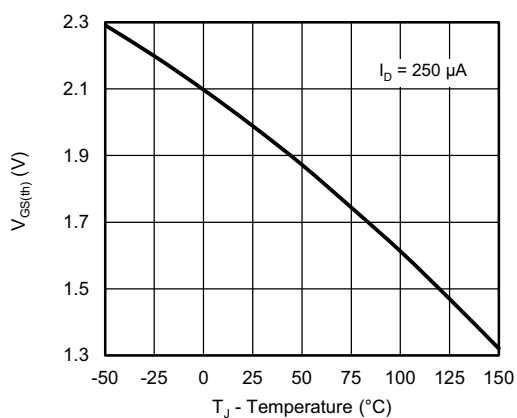
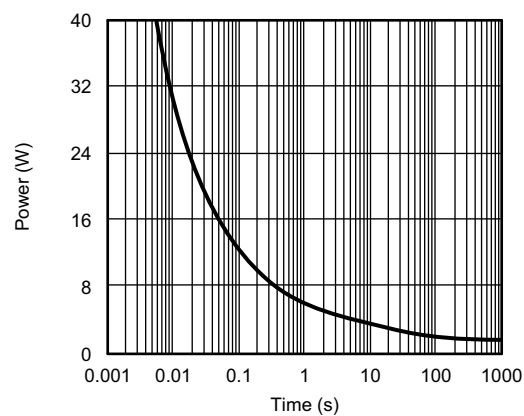
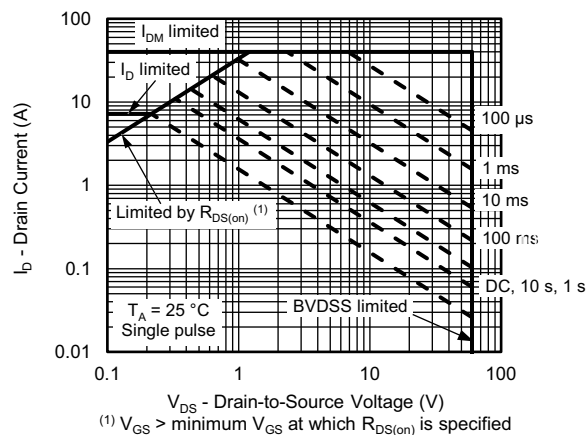
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	38	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-4.9	-	
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2	-	2.7	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 85 °C	-	-	10	
On-state drain current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	60	-	-	A
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 11 A	-	0.032	-	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.038	-	
Forward transconductance ^b	g _{fs}	V _{DS} = 30 V, I _D = 11 A	-	38	-	S
Dynamic ^a						
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	-	1050	-	pF
Output capacitance	C _{oss}		-	435	-	
Reverse transfer capacitance	C _{rss}		-	20	-	
Total gate charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 11 A	-	15.2	23	nC
Gate-source charge	Q _{gs}	V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 11 A	-	7.1	11	
Gate-drain charge	Q _{gd}		-	4.4	-	
			-	1.3	-	
Gate resistance	R _g	f = 1 MHz	0.12	0.6	1.2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, R _L = 3.45 Ω I _D ≅ 8.7 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	15	120	ns
Rise time	t _r		-	80	30	
Turn-off delay time	t _{d(off)}		-	15	30	
Fall time	t _f		-	15	30	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, R _L = 3.45 Ω I _D ≅ 8.7 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	15	
Rise time	t _r		-	25	40	
Turn-off delay time	t _{d(off)}		-	20	30	
Fall time	t _f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode Current	I _S	T _C = 25 °C	-	-	8	A
Pulse diode forward current ^a	I _{SM}		-	-	40	
Body diode voltage	V _{SD}	I _S = 8.7 A	-	0.8	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 8.7 A, di/dt = 100 A/μs, T _J = 25 °C	-	34	51	ns
Body diode reverse recovery charge	Q _{rr}		-	30	45	nC
Reverse recovery fall time	t _a		-	16	-	ns
Reverse recovery rise time	t _b		-	18	-	

Notes

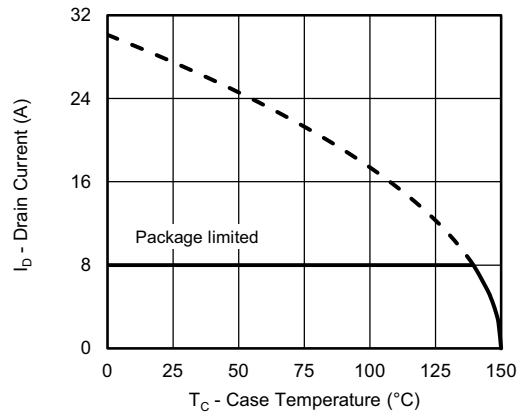
- a. Guaranteed by design, not subject to production testing
 b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

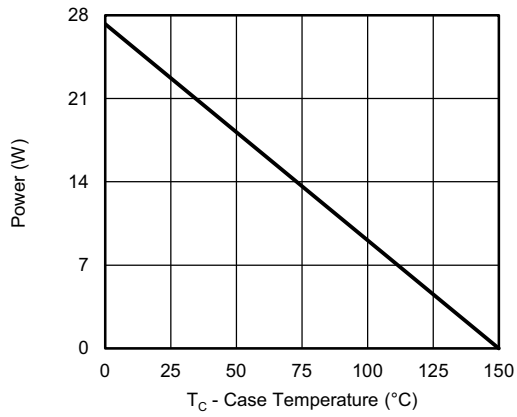
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

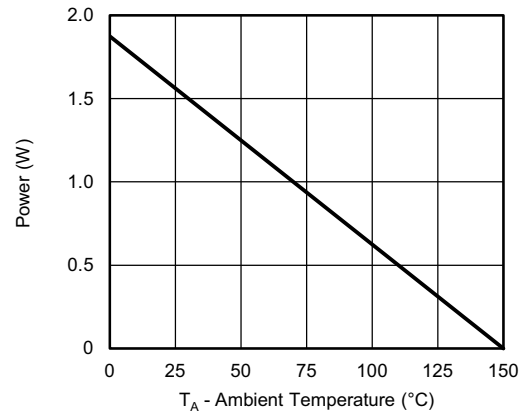
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



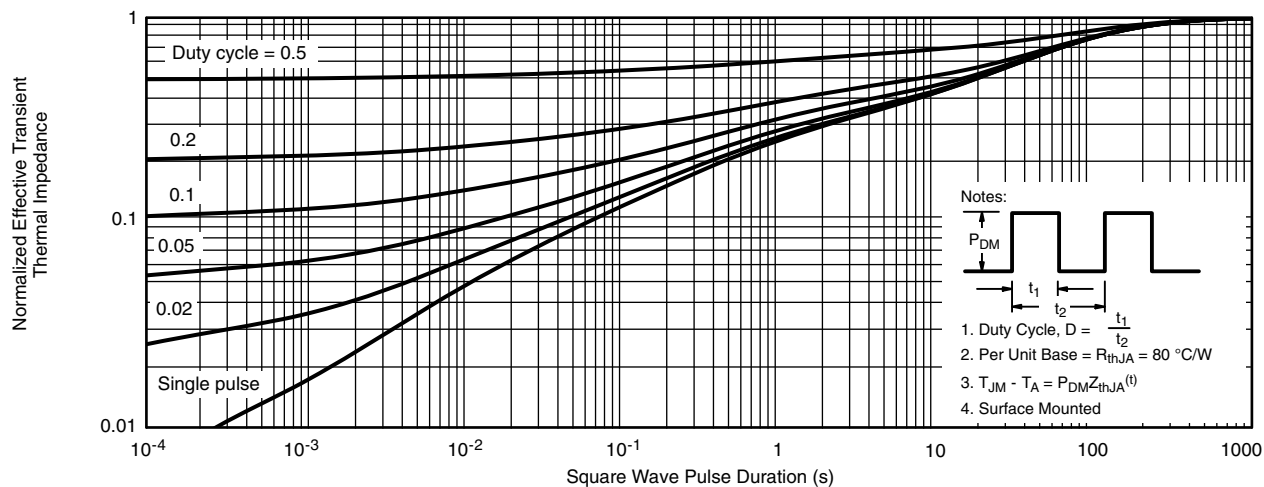
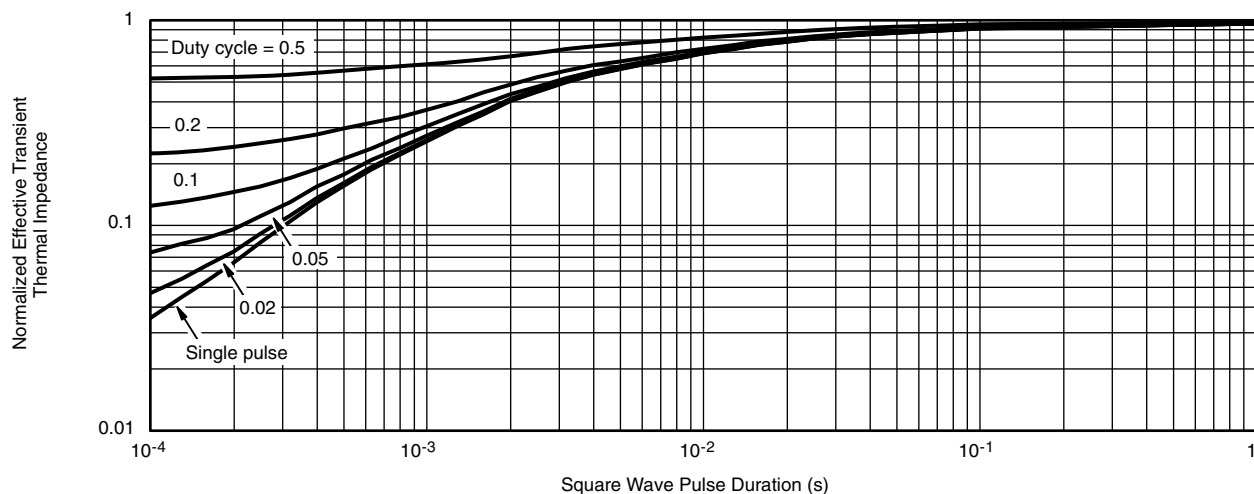
Power, Junction-to-Case



Power, Junction-to-Ambient

Note

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

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