

## P-Channel 100 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	- 100
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.033
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.037
$I_D$ (A)	- 40
Configuration	Single

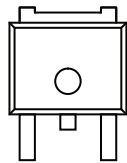
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

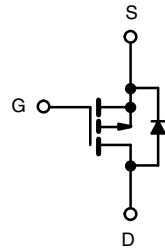
TO-252



G D S

Top View

Drain Connected to Tab



P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	- 100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25^\circ\text{C}$	$I_D$	- 40	A
	$T_C = 125^\circ\text{C}$		- 22	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	- 50	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	- 150	
Single Pulse Avalanche Current	L = 0.1 mH	$I_{AS}$	- 44	
Single Pulse Avalanche Energy		$E_{AS}$	96	mJ
Maximum Power Dissipation <sup>b</sup>	$T_C = 25^\circ\text{C}$	$P_D$	136	W
	$T_C = 125^\circ\text{C}$		45	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	50	$^\circ\text{C/W}$
Junction-to-Case (Drain)		$R_{thJC}$	1.1	

#### Notes

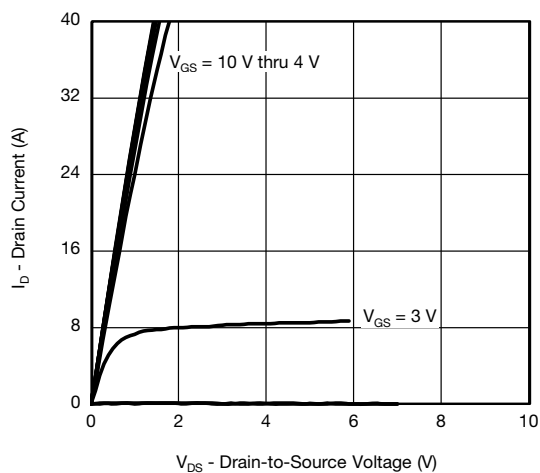
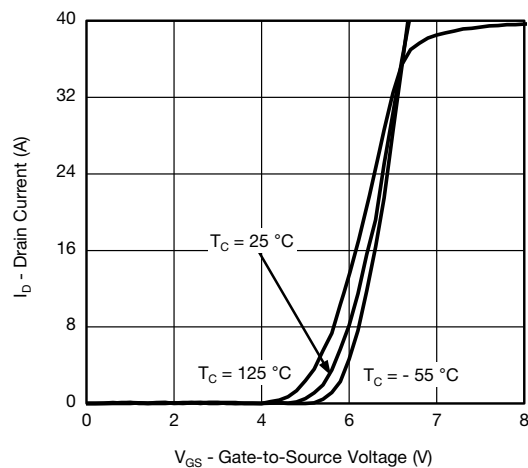
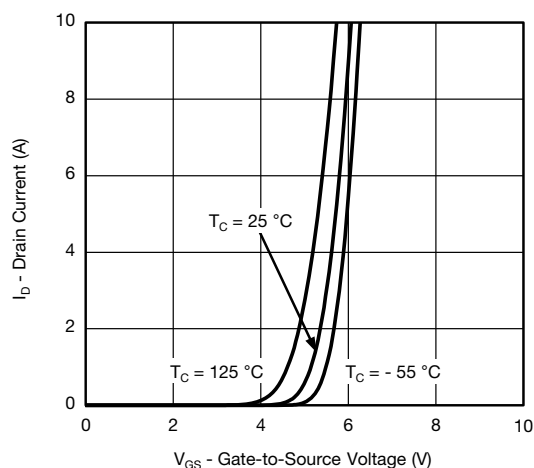
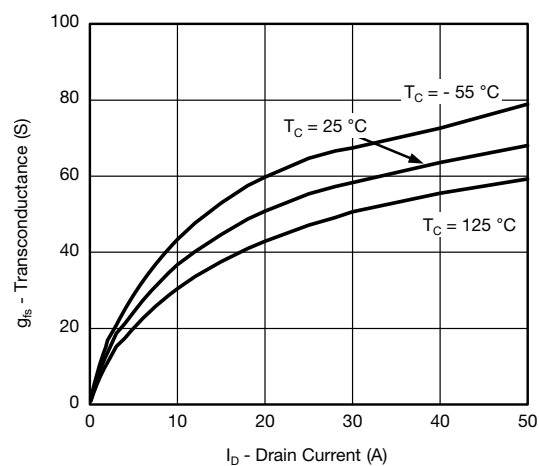
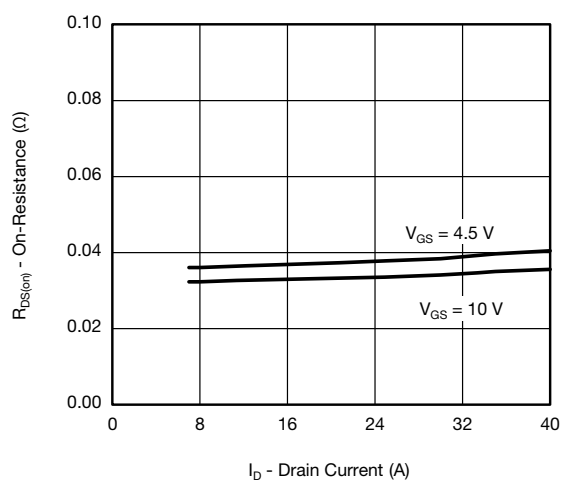
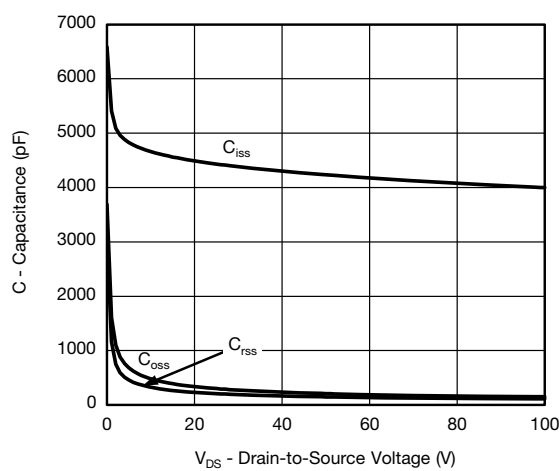
- Package limited.
- Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

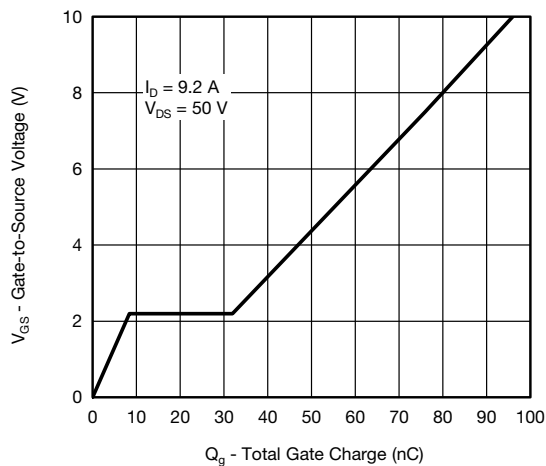
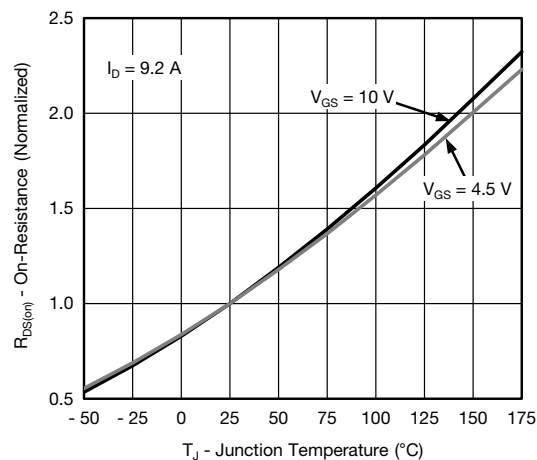
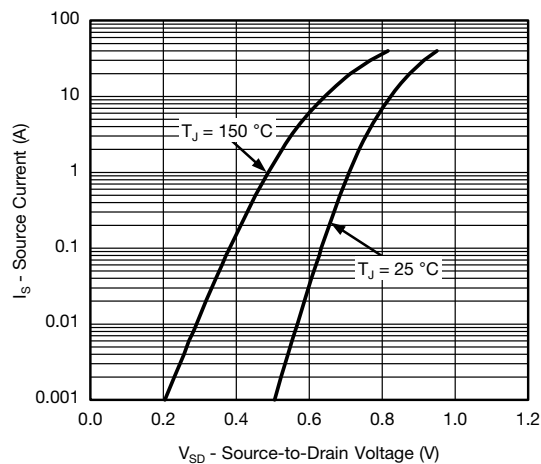
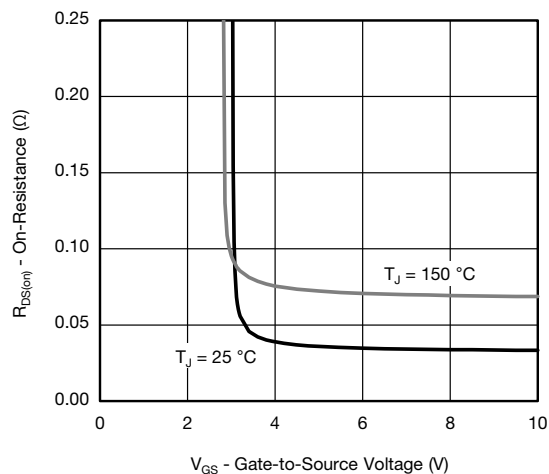
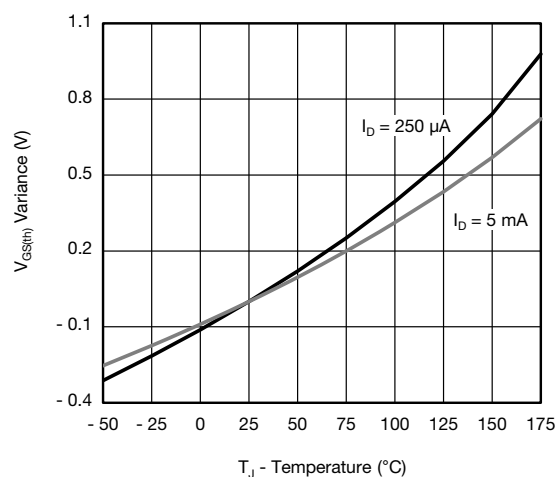
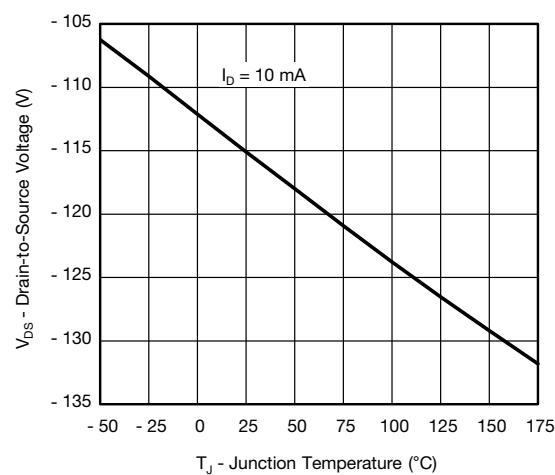
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA		- 100	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA		- 1.0	-	-2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 100 V	-	-	- 1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 100 V, T <sub>J</sub> = 125 °C	-	-	- 50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 100 V, T <sub>J</sub> = 175 °C	-	-	- 250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> ≤ - 5 V	- 30	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 9.2 A	-	0.033	-	Ω
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 9.2 A, T <sub>J</sub> = 125 °C	-	0.065	-	
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 9.2 A, T <sub>J</sub> = 175 °C	-	0.081	-	
		V <sub>GS</sub> = - 4.5 V	I <sub>D</sub> = - 7.7 A	-	0.037	-	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 9.2 A		-	35	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 25 V, f = 1 MHz	-	4433	-	pF
Output Capacitance	C <sub>oss</sub>			-	301	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	208	-	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> = - 50V, I <sub>D</sub> = - 9.2 A	-	96	144	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	8.4	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	23.5	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.5	3.13	4.7	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = - 50 V, R <sub>L</sub> = 6.49 Ω I <sub>D</sub> ≅ - 7.7 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1.0 Ω		-	11	17	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	11	17	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	78	117	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	15	23	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	- 150	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = - 7.7 A, V <sub>GS</sub> = 0 V		-	- 0.8	- 1.5	V

**Notes**

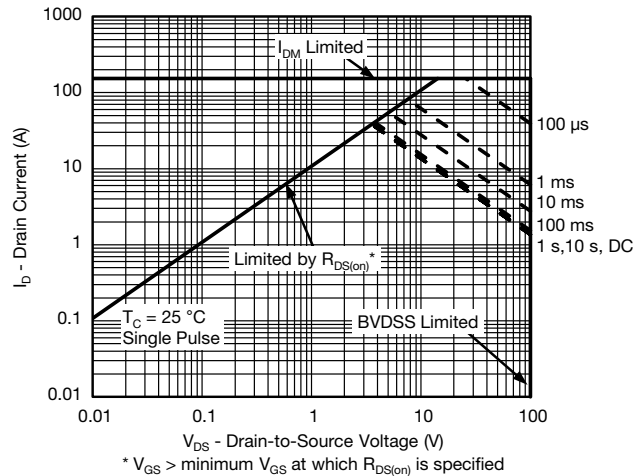
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.  
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

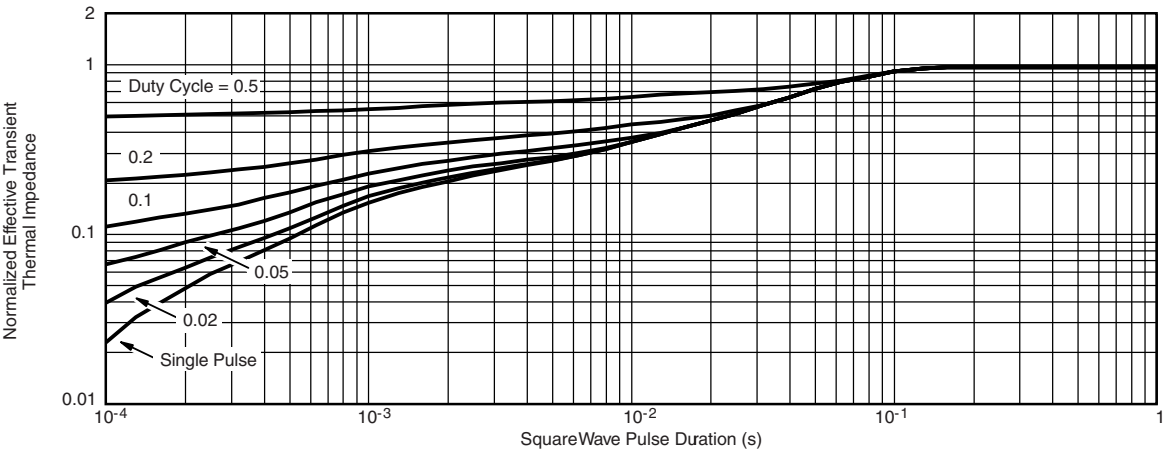
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Drain Source Breakdown vs. Junction Temperature**

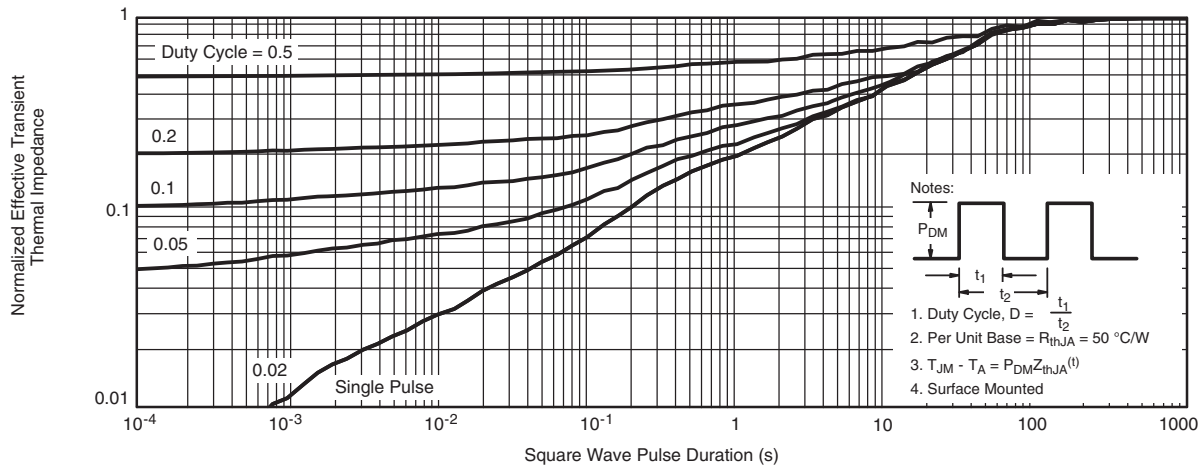
**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



**Safe Operating Area**

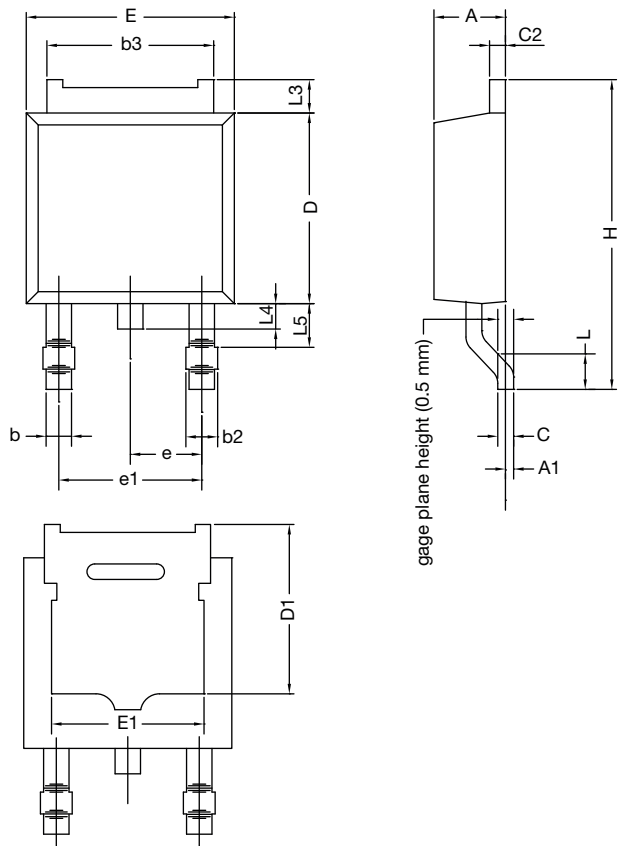


**Normalized Thermal Transient Impedance, Junction-to-Case**

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction to Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction to Case ( $25\text{ }^{\circ}\text{C}$ )
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

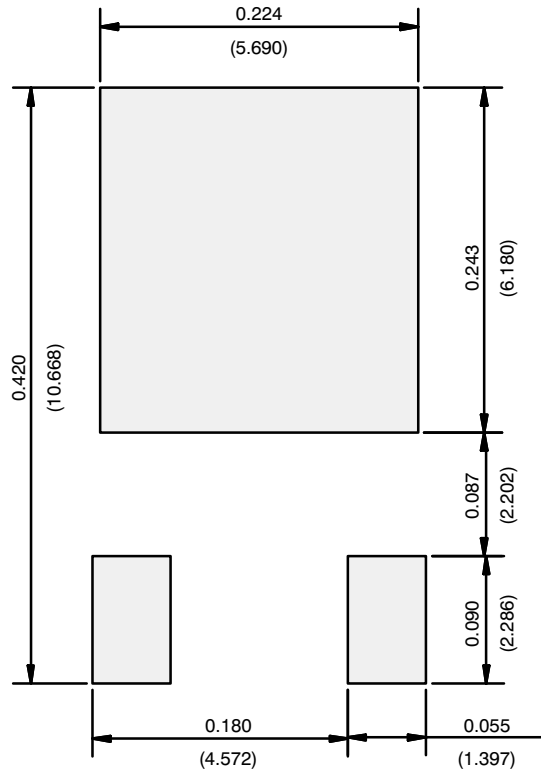
TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13				
DWG: 6019				

- Note**
- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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