Integrated Driver and MOSFET & Linear Regulator

General Description

The DS9613 are high frequency integrated power stage optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance with very low shutdown current. Packaged in QFN3x3-21L & QFN4x4-23L package, DS9613 enable voltage regulator designs to deliver up to 8 A continuous current per phase.

The DS9613 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap switch.

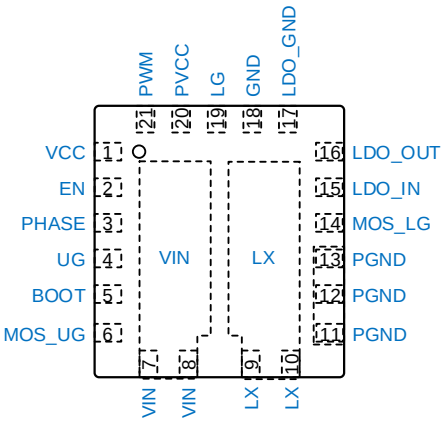
The DS9613 offer operating temperature monitoring, protection features, and warning flags that improve system monitoring and reliability.

Features

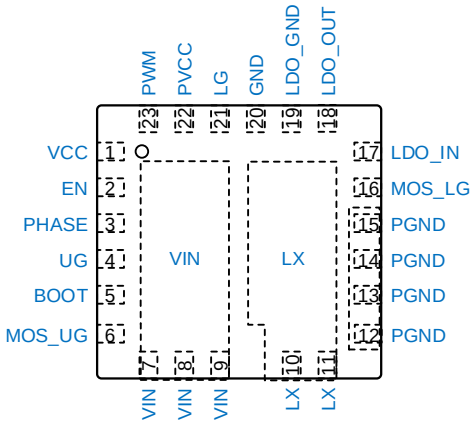
- Capable of Average Currents up to 8A
- Capable of Switching at Frequencies up to 1 MHz
- Integrated High Voltage Linear Regulator
- Compatible with 2V ~ 5V PWM Input
- Support VCC to 2.5V ~ 5.5V Power
- Internal Bootstrap Diode
- Undervoltage Lockout
- The QFN3x3-21L & QFN4x4-23L Package Available

Pin Configurations

QFN3x3-21L



QFN4x4-23L



Applications

- True Wireless Stereo

Ordering Information

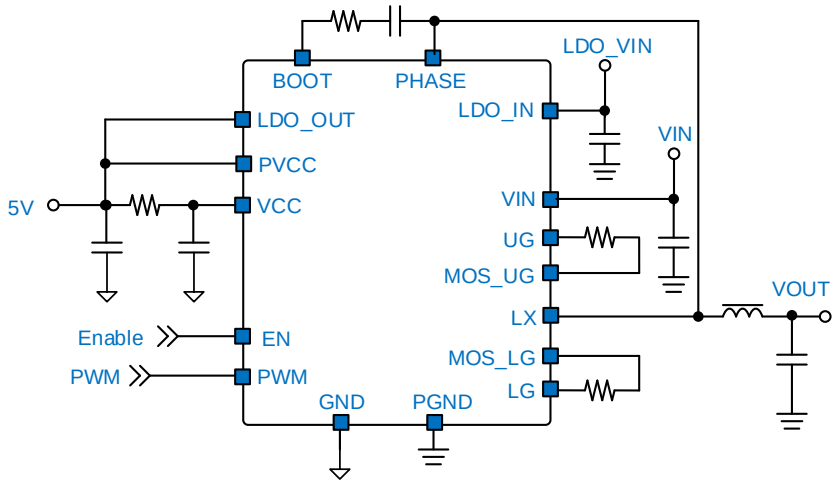
DS9613XX

Designator	Description	Symbol	Description
XX	Package Type	Q33	QFN3x3-21L
		Q44	QFN4x4-23L

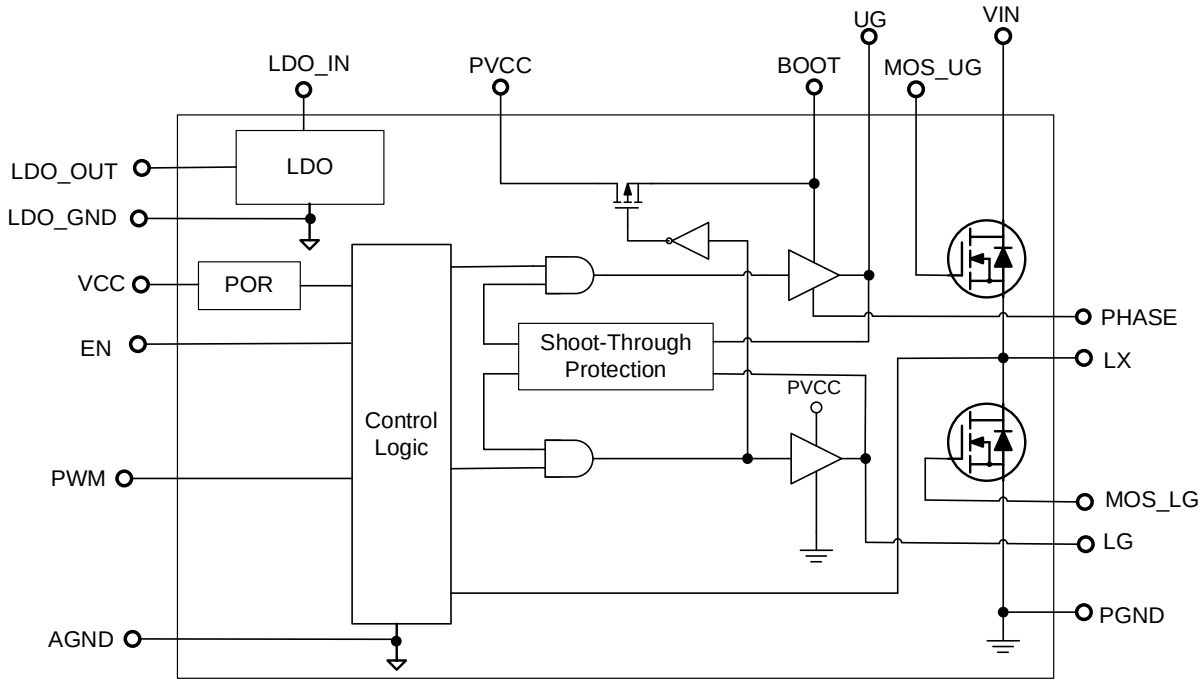
Description of Functional Pins

Pin No		Pin Name	Pin Function
QFN3x3-21L	QFN4x4-23L		
1	1	VCC	Power supply of internal control logic. The required bias voltage for VCC is 2.5V ~ 5.5V. For avoiding noise disturbance, the supplied bias voltage must be stable.
2	2	EN	Enable Pin. When low, both UGATE and LGATE are driven low and the normal operation is disabled.
3	3	PHASE	Bootstrap Capacitor Return , Must be connected to LX .
4	4	UG	Driver for High Side MOSFET Gate Access .
5	5	BOOT	Bootstrap Supply for High Side Gate Drive.
6	6	MOS_UG	High Side MOSFET Gate Input .
7 , 8	7 , 8 , 9	VIN	Conversion Supply Power Input .
9 , 10	10 , 11	LX	Switch Node Output .
11 , 12 , 13	12 , 13 , 14 , 15	PGND	Power Ground .
14	16	MOS_LG	Low Side MOSFET Gate Input .
15	17	LDO_OUT	Linear Regulator Output Pin.
16	18	LDO_IN	Linear Regulator Input Pin.
17	19	GND	Linear Regulator (LDO) ground.
18	20	GND	Analog ground.
19	21	LG	Driver for Low Side MOSFET Gate Access .
20	22	PVCC	Power supply of gate driver. The required bias voltage for PVCC is 2.5V ~ 5.5V. Connect a 1uF/X7R between PVCC and PGND.
21	23	PWM	PWM Signal Input. Connect this pin to the PWM output of the controller .

Typical Application Circuits



Function Block Diagram



Absolute Maximum Ratings (Note 1)

VIN to GND ---------- 30V

VCC & PVCC to GND ---------- 6.5V

BOOT to PHASE, $V_{BOOT-PHASE}$

DC ---------- −0.3V to 6.5V

< 20ns ---------- −5V to 7.5V

PHASE & LX to GND

DC ---------- −0.3V to 30V

< 20ns ---------- −10V to 35V

GL to GND

DC ---------- −0.3V to 6.5V

< 20ns ---------- −2.5V to 7.5V

LDO_IN to GND ---------- 28V

Other Pins ---------- (GND − 0.3V) to 6.5V

Power Dissipation, PD @ T_A = 25°C

QFN3x3-21L ---------- 3.3W

QFN4x4-23L ---------- 5.8W

Package Thermal Resistance (Note 2)

QFN3x3-21L , θ_{JA} ---------- 35°C/W

QFN4x4-23L , θ_{JA} ---------- 19°C/W

Lead Temperature (Soldering, 10 sec.) ---------- 260°C

Junction Temperature ---------- 150°C

Storage Temperature Range ---------- −65°C to 150°C

ESD Susceptibility (Note 3)

HBM (Human Body Model) ---------- 2KV

Recommended Operating Conditions

Supply Input Voltage, VIN ---------- 2.5V to 24V

Supply LDO Input Voltage, LDO_IN ---------- 5.5V to 23V

Control Input Voltage, VCC & PVCC ---------- 2.5V to 5.5V

Junction Temperature Range ---------- −10°C to 125°C

Ambient Temperature Range ---------- −10°C to 85°C

Electrical Characteristics

(V_{IN} =12V, V_{CC} =5V, T_A=25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range		VCC , PVCC		2.5	5.0	5.5	V
Quiescent Current		I_{Q_VCC}	PWM Input Floating		50		μA
Power On Reset		V_{POR_R}	VCC & PVCC Rising	--	2.5	2.8	V
		V_{POR_F}	VCC & PVCC Falling	2.1	2.3	--	V
Conversion Voltage		VIN		2.5	12	24	V
Continuous Output Current			F_{SW} = 1 MHz, VIN = 12 V, VOUT = 1.0 V,			5	A
			F_{SW} = 300 KHz, VIN = 12 V, VOUT = 1.0 V,			8	
Peak Output Current			Duration = 5 S, Period = 10 mS ,			12	A
			F_{SW} = 300 KHz, VIN = 12 V, VOUT = 1.0V, Duration = 10 mS, Period = 1 S,			18	
High & Low Side MOSFET		$R_{DS(ON)}$	V_{GS} = 4.5V		23		mΩ
PWM INPUT							
Maximum Input Current		I_{PWM}	PWM = 5V or 0V			100	μA
PWM Rising Threshold		V_{PWM_Rth}		1.8			V
PWM Falling Threshold		V_{PWM_Fth}				0.4	V
GATE DRIVER TIMINGS							
LS to HS Gate Deadtime		$t_{PD\ HU}$			20		nS
HS to LS Gate Deadtime		$t_{PD\ HL}$			20		nS
EN# INPUT							
EN Input Voltage	Logic-High	V_{EN_H}	VCC = 5V	2	--	--	V
	Logic-Low	V_{EN_L}		--	--	0.48	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Linear Regulator						
Supply Voltage	V_{IN}		5.5	--	23	V
DC Output Voltage Accuracy		I_{LOAD} = 0.1mA	-1		1	%
Dropout Voltage (I_{LOAD} =100mA)	V_{DROP}	V_{OUT} = 5V	--	0.35		V
Ground Current (I_{LOAD} = 0mA)	I_Q	V_{IN} > 5.5V		1.5		μA
Line Regulation	ΔLINE	I_{LOAD} =1mA, 10V ≤ V_{IN} ≤ 20V	--	0.5		%
Load Regulation	ΔLOAD	10mA≤ I_{LOAD} ≤ 0.2A		0.3		%
Output Current Limit	I_{LIM}	V_{OUT} = 0V	501	700		mA
Power Supply Rejection Ratio	PSRR	V_{OUT} = 5V, I_{LOAD} = 30mA, V_{IN} = 12V, f = 1KHz		70		dB
Thermal Shutdown Temperature	T_{SD}	I_{LOAD} = 10mA	--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}			15		°C

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θJA is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Application Guideline

Theory of Operation

The DS9613 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. A PWM input signal is required to control the drive signals to the high−side and low−side integrated MOSFETs.

POR (Power On Reset)

POR block detects the voltage of the VCC pin. When the VCC pin voltage is higher than POR rising hreshold, POR block output is high. POR output is low when VCC is not higher than POR rising threshold. When the POR block output is high, UGATE and LGATE can be controlled by PWM input voltage. If the POR block output is low, both UGATE and LGATE will be pulled to low.

Bootstrap Control

Bootstrap control block controls the integrated bootstrap switch. When LGATE is high (low side MOSFET is turned on), the bootstrap switch is turned on to charge the bootstrap capacitor connected to BOOT pin. When LGATE is low (low side MOSFET is turned off), the bootstrap switch is turned off to disconnect VCC pin and BOOT pin.

Power Supply Decoupling

The DS9613 sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (PVCC) a low−ESR capacitor should be placed near the power and ground pins. A multi−layer ceramic capacitor (MLCC) between 1uF and 4.7uF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1uF ceramic capacitor should be placed on this pin in close proximity to the DS9613. It is good practice to separate the VCC and PVCC decoupling capacitors with a resistor (10 typical) to avoid coupling driver noise to the analog and digital circuits that control the driver function .

Safety Timer and Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The DS9613 and applying the appropriate amount of non−overlap time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). When the PWM input pin is driven high, the gate of the low−side MOSFET goes low after a propagation delay . The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate.

The DS9613 monitors the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer delays the turn−on of the high−side MOSFET. When the PWM input pin goes low, the gate of the high−side MOSFET goes low after the propagation delay . The time to turn off the high−side MOSFET is dependent on the total gate charge of the high−side MOSFET. A timer is triggered once the high−side MOSFET stops conducting, to delay the turn−on of the low−side MOSFET.

Enable and Disable

The DS9613 includes an EN pin for sequence control. When the EN pin rises above the VEN_H trip point, the DS9613 begins a new initialization and follows the PWM command to control the UGATE and LGATE. When the EN pin falls below the VEN_L trip point, the DS9613 shuts down and keeps UGATE and LGATE low.

UVLO	EN#	Driver State
L	X	Disabled (UG = LG = 0)
H	L	Disabled (UG = LG = 0)
H	H	Enabled
H	Open	Enabled

Linear Regulator (LDO) Input and Output Capacitor Requirements

The external input and output capacitors of LDO must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's LDO_IN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1μF and 22μF requirement may be used. Place the output capacitor close to the IC's LDO_OUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Linear Regulator Current Limit

The LDO contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 700mA (typical).

The output can be shorted to ground indefinitely without damaging the part.

Linear Regulator Dropout Voltage

The LDO use a PMOS pass transistor to achieve low dropout. When (LDO_IN – LDO_OUT) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $RDS_{(ON)}$ of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (LDO_IN – LDO_OUT) approaches dropout condition.

Linear Regulator OTP (Over Temperature Protection)

The over temperature protection function of LDO will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.). Once the junction temperature cools down by approximately 15°C, the regulator will automatically resume operation.

PCB Layout Guidelines

DS9613 is a high current module rated for operation up to 1MHz. This requires high switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients.

As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor CIN. The PCB design is greatly simplified by the optimization of the DS9613 pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors CIN should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor , and output capacitor COUT is the next critical requirement.

While DS9613 is a highly efficient module, it still dissipates a significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and LX pads should be attached to large areas of PCB copper. Thermal relief pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins.

A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

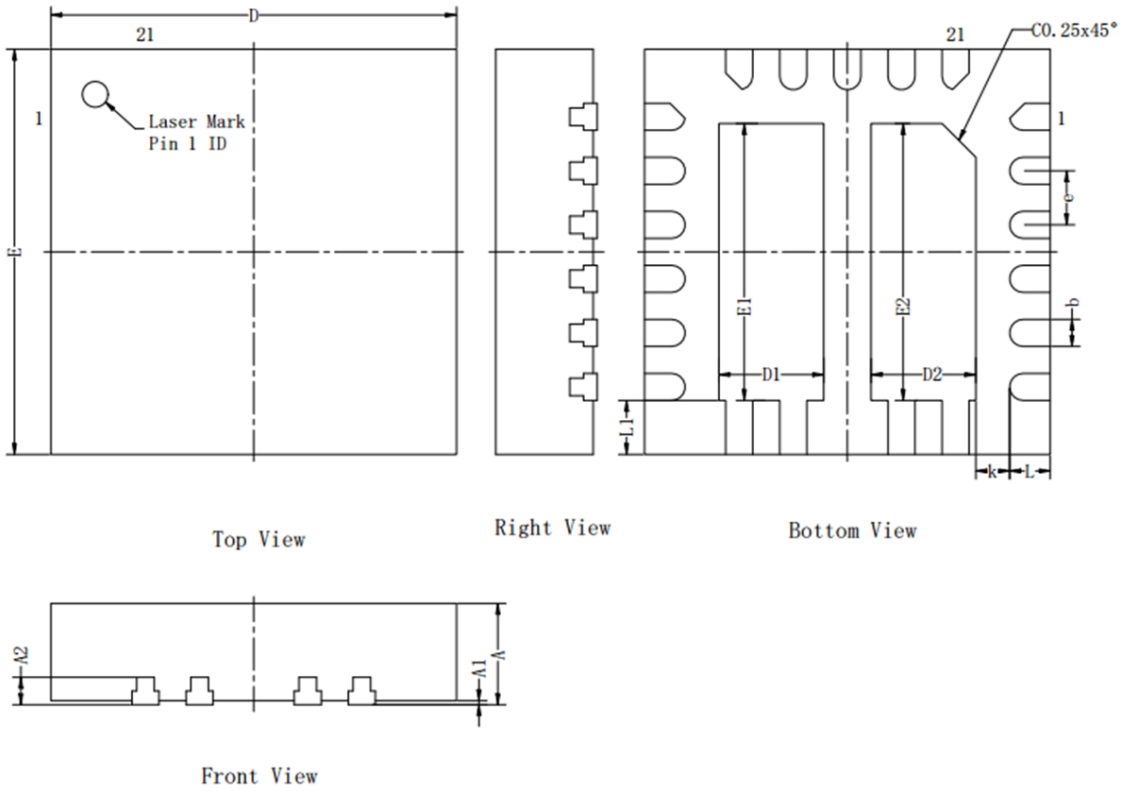
As shown on Figure , the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop which runs along VIN pad originating from the input capacitors hat are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area.

Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

As the primary and secondary (complimentary) AC current loops move through VIN to LX and through PGND to LX, large positive and negative voltage spikes appear at the LX terminal which are caused by the large internal di/dt produced by the package parasitic.

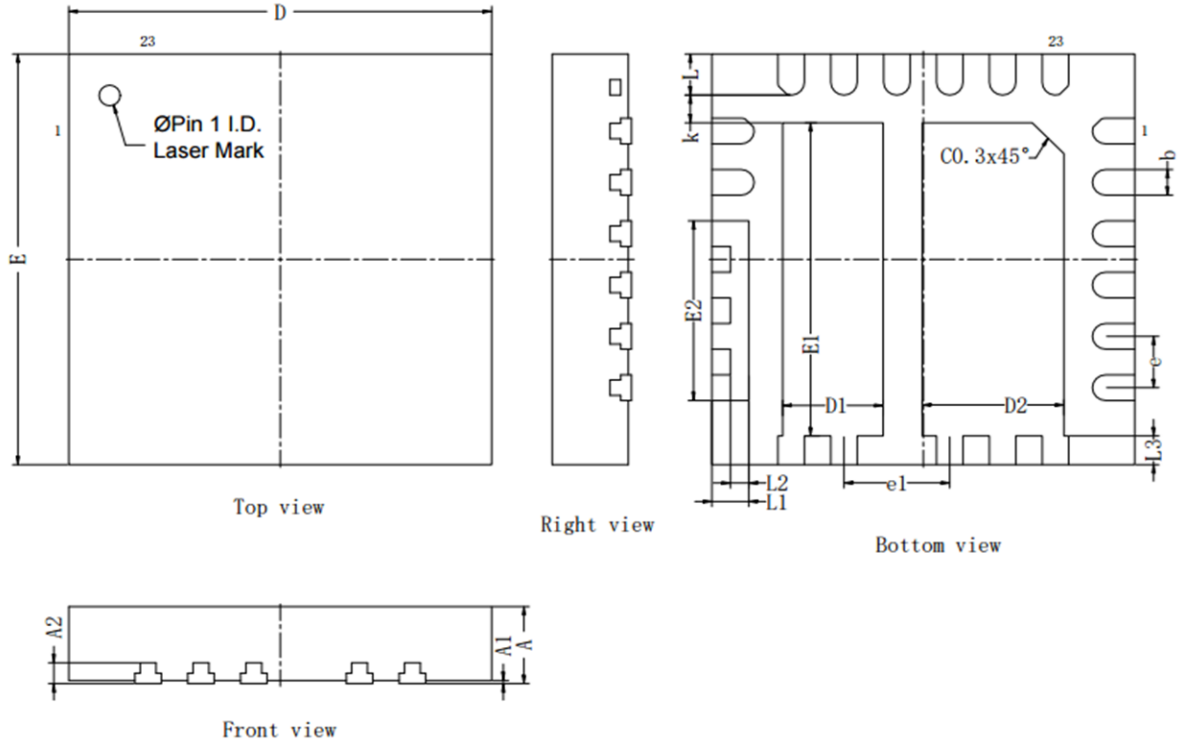
To minimize the effects of this interference at the LX terminal, at which the main inductor is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this LX terminal, only enough so the inductor can be securely mounted.

Package Information:



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	/	0.05
A2		0.203 REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
D1	0.675	0.775	0.875
D2	0.675	0.775	0.875
E	2.90	3.00	3.10
E1	1.95	2.05	2.15
E2	1.95	2.05	2.15
e		0.40 BSC	
k		0.25 REF.	
L	0.20	0.30	0.40
L1	0.30	0.40	0.50

QFN3x3-21L



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	/	0.05
A2		0.203 REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D1	0.85	0.95	1.05
D2	1.24	1.34	1.44
E	3.90	4.00	4.10
E1	2.35	3.05	2.55
E2	1.65	1.75	1.85
e		0.50 BSC	
e1		1.00 BSC	
k		0.27 REF.	
L	0.30	0.40	0.50
L1	0.25	0.35	0.45
L2	0.075	0.175	0.275
L3	0.18	0.28	0.38

QFN4x4-23L