40V, 200mA Low Dropout Voltage Linear Regulator

General Description

The DS8401 series are a group of low-dropout (LDO) voltage regulators offering the benefits of wide input voltage range, low dropout voltage, low power consumption, and miniaturized packaging.

Quiescent current of only $2\mu A$ makes these devices ideal for powering the battery-powered, always-on systems that require very little idle-state power dissipation to a longer service life. There is a shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to only 100nA (typical).

The DS8401 series of linear regulators are stable with the ceramic output capacitor over its wide input range from 2.5V to 40V and the entire range of output load current (0mA to 200mA).

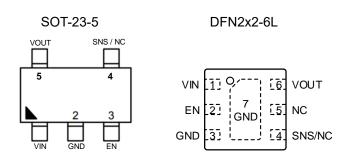
Features

- 2µA Ground Current at no Load
- ±1% Output Accuracy
- 200mA Output Peak Current
- 100nA Disable Current
- Wide Operating Input Voltage Range: 2.5V to 40V
- Dropout Voltage: 0.35V at 100mA / Vout 5V
- Support Fixed Output Voltage 1.8V, 3.3V, 5V, 12V.
- Adjustable Output Voltage Available by Specific Application
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- SOT-23-5 & DFN2x2-6L Package Available

Applications

- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- · Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems
- Industrial Controls
- Weighting Scales
- Meters
- Home Automation

Pin Configurations





Ordering Information

DS8401-AABB

| Designator | Description | Symbol | Description |
|------------|----------------|--------|-------------------------|
| | Output Voltage | 18 | V _{OUT} = 1.8V |
| | | : | |
| AA | | 33 | $V_{OUT} = 3.3V$ |
| | | 50 | V _{OUT} = 5.0V |
| | | A1 | V _{OUT} = 12V |
| ВВ | Package type | S5 | SOT-23-5 |
| | | D6 | DFN2x2-6L |

Special Request : Any Voltage between 1.8V and 12V under specific business agreement .

DS8401N-AABB (For with SNS pin)

| Designator | esignator Description | | Description |
|------------|-----------------------|----|------------------|
| AA | Output Voltage | 18 | $V_{OUT} = 1.8V$ |
| DD | Doolsono tuno | S5 | SOT-23-5 |
| BB | Package type | D6 | DFN2x2-6L |

Notes: $V_{OUT} = (R1 + R2) / R2 \times 1.8 V$, And $R2 < 36 K\Omega$.



Description of Functional Pins

DS8401-AABB

| Pi | n No | Din Name | Din Franchica |
|----------|-------------|----------|--|
| SOT-23-5 | DFN2x2-6L | Pin Name | Pin Function |
| 1 | 1 | VIN | Input of Supply Voltage. |
| 2 | 3 | GND | Ground |
| 3 | 2 | EN | Enable Control Input. |
| 4 | 4,5 | NC | No internal connection |
| 5 | 6 | VOUT | Output of the Regulator |
| | Exposed (7) | SGND | Substrate of Chip. Leave floating or tie to GND. |

${\sf DS8401} \mbox{\bf N-} \mbox{\sf AABB}$ (For with $\mbox{\bf SNS}$ pin)

| Pi | Pin No | | B. E |
|----------|-------------|----------|--|
| SOT-23-5 | DFN2x2-6L | Pin Name | Pin Function |
| 1 | 1 | VIN | Input of Supply Voltage. |
| 2 | 3 | GND | Ground |
| 3 | 2 | EN | Enable Control Input. |
| 4 | 4 | SNS | Sense of Output Voltage. |
| | 5 | NC | No internal connection |
| 5 | 6 | VOUT | Output of the Regulator |
| | Exposed (7) | SGND | Substrate of Chip. Leave floating or tie to GND. |

Typical Application Circuits

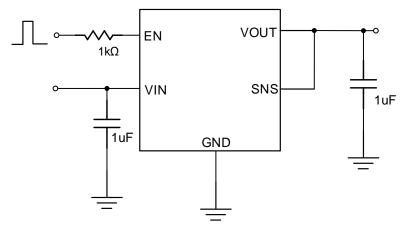


Figure 1: Application circuit of Fixed VouT LDO with enable and sense functions

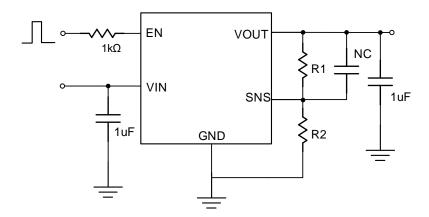


Figure 2: Adjustable output voltage LDO application circuit by DS8401N

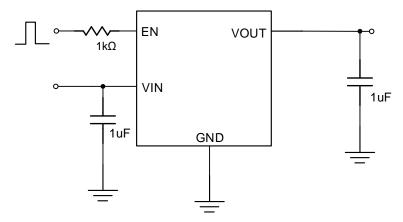
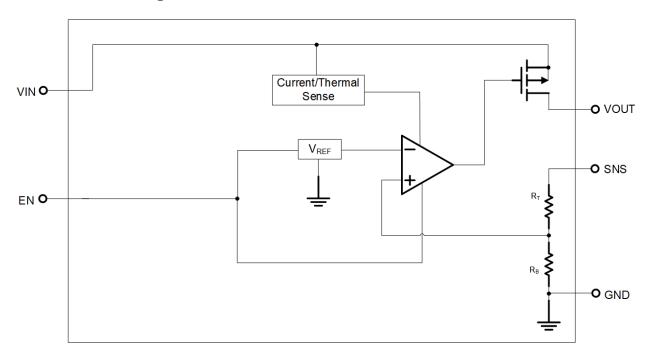


Figure 3: Application circuit of Fixed VOUT LDO with enable function

Function Block Diagram



Absolute Maximum Ratings (Note 1)

| VIN, EN to GND0.3V to 40V |
|--|
| SNS to GND |
| VOUT to GND |
| VOUT to VIN |
| Package Thermal Resistance (Note 2) |
| SOT-23-5, θ _{JA} |
| DFN2x2-6L, θ _{JA} 95 °C /W |
| Lead Temperature (Soldering, 10 sec.) 260 °C |
| Junction Temperature 150 °C |
| Storage Temperature Range40 °C to 150 °C |
| ESD Susceptibility |
| HBM 2KV |
| MM 200V |

Recommended Operating Conditions

| Input Voltage VIN | 2.5V to 36V |
|----------------------------|------------------|
| Junction Temperature Range | -40 °C to 125 °C |
| Ambient Temperature Range | -40 °C to 85 °C |

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Electrical Characteristics

(V_{IN} =15V, V_{EN} =5V, T_A=25°C unless otherwise specified)

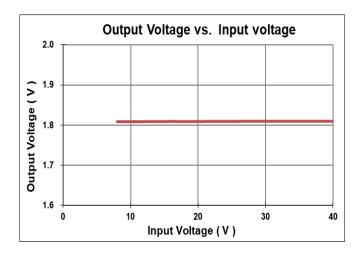
| Parameter | Symbol | Test Conditions | Min | Тур | Max | Unit | |
|--|------------------------|---|-----|------|-----|------|--|
| Supply Voltage | VIN | | 2.5 | | 36 | V | |
| DC Output Voltage Accuracy | | I _{LOAD} =0.1mA | -1 | | 1 | % | |
| | V _{DROP} | V _{OUT} ≥ 5V | | 0.35 | | | |
| Dropout Voltage (I _{LOAD} =100mA) | V _{DROP_3.3V} | V _{OUT} = 3.3V | | 0.38 | | V | |
| | VDROP_1.8V | V _{OUT} = 1.8V | | 0.46 | | | |
| Cround Current (I Om A) | ΙQ | V _{OUT} ≤ 5V | | 2.0 | | | |
| Ground Current (I _{LOAD} = 0mA) | Iqн | 5V < V _{OUT} ≤ 12V | | 3.5 | | μA | |
| Shutdown Ground Current | I _{SD} | V _{EN} = 0V, V _{OUT} = 0V | | 0.1 | 0.5 | μA | |
| SNS Input Current | Isns | SNS = Vout Vout ≤ 5V | | 0.6 | | μA | |
| | VIH | EN Rising | 1.1 | | | | |
| Enable Threshold Voltage | VIL | EN Falling | | | 0.4 | V | |
| EN Input Current | len | V _{EN} = 24V | | 10 | 100 | nA | |
| Line Regulation | ΔLINE | $I_{LOAD} = 1 \text{mA},$ $10 \text{V} \leq V_{IN} \leq 20 \text{V}$ | | 0.8 | | % | |
| Load Regulation | ΔLOAD | 10mA≤ I _{LOAD} ≤ 0.1A | | 0.5 | | % | |
| Output Current Limit | ILIM | V _{OUT} =0 | 201 | 350 | | mA | |
| Power Supply Rejection Ratio | PSRR | V _{OUT} =3.3V, I _{LOAD} =30mA, V _{IN} = 12V, f = 1KHz | | 70 | | dB | |
| Thermal Shutdown Temperature | T _{SD} | 1 40 1 | | 160 | | °C | |
| Thermal Shutdown Hysteresis | ΔT _{SD} | - I _{LOAD} =10mA | | 30 | | °C | |

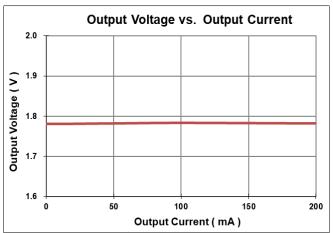
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

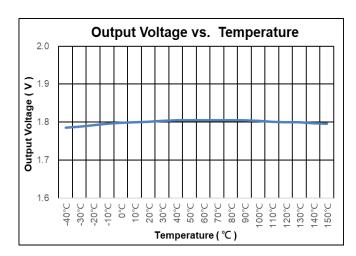
Note 2. θ_{JA} is measured at T_A = 25°C on a DSTECH EVB board.

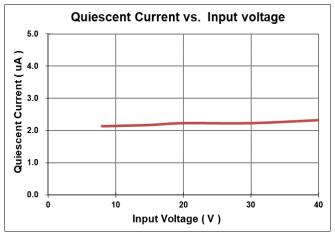
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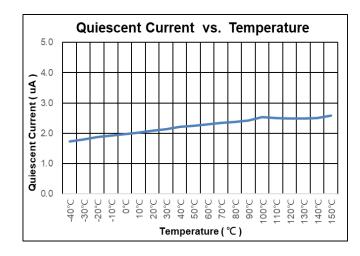
Typical Characteristics

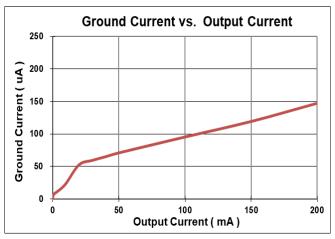


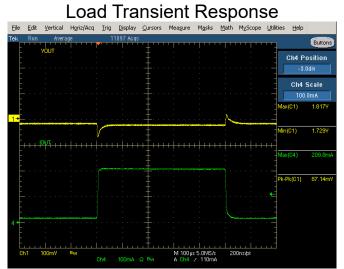


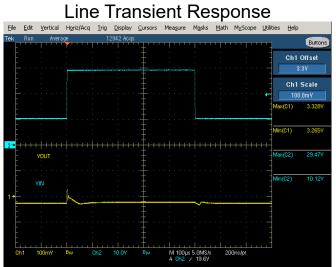








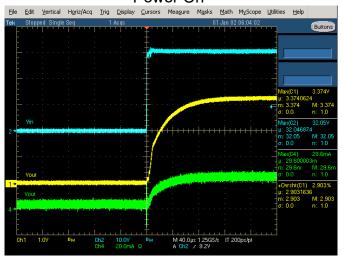




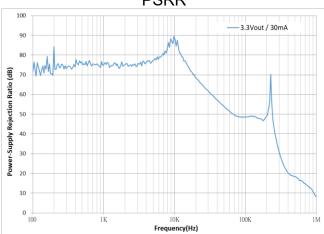
Current Limit



Power On



PSRR



Application Guideline

Input and Output Capacitor Requirements

The external input and output capacitors of DS8401 series must be properly selected for stability and performance. Use a 1µF or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1m Ω ESR (Equivalent Series Resistance) and effective capacitance between 1µF and 22µF requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The DS8401 series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 350mA (typical). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The DS8401 series use a PMOS pass transistor to achieve low dropout. When (VIN-VOUT) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the RDS(ON) of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (VIN-VOUT) approaches dropout condition.

Adjustable Output Voltage Application

The DS8401N with SNS pin also can work as an adjustable output voltage LDO. Figure 2 gives the connections for the adjustable output voltage application. The resistor divider from VOUT to SNS sets the output voltage when in regulation.

The voltage on the SNS pin sets the output voltage and is determined by the values of R1 and R2. In order to keep a good temperature coefficient of output voltage, the values of R1 and R2 should be selected carefully to ignore the temperature effect of input current at the SNS pin. A current greater than 50µA in the resistor divider is recommended to meet the above requirement. The adjustable output voltage can be calculated using the formula given in equation 1:

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{SNS}$$
 (1)

where V_{SNS} is determined by the output voltage selections in the ordering information of DS8401N-18. The maximum adjustable output voltage is 5V. Generally, to maximize the available adjustable output voltage range, DS8401N-18S5 is recommended (V_{SNS} is 1.8V in formula 1 now).

The minimum recommended $50\mu A$ in the resistor divider makes the application no longer a $2\mu A$ low quiescent LDO.

OTP (Over Temperature Protection)

The over temperature protection function of DS8401 series will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, DSTECH PCB,

The max PD (Max) = $(125^{\circ}C - 25^{\circ}C) / (220^{\circ}C/W) = 0.45W$ for SOT-23-5 packages.

The max PD (Max) = $(125^{\circ}C - 25^{\circ}C) / (95^{\circ}C/W) = 1.05W$ for SOT-23-5 packages.

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

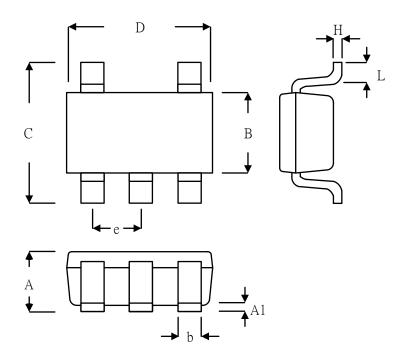
Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the DS8401 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.



Package Information:

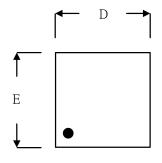


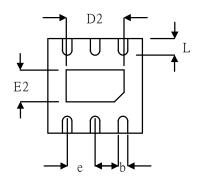
| Symbol | Millim | eters | Inches | |
|---------------|--------|-------|--------|-------|
| D y III O O I | Min. | Max. | Min. | Max. |
| А | 0.889 | 1.295 | 0.035 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| В | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.250 | 0.560 | 0.010 | 0.022 |
| С | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| е | 0.838 | 1.041 | 0.033 | 0.041 |
| Н | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

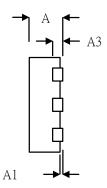
SOT-23-5L

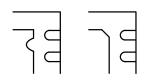
DS8401-P03 http://www.dstech.com.cn/











DETAILAPIN #1 ID and Tie Bar Mark Options

Note: The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Millim | eters | Inches | |
|----------|--------|-------|--------|-------|
| 5 ym 001 | Min. | Max. | Min. | Max. |
| А | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.200 | 0.350 | 0.008 | 0.014 |
| D | 1.950 | 2.050 | 0.077 | 0.081 |
| D2 | 1.000 | 1.450 | 0.039 | 0.057 |
| Е | 1.950 | 2.050 | 0.077 | 0.081 |
| E2 | 0.500 | 0.850 | 0.020 | 0.033 |
| е | 0.650 | | 0.0 | 26 |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

DFN2x2-6L