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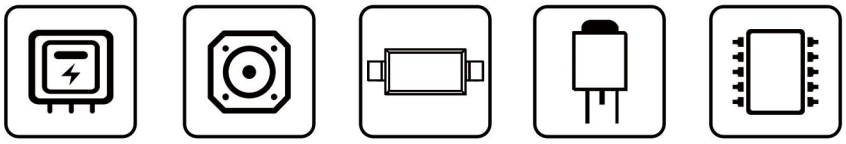
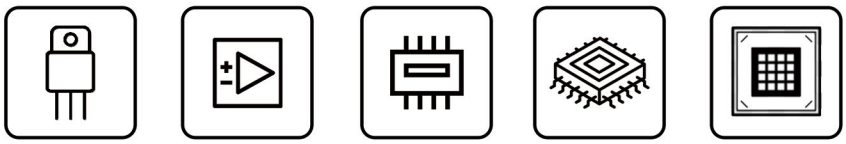




AO4485-TD

產品規格說明書

AO4485-TD
-40V P-Channel Enhancement Mode MOSFET

The JCW015EPC uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = -40V I_D =-12 A

$R_{DS(ON)}$ < 15 mΩ @ V_{GS}=10V

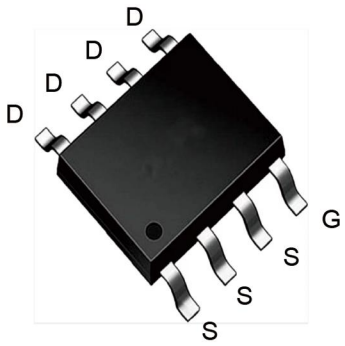
$R_{DS(ON)}$ < 20 mΩ @ V_{GS}=4.5 V

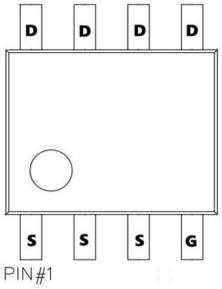
Application

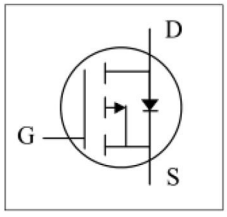
Battery protection

Load switch

Uninterruptible power supply







Package Marking and Ordering Information

Product ID	Package	Marking	QTY(PCS)	Packing methed
AO4485-TD	SOP-8L	AO4485-TD	3000	Reel

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-12	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-10	A
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-10	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ -10V[1]	-8	A
I_{DM}	Pulsed Drain Current[2]	-105	A
EAS	Single Pulse Avalanche Energy[3]	146	mJ
I_{AS}	Avalanche Current	-54	A
P_D@T_C=25℃	Total Power Dissipation[4]	52.1	W
P_D@T_A=25℃	Total Power Dissipation[4]	2	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	2.4	℃/W

AO4485-TD
-40V P-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25℃ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.023	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-12A	---	---	15	mΩ
		V_{GS}=-4.5V , I_D=-10A	---	---	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.6	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.74	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-32V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=-32V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-18A	---	24	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	7	14	
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS}=-4.5V , I_D=-12A	---	27.9	---	nC
Q_{gs}	Gate-Source Charge		---	7.7	---	
Q_{gd}	Gate-Drain Charge		---	7.5	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3 , I_D=-1A	---	40	---	ns
T_r	Rise Time		---	35.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	100	---	
T_f	Fall Time		---	9.6	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	3500	---	pF
C_{oss}	Output Capacitance		---	323	---	
C_{rss}	Reverse Transfer Capacitance		---	222	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-52	A
I_{SM}	Pulsed Source Current[2,5]		---	---	-105	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-54A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

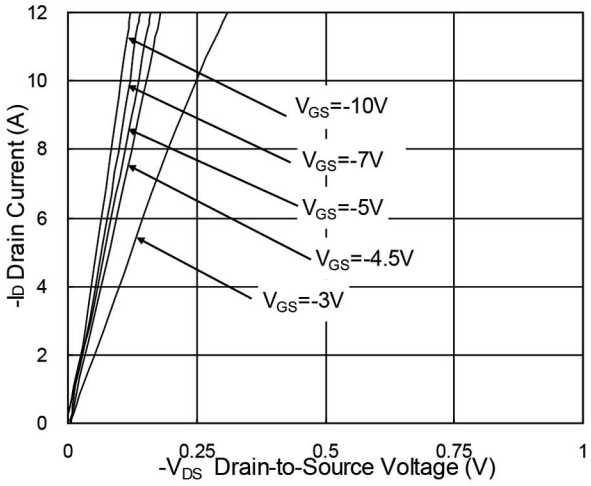


Fig.1 Typical Output Characteristics

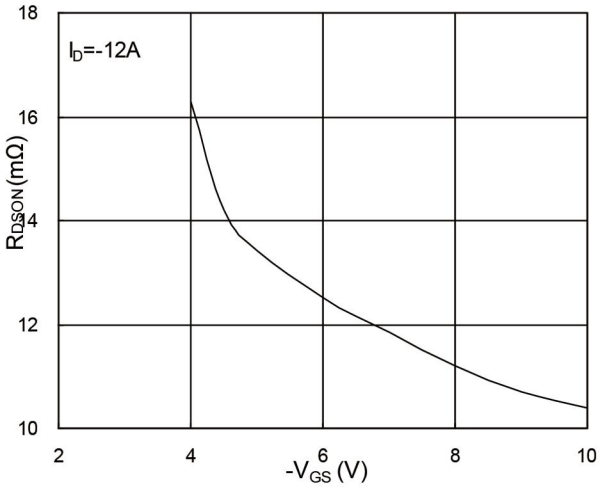


Fig.2 On-Resistance v.s Gate-Source

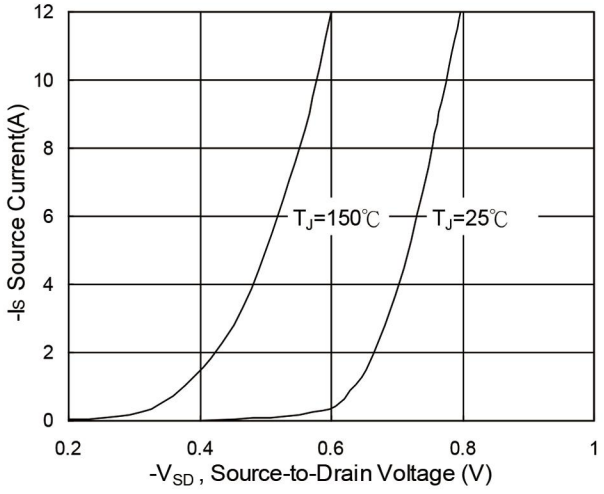


Fig.3 Forward Characteristics Of Reverse

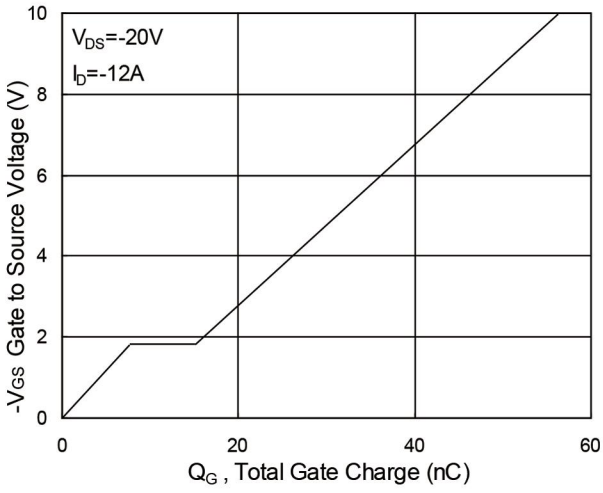


Fig.4 Gate-Charge Characteristics

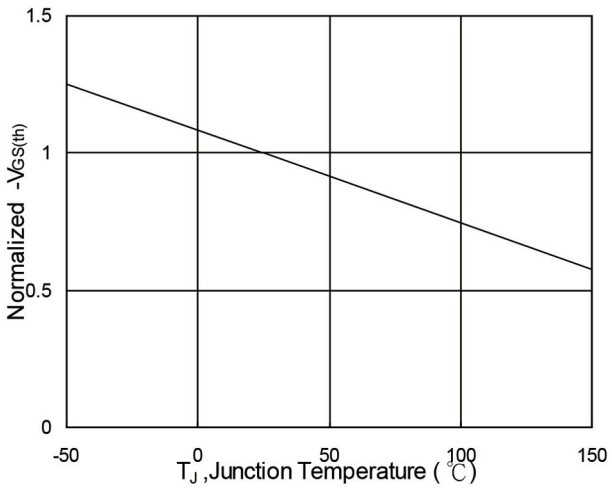


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

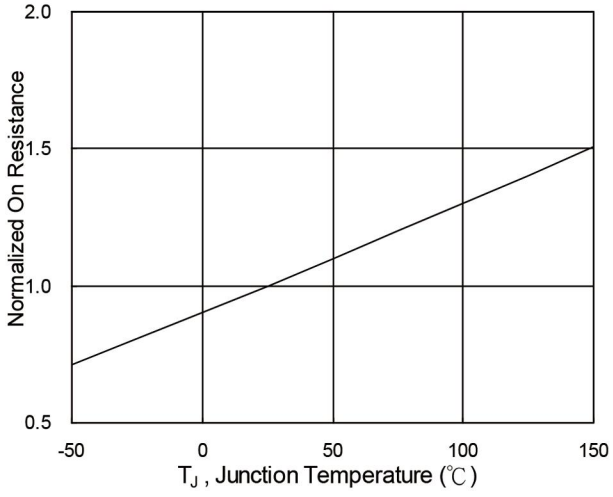


Fig.6 Normalized R_{DSON} v.s T_J

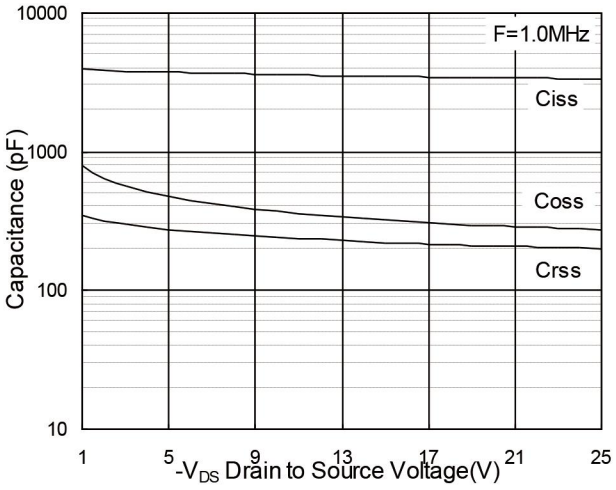


Fig.7 Capacitance

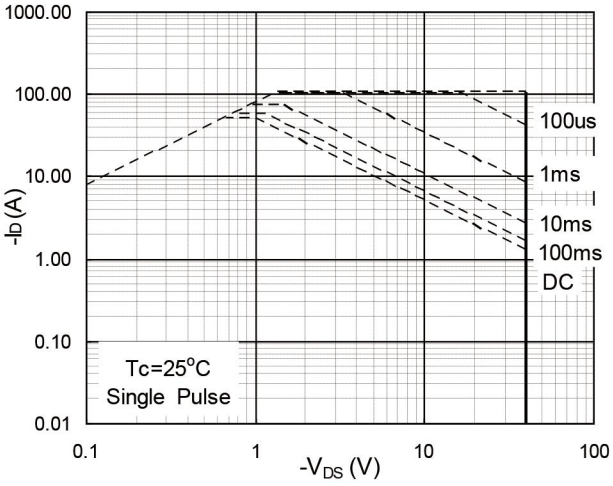


Fig.8 Safe Operating Area

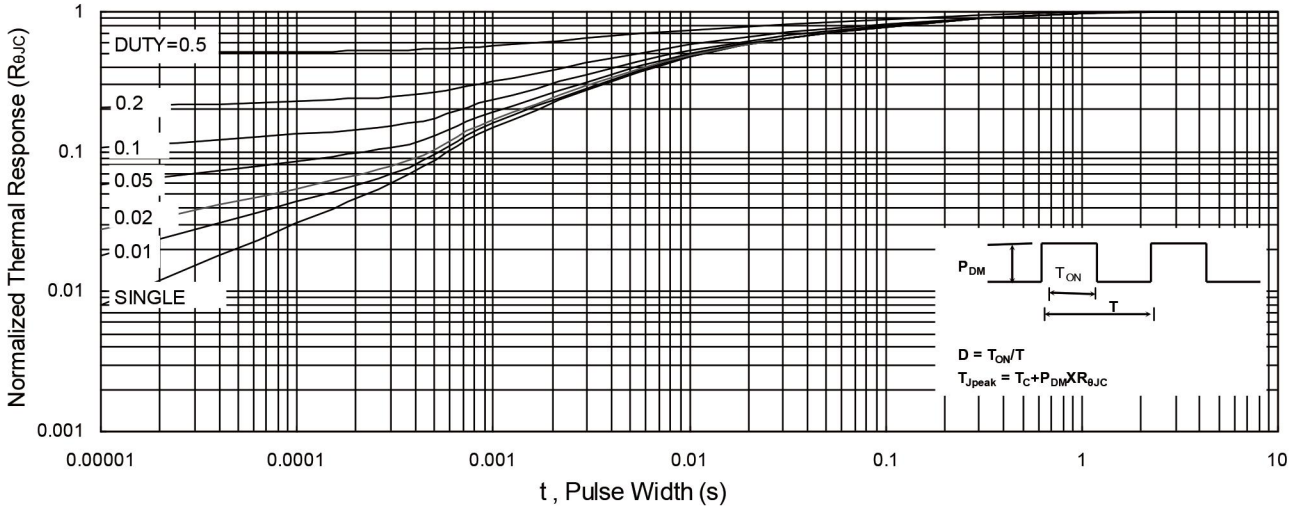


Fig.9 Normalized Maximum Transient Thermal Impedance

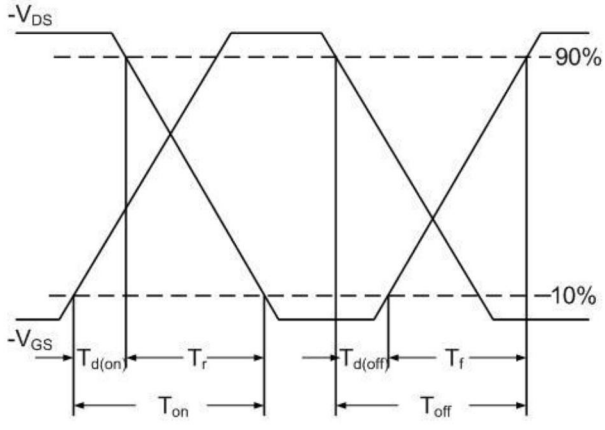


Fig.10 Switching Time Waveform

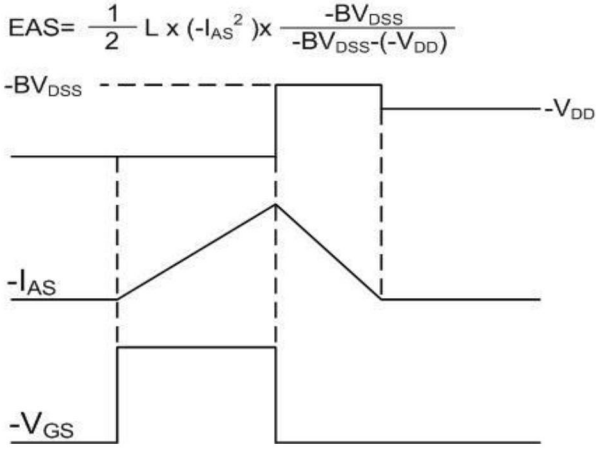
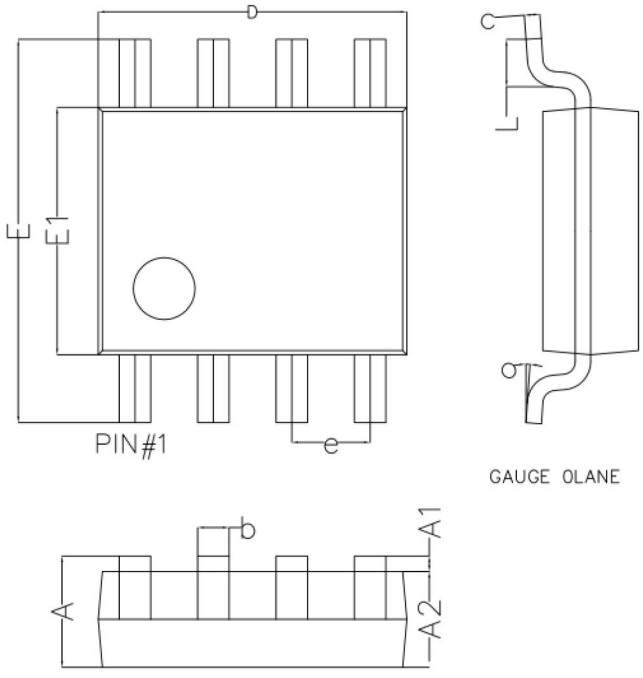


Fig.11 Unclamped Inductive Waveform

PACK SOP-8

SOP8 Package outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270(BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°