3-Phase 200V Half Bridge Driver

General description:

The XJNG2302 is a three-phase gate driver IC which can be used to driver power MOSFETs in the high- and low-side or half bridge configuration. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 200 V.

Application

- Three phase DC brushless motor driver
- Industrial motor control

Features:

- Fully operational to +200 V
- dV/dt Immunity ±50 V/nsec
- Typically - 9V negative Vs bias capability
- Gate drive supply range from 7 V to 20 V
- 3.3V/5V input logic compatible
- UVLO for all channels
- Cross-conduction prevention logic
- Typically Source/Sink current capability 1.5A/1.8A

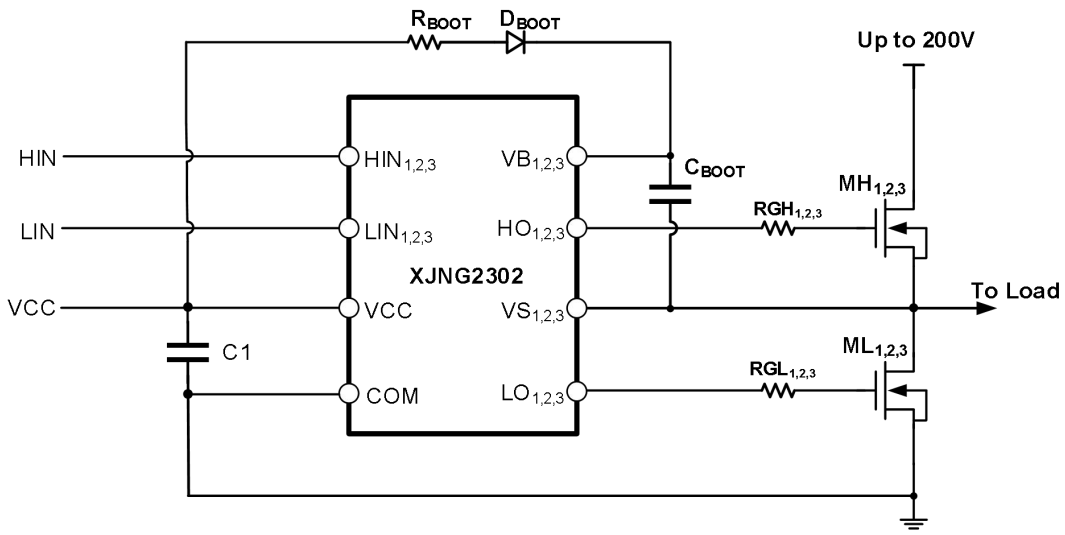
Package top view

TSSOP-20

Package Marking and Ordering Information

Device	Order code	Device Package	Device Marking
XJNG2302	XJNG2302	TSSOP-20	XJNG2302

Typical Application Circuit



Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply	-0.3	225	V
$V_{S1,2,3}$	High side floating supply return	V_B – 25	V_B + 0.3	V
$V_{HO1,2,3}$	High side gate drive output	V_S -0.3	V_B + 0.3	V
V_{CC}	Low side and main power supply	-0.3	25	V
$V_{LO1,2,3}$	Low side gate drive output	-0.3	V_{CC} + 0.3	V
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	V
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package Power Dissipation @ TA ≤25°C (TSSOP-20)	—	1.25	W
Rth_{JA}	Thermal Resistance Junction to Ambient (TSSOP-20)	—	100	°C /W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	°C
ESD	HBM Model	1500	—	V
	CDM Model	500	—	V

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply	V_S + 7	V_S + 20	V
$V_{S1,2,3}$	High side floating supply return	-9	200	V
$V_{HO1,2,3}$	High side gate drive output	V_S	V_B	V
$V_{CC1,2,3}$	Low side and main power supply	7	20	V
$V_{LO1,2,3}$	Low side gate drive output	0	V_{CC}	V
V_{IN}	Logic input of HIN & LIN	0	V_{CC}	V
T_A	Ambient temperature	-40	125	°C

Dynamic Electrical Characteristics

VBIAS (VCC, VBS) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified

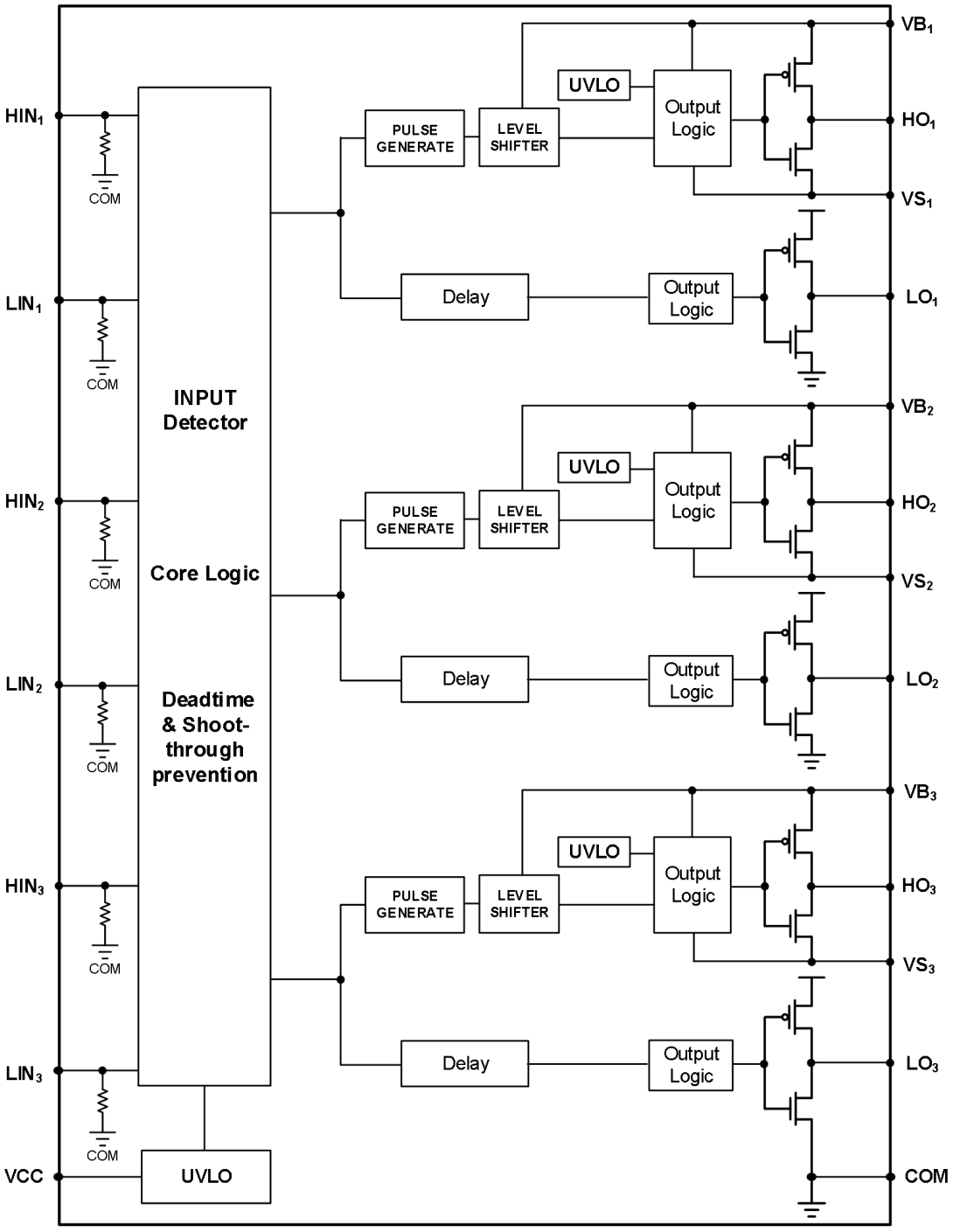
Symbol	Definition	Min.	Typ.	Max.	Units
t_{ON}	Turn on propagation delay	—	150	250	ns
t_{OFF}	Turn off propagation delay	—	120	250	ns
MT	Delay matching time (t_{ON}, t_{OFF})	—	--	50	ns
DT	Dead time	100	200	300	ns
t_R	Turn on rising time	—	30	—	ns
t_F	Turn off falling time	—	30	—	ns

Static Electrical Characteristics

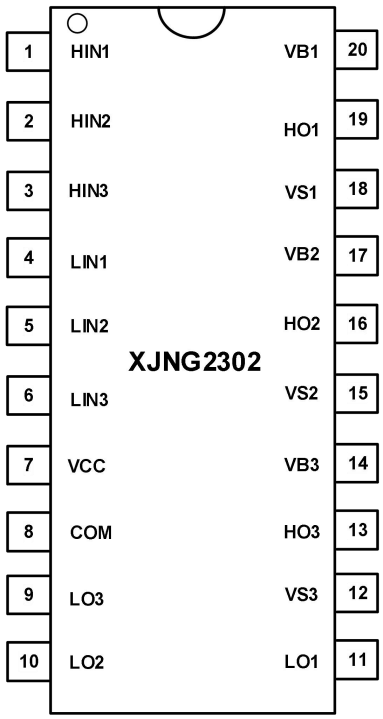
VBIAS (VCC, VBS) = 15V, CL = 1000 pF and TA = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units
V_{IH}	High level input threshold voltage	2.5	—	—	V
V_{IL}	Low level input threshold voltage	—	—	0.8	V
V_{CCUV+}	VCC supply undervoltage positive going threshold	6.4	7	7.6	V
V_{CCUV-}	VCC supply undervoltage negative going threshold	5.9	6.5	7.1	V
V_{CCHYS}	VCC supply under voltage hysteresis	—	0.5	—	V
V_{BSUV+}	VBS supply undervoltage positive going threshold	6.4	7.1	7.7	V
V_{BSUV-}	VBS supply undervoltage negative going threshold	6.2	6.9	7.5	V
V_{BSHYS}	VBS supply under voltage hysteresis	—	0.2	—	V
I_{LK}	High-side floating supply leakage current	—	—	90	μA
I_{QBS}	Quiescent V_{BS} supply current	—	70	150	μA
I_{QCC}	Quiescent V_{CC} supply current	—	230	350	μA
I_{IN+}	Input bias current (HO/LO = "1")	—	25	50	μA
I_{IN-}	Input bias current (HO/LO = "0")	—	—	2	μA
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	—	0.6	—	V
V_{OL}	Low level output voltage drop, V_O	—	0.3	—	V
V_S	VS Negative voltage	—	-9	—	V
I_{O+}	Output High short circuit pulsed current	—	1.5	—	A
I_{O-}	Output low short circuit pulsed current	—	1.8	—	A

Function Block Diagram

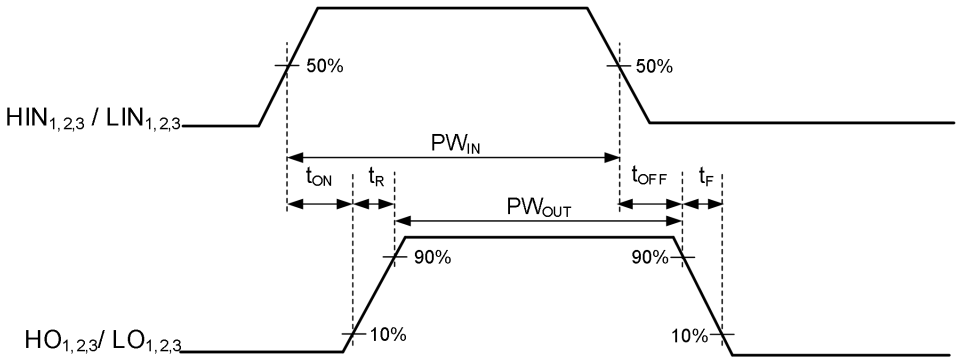


Pin Configuration

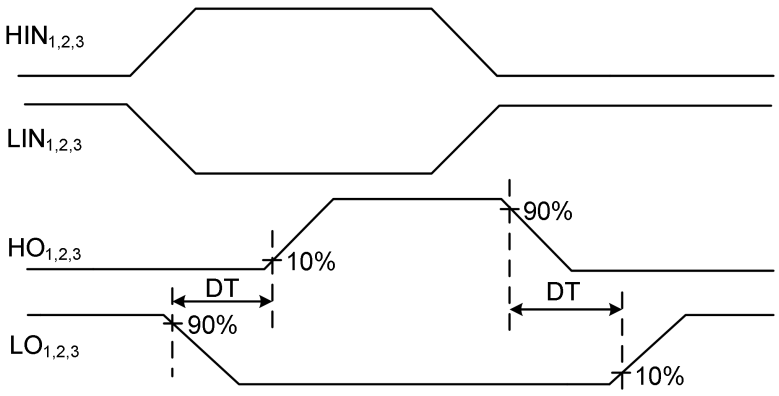


Pin No.	Pin Name	Pin Function
1, 2, 3	HIN1, HIN2, HIN3	Logic input for high side gate driver output (HO)
4, 5, 6	LIN1, LIN2, LIN3	Logic input for low side gate driver output (LO)
7	V_{CC}	Low side and main power supply
8	COM	Ground
9,10,11	LO1, LO2, LO3	Low side gate drive output, out of phase with LIN
12,15,18	VS1, VS2, VS3	High side floating supply return or bootstrap return
13,16,19	HO1, HO2, HO3	High side gate drive output, in phase with HIN
14,17,20	VB1, VB2, VB3	High side floating supply

Function Timing Diagram



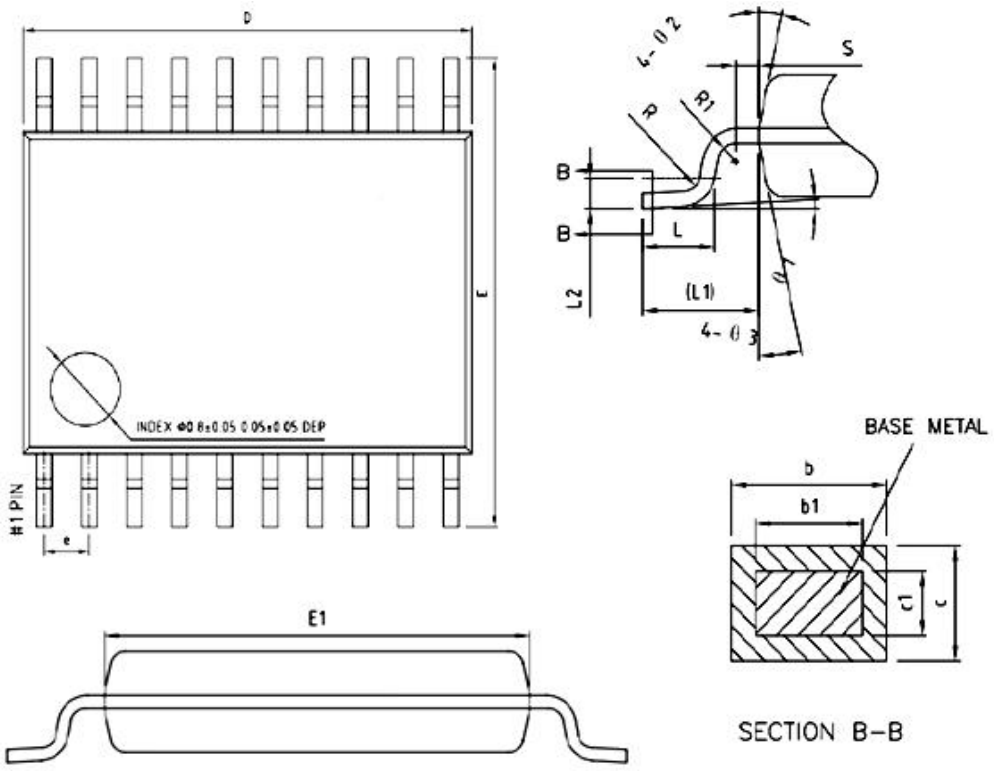
Switching Time Waveform Definition

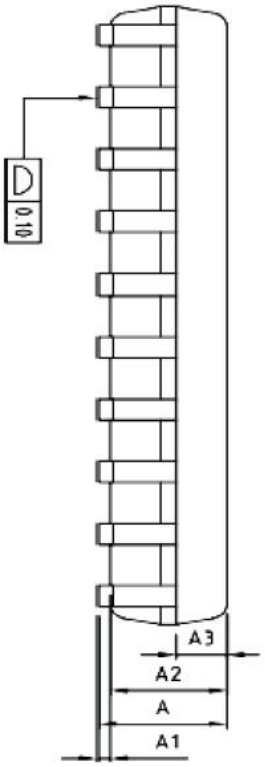


Cross Conduction Prevention Delay Time Waveform Definition

Package Information

TSSOP-20 Package Outlines





	MIN(mm)	NOM(mm)	MAX(mm)
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

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