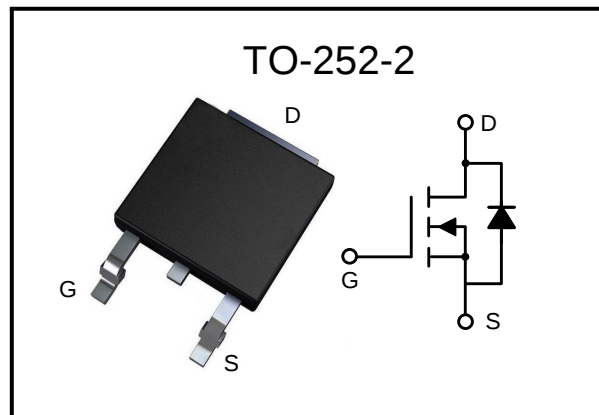


Features

- $V_{BR(DSS)}=100V$
- $I_D=15A$
- $R_{DS(ON)}@10V,TYP=88m\Omega$
- Trench Technology Power MOSFET
- Low $R_{DS(ON)}$
- Low Gate Charge
- Low Gate Resistance

Package



Application

- Power Switching Application
- SMPS 2nd Synchronous Rectifier
- MB/VGA Vcore
- Lighting

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter		Value	Units
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate - Source Voltage		± 20	
I_D	Drain Current	$T_C=25^{\circ}C$	15	A
		$T_C=100^{\circ}C$	8.5	
		$T_A=25^{\circ}C$	5	
I_{DM}	Drain Current-Pulse ⁽¹⁾		60	A
I_{AS}	Single Pulsed Avalanche Current		12.5	A
E_{AS}	Single Pulsed Avalanche Energy		16	mJ
P_D	Power Dissipation	$T_C=25^{\circ}C$	34.5	W
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient		50	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance From Junction to Case		3.6	$^{\circ}C/W$
T_J	Junction Temperature		150	$^{\circ}C$
T_{stg}	Storage Temperature Range		-55 to +150	$^{\circ}C$



Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D=250\mu A$	100	—	—	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS}=0V$	—	—	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS}=0V$	—	—	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D=250\mu A$	1.0	1.5	2.5	V
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=12A$	—	88	110	$m\Omega$
		$V_{GS}=4.5V, I_D=8A$	—	96	140	$m\Omega$
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=4.5A$	—	13	—	S
Dynamic Characteristics						
Input capacitance	C_{iss}	$V_{DS} = 25V,$ $V_{GS} = 0V,$ $f = 1MHz$	—	890	—	pF
Output capacitance	C_{oss}		—	60	—	
Reverse transfer capacitance	C_{rss}		—	25	—	
Static Drain-source On Resistance	R_g	$V_{GS}=V_{DS}=0V, f=1MHz$	—	1.5	—	Ω
Switching Characteristics						
Turn-on delay time	$T_{d(on)}$	$V_{DD}=25V,$ $V_{GS}=10V,$ $R_G = 1\Omega,$ $R_L = 5\Omega$	—	14.2	—	nS
Turn-on Rise time	T_r		—	33.7	—	
Turn -Off Delay Time	$T_{d(off)}$		—	40.2	—	
Turn -Off Fall time	T_f		—	6	—	
Gate to Drain Charge	Q_g	$V_{DS}=80V,$ $V_{GS}=10V,$ $I_D=10A$	—	24	—	nC
Gate to Source Charge	Q_{gs}		—	5	—	
Gate to Drain Charge	Q_{gd}		—	8	—	
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=1A$	—	—	1.2	V
Continuous Source Current	I_S	—	—	12	—	A
Pulsed Source Current	I_{SM}		—	24	—	
Reverse Recovery Time	T_{rr}	$I_F=4.5A, d_{IF}/d_t=500A/\mu s$	—	21	—	ns
Reverse Recovery Charge	Q_{rr}		—	27.3	—	nC

Notes:

(1) Pulse Test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 1.5\%$, Starting $T_J = 25^{\circ}\text{C}$.



Typical Characteristics

Figure 1 : Typical Output Characteristics

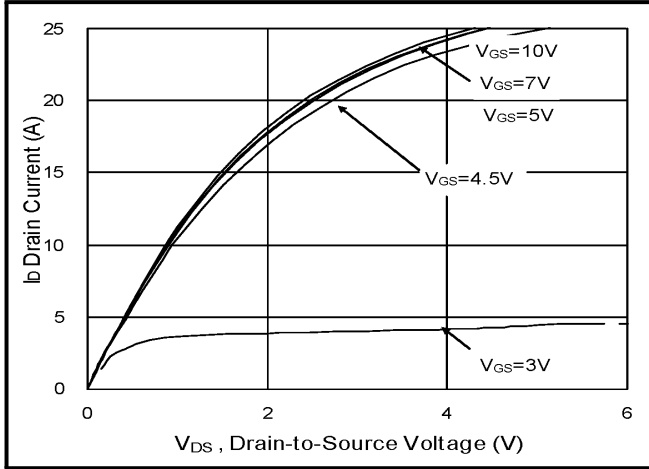


Figure 2 : On-Resistance vs. Gate-Source

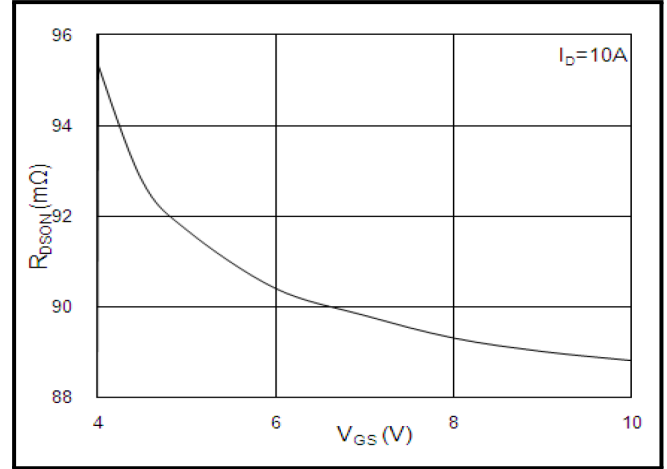


Figure 3 : Forward Characteristics Of Reverse

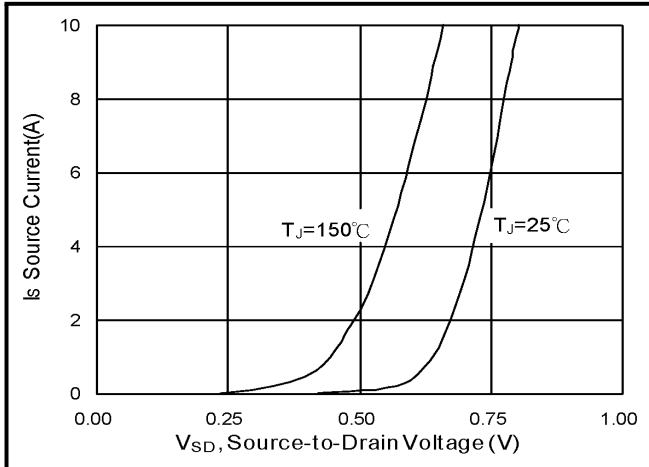


Figure 4 : Gate-Charge Characteristics

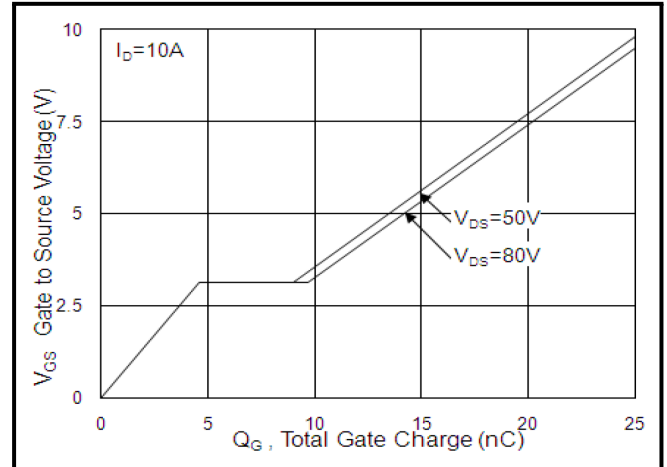


Figure 5 : Normalized VGS(th) vs. TJ

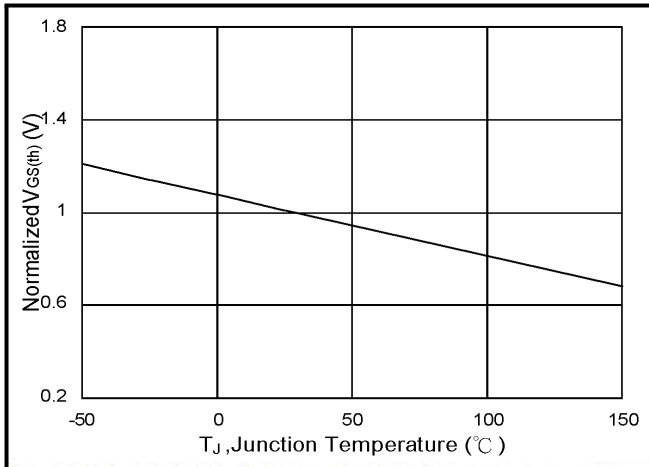
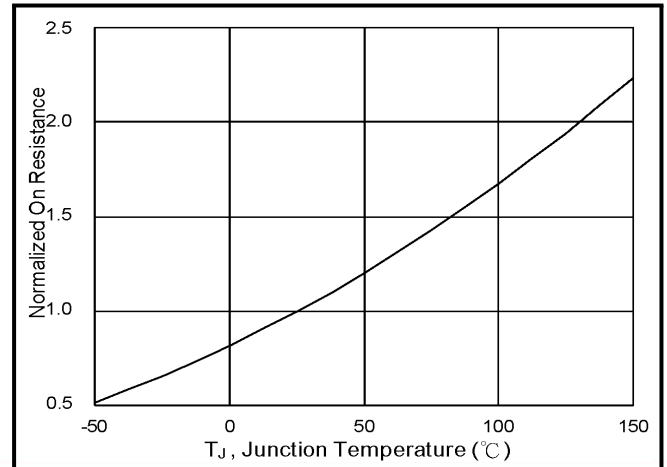


Figure 6 : Normalized RDSON vs. TJ



Typical Characteristics

Figure 7 : Capacitance

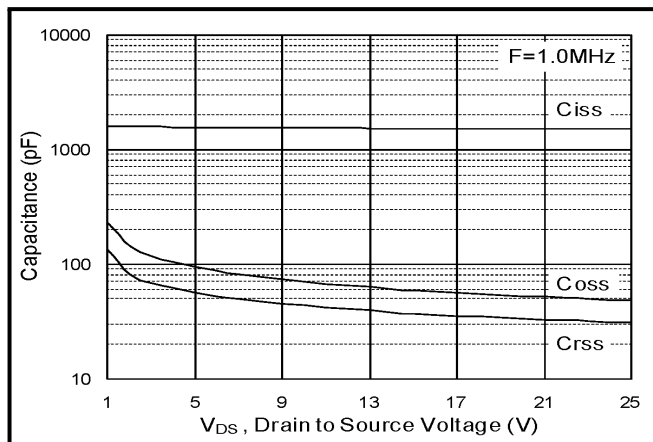


Figure 8 : Safe Operating Area

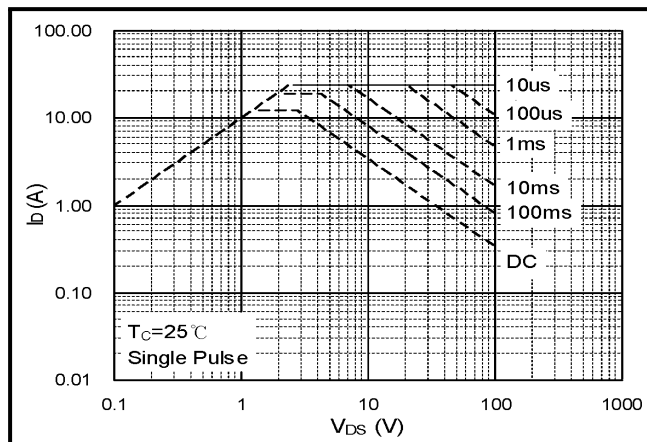
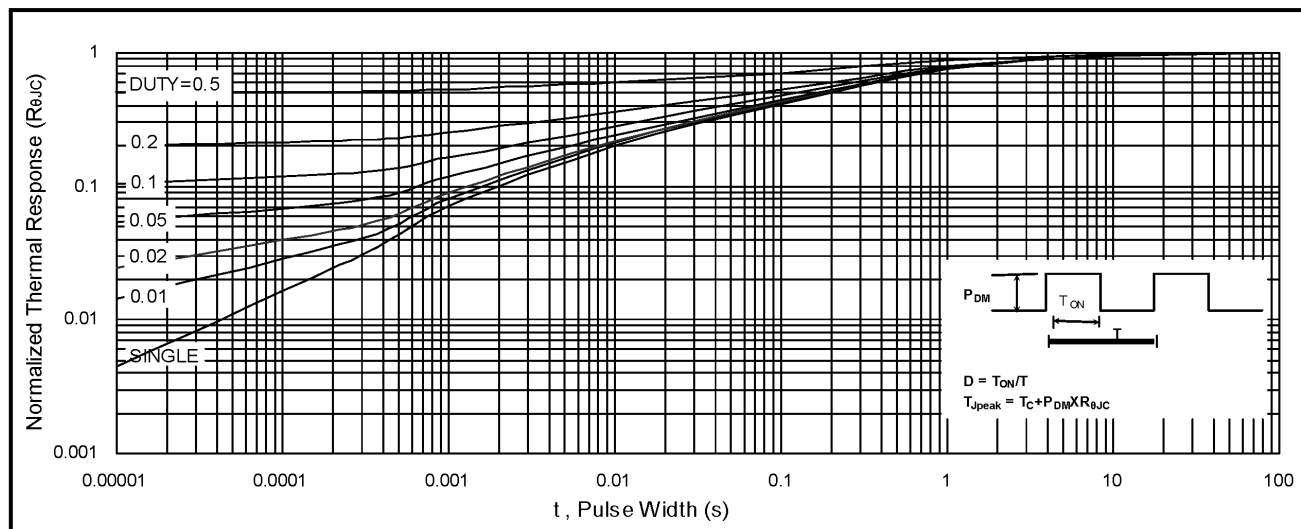


Figure 9 : Normalized Maximum Transient Thermal Impedance



Test Circuit

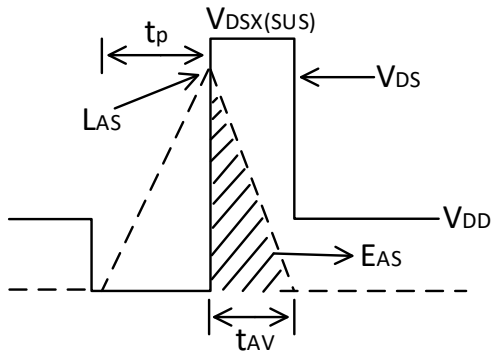


Fig 1.EAS Test Circuit

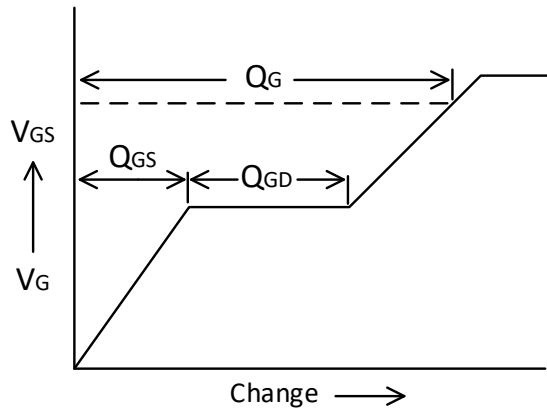
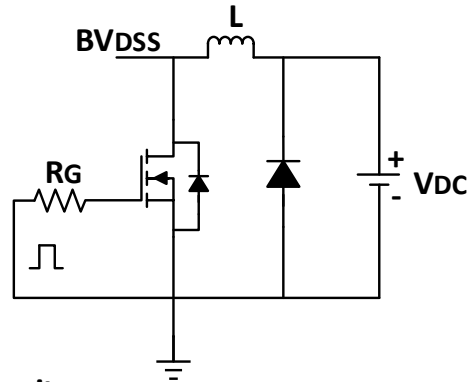


Fig 2.Gate Charge Test Circuit

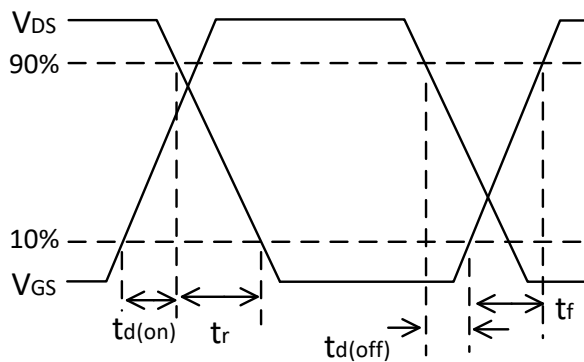
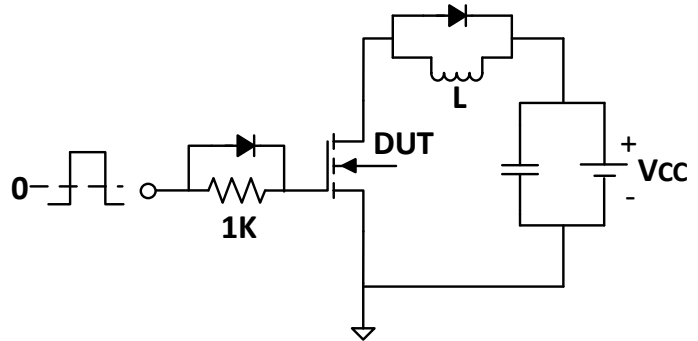
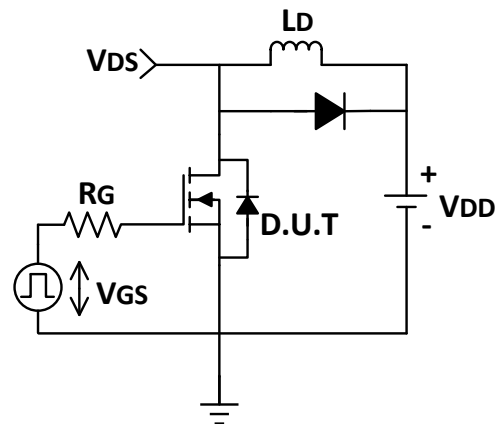
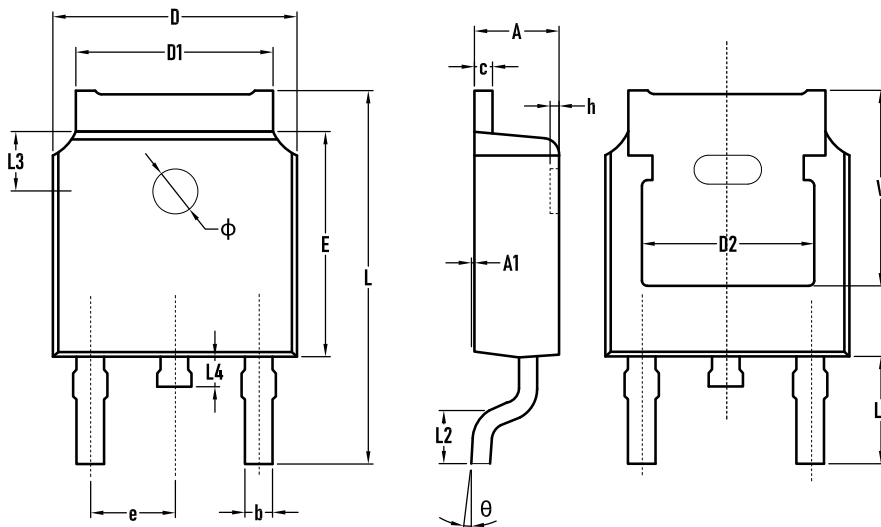


Fig 3 . Switch Time Test Circuit





SYMBOL	Millimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

