GOODWORK

AO4485

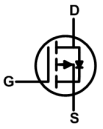
P-Ch 40V Fast Switching MOSFETs

General Description

The AO4485 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The AO4485 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

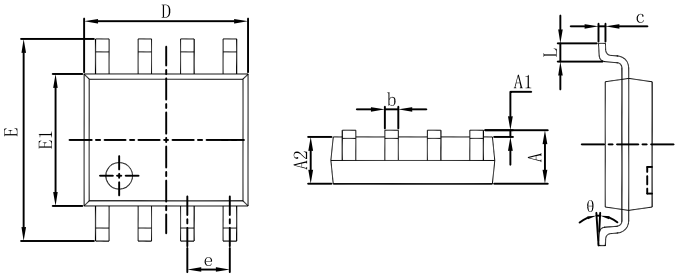
100% EAS Guaranteed
Green Device Available
Super Low Gate Charge
Excellent CdV/dt effect decline
Advanced high cell density Trench technology



Product Summary

BVDSS	RDSON	ID
-40V	14 mΩ	-13 A

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Absolute Maximum Ratings (T_A= 25°C, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	-13	A
	T_A=100°C		-8.5	
Pulsed Drain Current[1]		I_{DM}	-52	A
Single Pulse Avalanche Energy[2]		EAS	80	mJ
Total Power Dissipation	T_A=25°C	P_D	3	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	41	°C/W

AO4485

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25℃	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	-	-	-1	μA
	T_J=100℃			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.5	-2.2	V
Drain-Source On-Resistance[4]		$R_{DS(on)}$	V_{GS} = -10V, I_D = -10A	-	14.0	19	mΩ
			V_{GS} = -4.5V, I_D = -5 A	-	19.5	25	
Forward Transconductance[4]		g_{fs}	V_{DS} = -10V, I_D = -10A	-	44	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = -20V, V_{GS} =0V, f =1MHz	-	2525	-	pF
Output Capacitance		C_{oss}		-	190	-	
Reverse Transfer Capacitance		C_{rss}		-	172	-	
Gate Resistance		R_g	f =1MHz	-	10	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = -10V,V_{DS} = -20V, I_D= -10A	-	35	-	nC
Gate-Source Charge		Q_{gs}		-	5.5	-	
Gate-Drain Charge		Q_{gd}		-	8	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} = -10V, V_{DD} = -20V, R_G = 3Ω, I_D= -10A	-	14.5	-	ns
Rise Time		t_r		-	20.2	-	
Turn-Off Delay Time		$t_{d(off)}$		-	32	-	
Fall Time		t_f		-	10	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = -10A, V_{GS} = 0V	-	-	-1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	-13	A

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -34A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

RATING AND CHARACTERISTIC CURVES (AO4485)

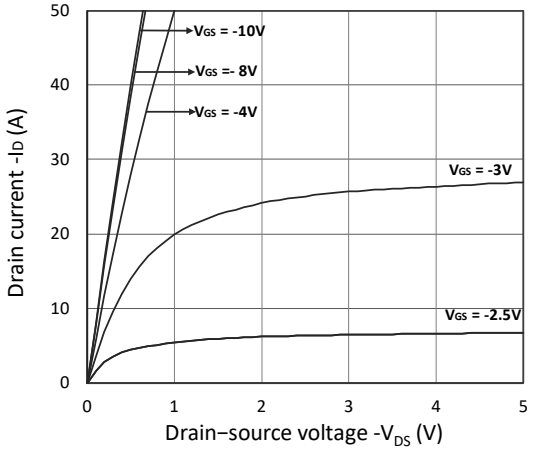


Figure 1. Output Characteristics

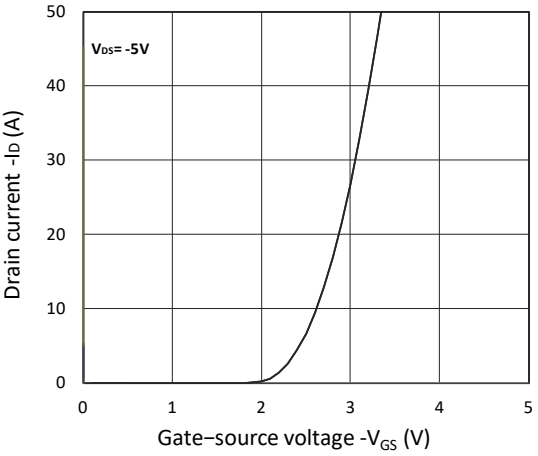


Figure 2. Transfer Characteristics

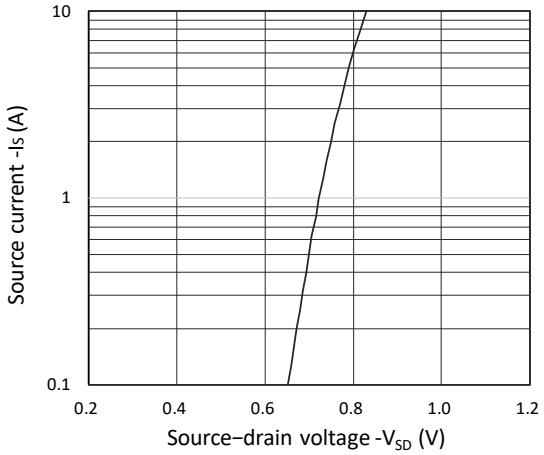


Figure 3. Forward Characteristics of Reverse

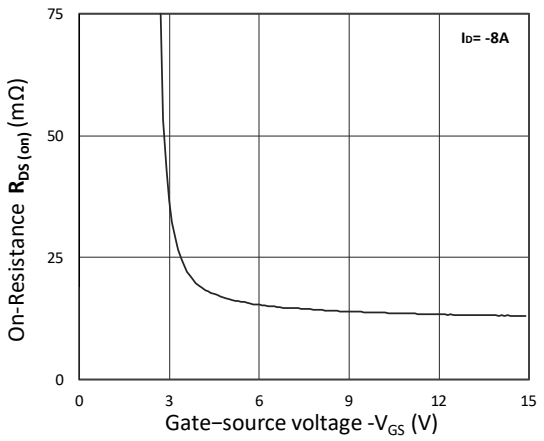


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

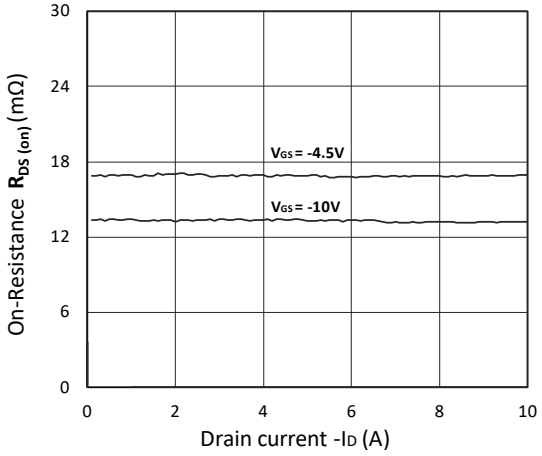


Figure 5. $R_{DS(ON)}$ vs. I_D

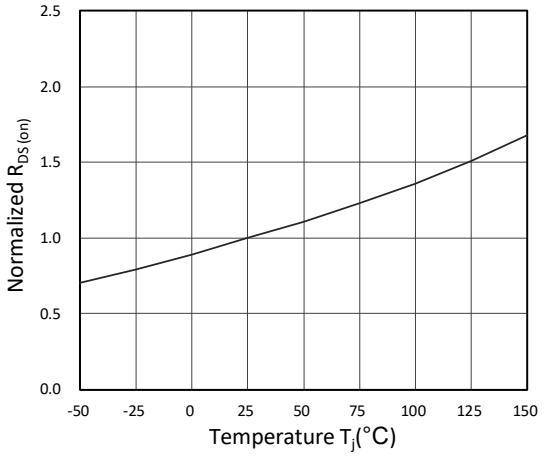


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

RATING AND CHARACTERISTIC CURVES (AO4485)

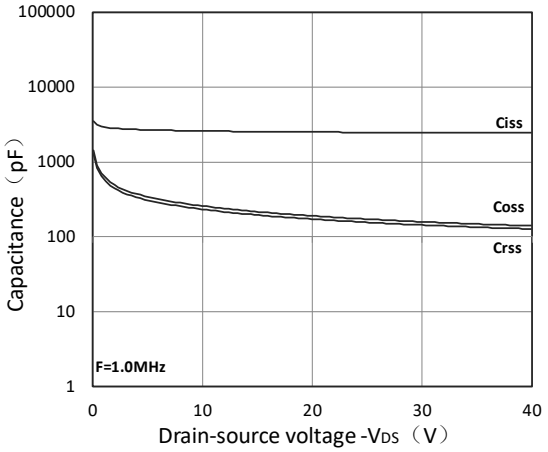


Figure 7. Capacitance Characteristics

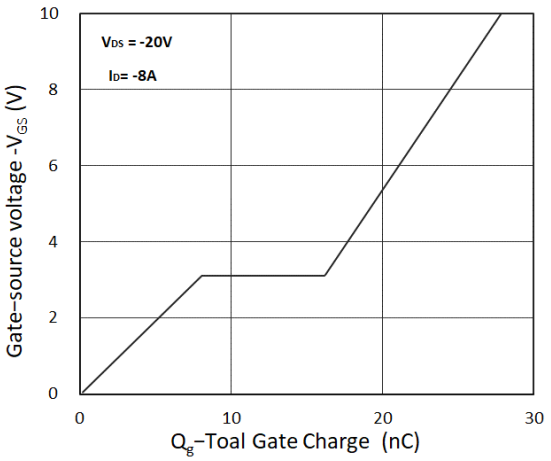


Figure 8. Gate Charge Characteristics

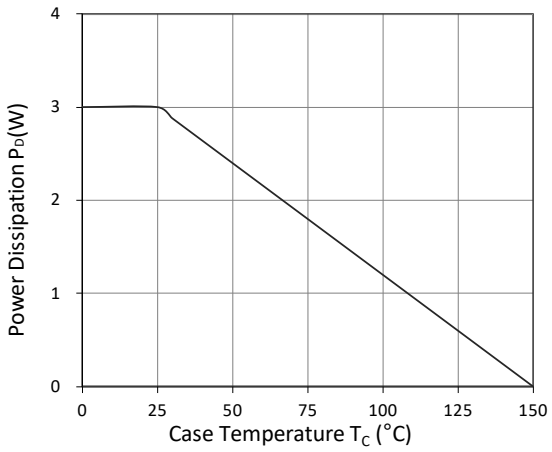


Figure 9. Power Dissipation

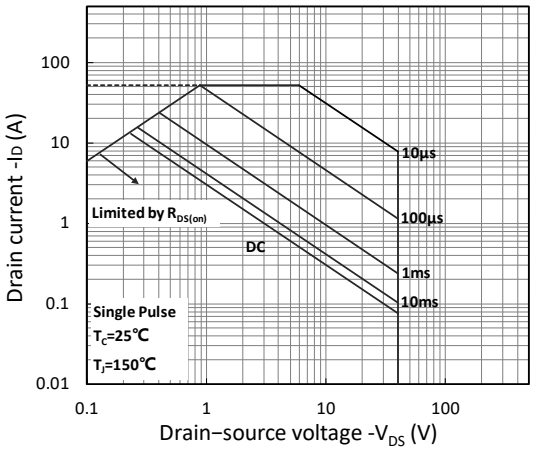


Figure10. Safe Operating Area

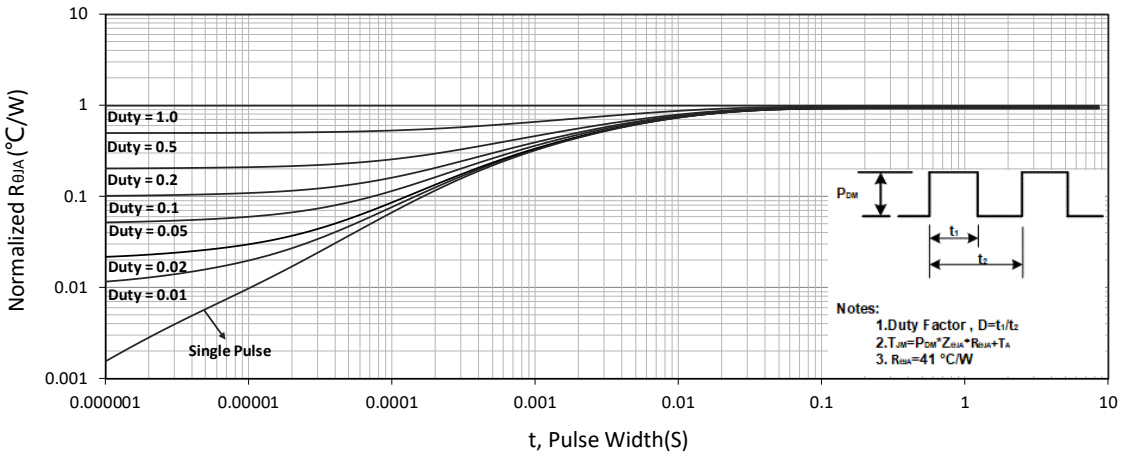


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

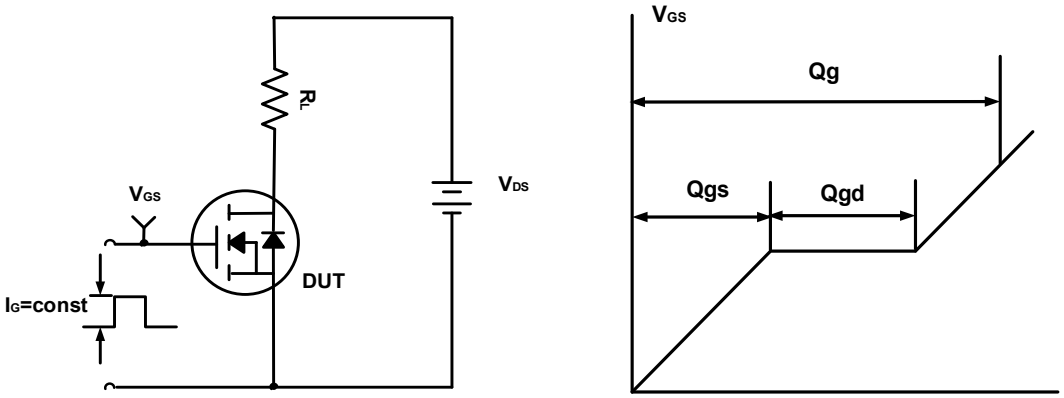


Figure A. Gate Charge Test Circuit & Waveforms

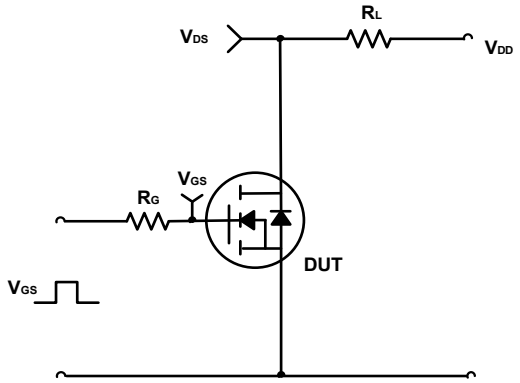


Figure B. Switching Test Circuit & Waveforms

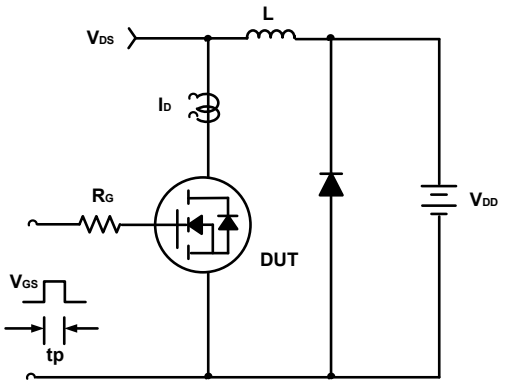


Figure C. Unclamped Inductive Switching Circuit & Waveforms