High Resolution OIS controller

Features

- 4-ch closed-loop control
- ARM 32-bit STARCU with FPU and DSP，frequency up to 96MHz
- 128KB Flash, SRAM: 64KB for program and 16KB for data, 8KB ROM
- Analog: V_{AVDD} = 2.6V to 3.6V,
  Driver: V_{VM} = 1.8V to 3.6V,
  I/O: V_{IOVDD} = 1.1V to 3.6V
- Current type linear driver (4-ch,12-bit), default Imax. = ±160mA,
  Imax can support ±215mA
- PGA (8-ch), support 4-ch differential signal input or 8-ch single-ended signal input
- Each PGA offset(8-ch,10bit DAC) independently adjustable
- PWM driver, support 4-ch current or 4-pairs voltage modulated output
- Sigma-delta ADC(13-ch),
  configurable 12/14/16bit resolution.
- DAC(4-ch,8bit), Hall bias current: 0 to 4mA,
- DAC(4-ch,8bit),TMR bias voltage: 1.2 to 2.5V
- SPI (2-ch), configurable master / slave / monitor mode, configurable 3/4 wire bus
- I2C(2-ch), configurable master / slave mode
- Support I3C slave and UART
- Support Hardware Cordic and Digital Filter

Applications

- Mobile phones / VR / AR / UAV
- Camcorder / Web camera
- Digital Still camera / Security camera

General Description

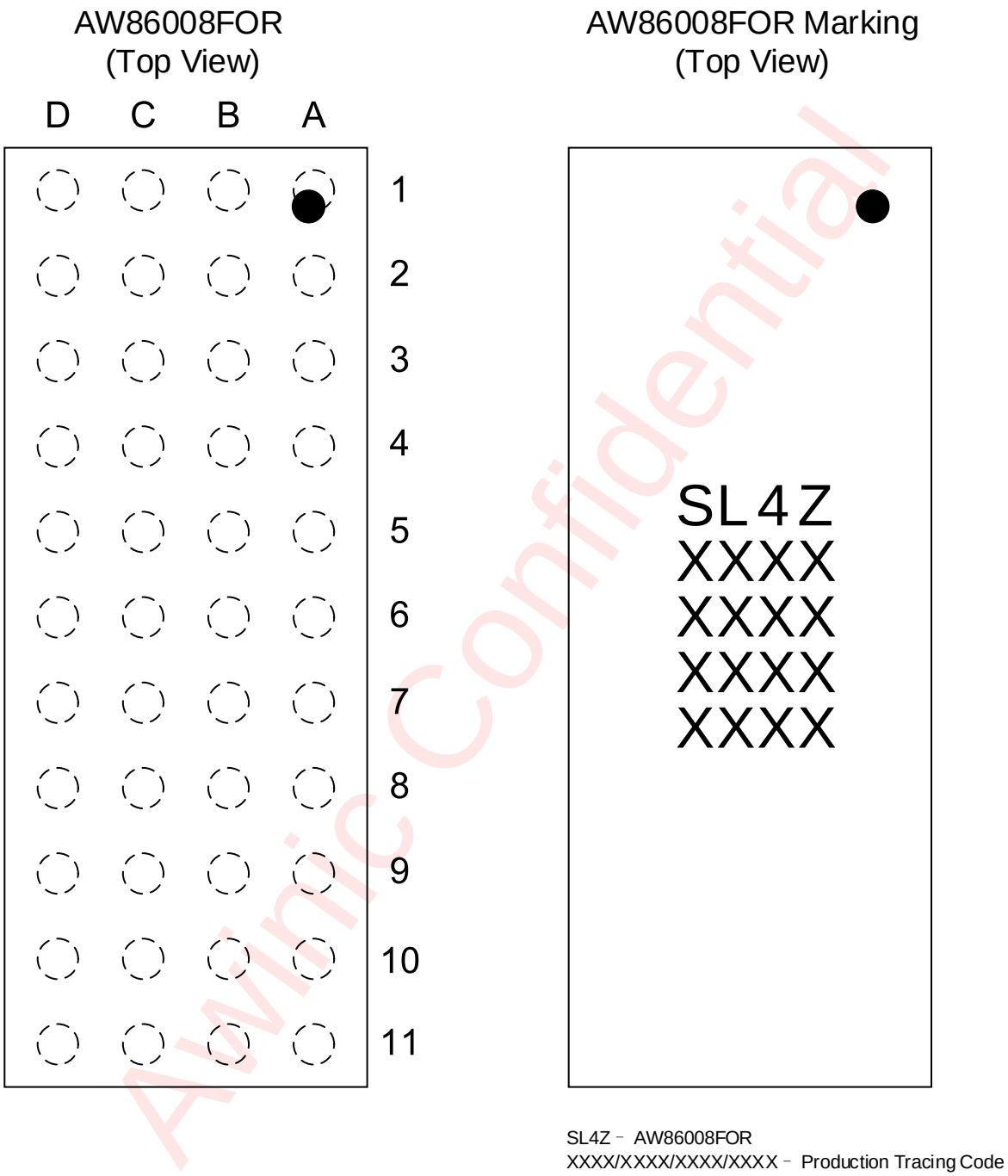
AW86008 is an Optical Image Stabilization (OIS) controller. AW86008 integrates an on-chip 32-bit CPU as controller. 128KB flash and 64+16KB SRAM is provided for program and data storage.

The driver in AW86008 support linear current out.

4-ch HALL bias DAC, which can be configured to current output, provide power supply for HALL sensor. 4-ch TMR bias DAC, which can be configured to voltage output, provide power supply for TMR sensor. 8-ch PGA, which support 8-ch single-ended signal input or 4-ch differential signal input.

There are two SPI modules in AW86008, which support master / slave / monitor mode. Two I2C modules is available, which support master and slave.

Pin Configuration And Top Mark



SL4Z – AW86008FOR
XXXX/XXXX/XXXX/XXXX – Production Tracing Code

Figure 1 AW86008FOR Pin Configuration And Top Mark

Pin Definition

NO.	PIN	TYPE	Primary Function	Sub Function
A1	OUTC2	VM Driver	H Bridge Driver C output2	
A2	OUTC1	VM Driver	H Bridge Driver C output1	
A3	OUTD1	VM Driver	H Bridge Driver D output1	
A4	OUTD2	VM Driver	H Bridge Driver D output2	
A5	AVDD	Power Supply	Power supply for analog	
A6	IOVDD	Power Supply	Power supply for digital IO	
A7	VREF	Analog	ADC reference voltage	
A8	SCL1	Digital	I2C1 interface clock	I3C interface clock
A9	SSB3	Digital	SPI chip select 3	Interrupt input
A10	SCLK1	Digital	SPI1 interface clock	
A11	MOSI1	Digital	SPI1 interface data	
B1	VM1	Power Supply	Power supply for driver C D	
B2	PGND	Ground	Driver ground	
B3	VM2	Power Supply	Power supply for driver A B	
B4	NC	NC	No connection.	
B5	BIASD	Analog	BIAS output D	
B6	AVSS	Ground	Analog ground	
B7	LDPO	Power Supply	Internal LDO power output	Power supply digital logic
B8	SDA1	Digital	I2C1 interface data	I3C interface data
B9	INT	Digital	SWCLK	Interrupt input
B10	MISO1	Digital	SPI1 interface data	Dynamic voltage scaling output/NTC input
B11	SSB1	Digital	SPI chip select 1	
C1	OUTB2	VM Driver	H Bridge Driver B output2	
C2	OUTB1	VM Driver	H Bridge Driver B output1	
C3	OPINA+	Analog	Positive input of PGA A	
C4	OPINB+	Analog	Positive input of PGA B	
C5	OPINC+	Analog	Positive input of PGA C	
C6	OPIND-	Analog	Negative input of PGA D	
C7	OPIND+	Analog	Positive input of PGA D	
C8	ECLK	Digital	SWDIO	External clock input

NO.	PIN	TYPE	Primary Function	Sub Function
C9	SDA2	Digital	I2C2 interface data	
C10	MISO2	Digital	SPI2 interface data	
C11	SSB2	Digital	SPI chip select 2	
D1	OUTA2	VM Driver	H Bridge Driver A output2	
D2	OUTA1	VM Driver	H Bridge Driver A output1	
D3	OPINA-	Analog	Negative input of PGA A	
D4	OPINB-	Analog	Negative input of PGA B	
D5	OPINC-	Analog	Negative input of PGA C	
D6	BIASA	Analog	BIAS output A	
D7	BIASB	Analog	BIAS output B	
D8	BIASC	Analog	BIAS output C	
D9	SCL2	Digital	I2C2 interface clock	
D10	SCLK2	Digital	SPI2 interface clock	
D11	MOSI2	Digital	SPI2 interface data	

Functional Block Diagram

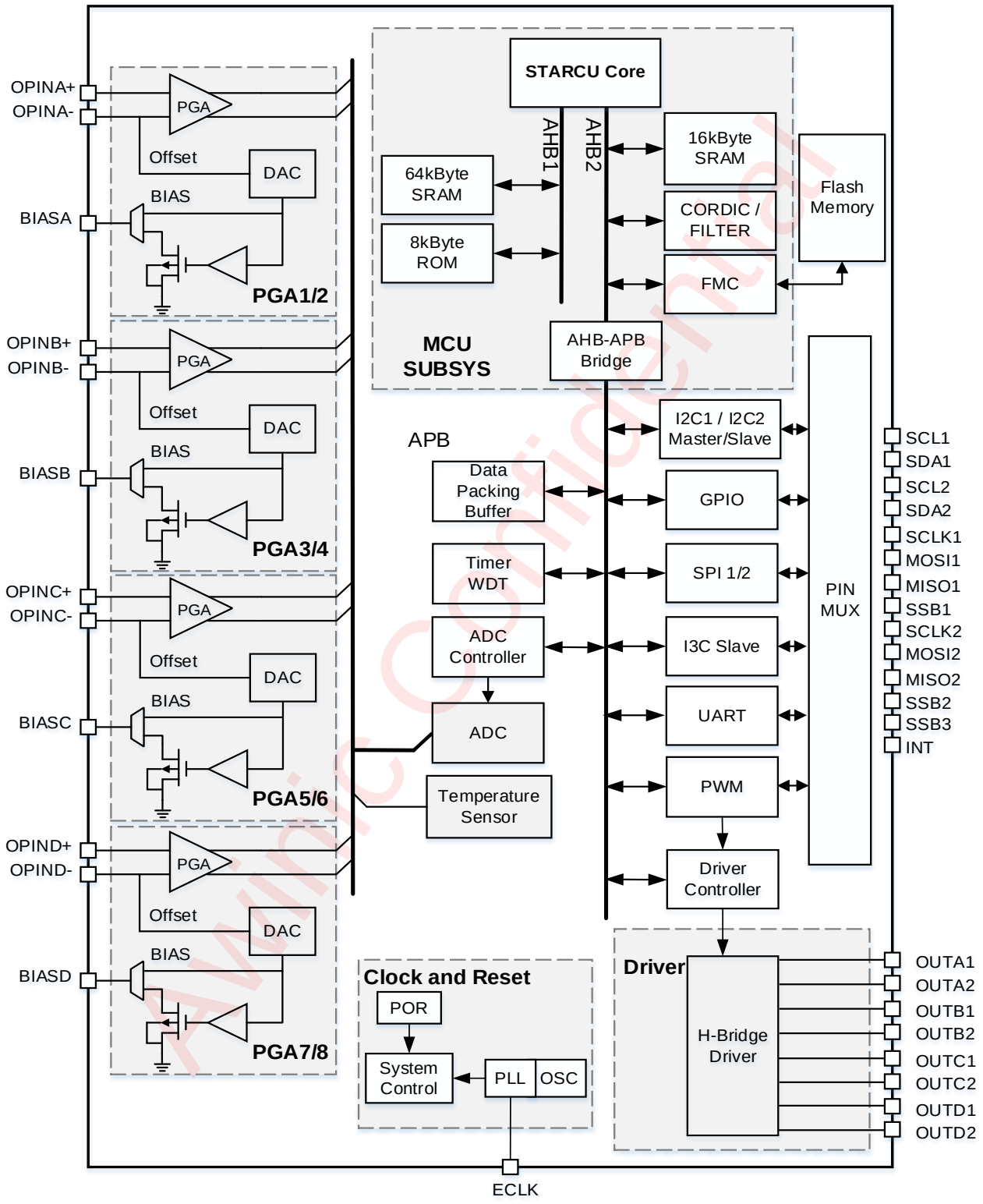


Figure 2 Functional Block Diagram

Typical Application Circuits

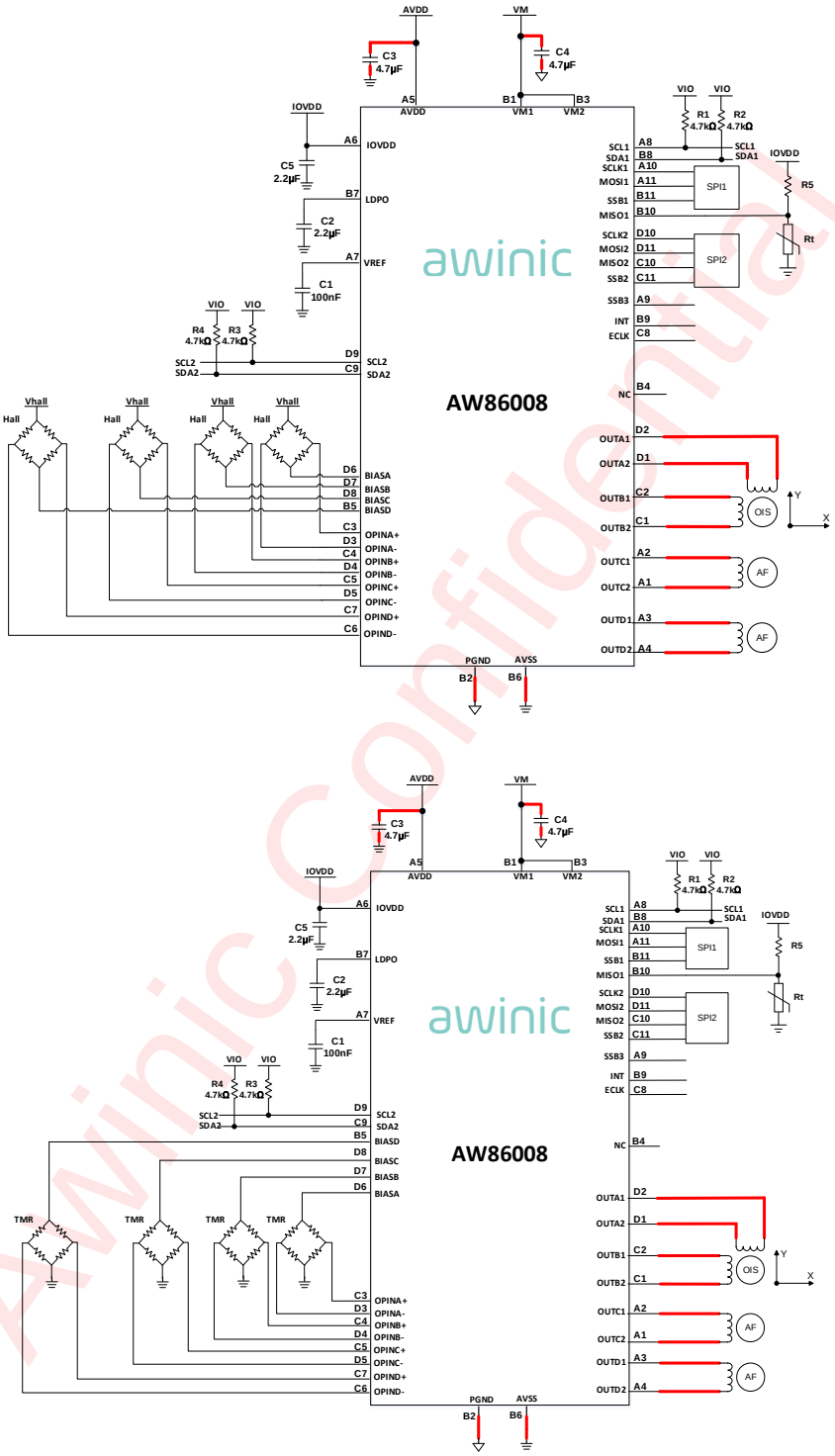


Figure 3 Typical Application Circuit of AW86008FOR

Notice for Typical Application Circuits:

1. The red line in typical application circuit mean these are large current in these lines. The max current of OUTA1, OUTA2, OUTB1, OUTB2, OUTC1, OUTC2, OUTD1, OUTD2 is 160mA. VM1 and VM2 are the power supply for drivers.

2. The ADC voltage acquisition range of MISO1(multiplexed as an NTC input pin) is 0.2V ~ IOVDD.
3. The voltage of the VM is not greater than that of the AVDD ($V_{VM} \leq V_{AVDD}$).
4. D6(BIASA),D7(BIASB),D8(BIASC),B5(BIASD) can be used as the output pin of the TMR BIAS DAC, which can output the voltage signal.
5. The B10(MISO1) pin can be used as a voltage signal output pin, and the output voltage cannot be higher than the voltage of the IOVDD.
6. If you need I2C communication speed above 400kHz, it is recommend to use 1.2kΩ resistors for R1, R2, R3, and R4.
7. It is recommended that the voltage of VIO be equal to the voltage of IOVDD.

Recommended Operating Condition

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Analog power supply voltage	V_{AVDD}	2.6	2.8	3.6	V
Input voltage range	V_{INA}	0		V_{AVDD}	V
Digital power supply voltage	V_{LDPO}	1.0	1.1	1.2	V
Driver power supply voltage	V_{VM}	1.8	2.8	3.6	V
GPIO power supply voltage	V_{IOVDD}	1.1	1.8	3.6	V
GPIO input voltage	V_{GPIO}	0		V_{IOVDD}	V

Notice: Devices working under the conditions in those ranges listed in "Recommended Operating Condition" can show the best performance. ($V_{VM} \leq V_{AVDD}$)

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW86008FOR	-40°C～85°C	FOWLP 4.4mm×1.7mm×0.3 mm -44B	SL4Z	MSL1	ROHS+HF	6000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	SYMBOL	RANGE
Power Supply Voltage	V_{AVDD}	-0.3 to 4.2V
	V_{VM}	-0.3 to 4.2V
	V_{LDPO}	-0.25 to 1.5V
	V_{VDDIO}	-0.3 to 4.2V
Input / Output voltage	V_{GPIO}	-0.3 to IOVDD+0.3V
Operating Temperature		-40 ~ 85°C
Storage Temperature		-55 ~ 125°C
ESD(Including CDM HBM)(NOTE 2)		
ALL PIN(HBM)(NOTE 2)		±2000V
ALL PIN(CDM)(NOTE 3)		±1500V
Latch-Up		
Test method: JESD78F		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2023.

NOTE3: Test method: ANSI/ESDA/JEDEC JS -002-2022.

Electrical Characteristics

AVDD=VM=3.3V, IOVDD=1.8V, AVSS=PGND=0V,environment temperature 25°C

Characteristics	Symbol	conditions	Min	Typ	Max	Unit
General Section						
UVLO						
UVLO High Level	V_{UVLOH}	AVDD ramp-up		2		V
Hysteresis	V_{HYS}			0.1		V
Operating Current						
Analog / Digital IO Supply	I_{AVDD}	System Clock = 96MHz		20		mA
Standby Current						
Chip Supply	I_{SBC}			270		μA
Analog Block						
TMR Bias DAC						
Minimum Output Voltage	V_{TB_MIN}			1.2		V
Maximum Output Voltage	V_{TB_MAX}			2.5		V
Resolution	RES_{TB}			8		Bits
Hall Bias DAC						
Minimum Output Current	I_{HB_MIN}			0		mA
Maximum Output Current	I_{HB_MAX}			4		mA
Resolution	RES_{HB}			8		Bits
Hall Gain Amplifier						
Input Gain	A_{PGA_GAIN}	Programmable	2		100	-
Hall Offset DAC						
Resolution	$RES_{HOFFDAC}$			10		Bits
Full Scale Output Voltage	$V_{HOFFDAC}$		-1.2		1.2	V
ADC						
Typical Resolution	RES_{ADCT}			12		Bits
High Resolution mode	RES_{ADCH}			16		Bits
linear current Driver						
linear current driver DAC resolution	RES_{DRV_DAC}			12		Bits
On Resistance Output	R_{DSON}			2.5		Ω
Current Compliance	I_{MAX}	Full code	150	160	170	mA
Leakage Current	I_{LKG}	Output set to Hi-Z			10	μA
Logic I/O Interface						

Characteristics	Symbol	conditions	Min	Typ	Max	Unit
SPI (SCLK1, SSB1, SSB2, SSB3,MOSI1, MISO1, SCLK2, MOSI2, MISO2)						
Low Level Input Voltage	V_{IL1}				0.36	V
High Level Input Voltage	V_{IH1}		0.84			V
Low Level Input Current	I_{IL1}	VIN = AVSS		-0.1		μA
High Level Input Current	I_{IH1}	VIN = IOVDD			1	μA
Low Level Output Voltage	V_{OL1}	Sink current = 10mA			0.2IOVDD	V
High Level Output Voltage	V_{OH1}	Source current =-2mA	0.8IOVDD			V
I2C (SCL1,SDA1, SCL2,SDA2)						
Low Level Input Voltage	V_{IL2}				0.36	V
High Level Input Voltage	V_{IH2}		0.84			V
Low Level Input Current	I_{IL2}	VIN = AVSS		-0.1		μA
High Level Input Current	I_{IH2}	VIN = IOVDD			1	μA
Low Level Output Voltage	V_{OL2}	Sink current = 2mA			0.3	V
OD IO (INT,ECLK)						
Low Level Input Voltage	V_{IL3}				0.36	V
High Level Input Voltage	V_{IH3}		0.84			V
Low Level Input Current	I_{IL3}	VIN = AVSS		-0.1		μA
High Level Input Current	I_{IH3}	VIN = IOVDD			5	μA
Low Level Output Voltage	V_{OL3}	Sink current = 2mA			0.3	V

Power Supply Timing

Following is power on and power off timing.

Parameter			Value			UNIT
No.	Symbol	Name	MIN	TYP	MAX	
1	t_{rising}	Rising time of power supply	V_{AVDD}/ $IPUR_{max}$		15	ms
2	$t_{falling}$	Falling time of power supply	0			ms
3	IPUR	Instant Power-up rate			10	mV/us
4	t_{low}	Time between power off and power on	100*			ms

Note: There should be no step during power-up, and instant IPUR does not exceed 10mV/us.

** The t_{low} is to make sure the power supply below 100mV after power off.*

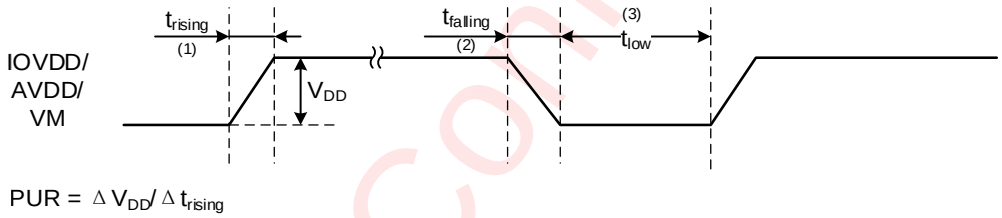


Figure 4 Power on timing and power off timing

I2C Timing Feature

Parameter			Fast mode			Fast mode plus			UNIT
No.	Symbol	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.3			μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.6			0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	Time between start and stop condition	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	0			0			ns

NOTE: This timing feature is tested on the basis of the system clock frequency of 48MHz.

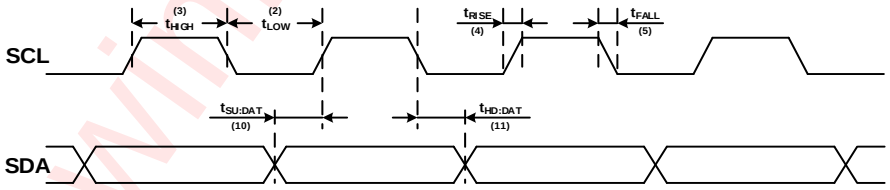


Figure 5 SCL and SDA timing relationships in the data transmission process

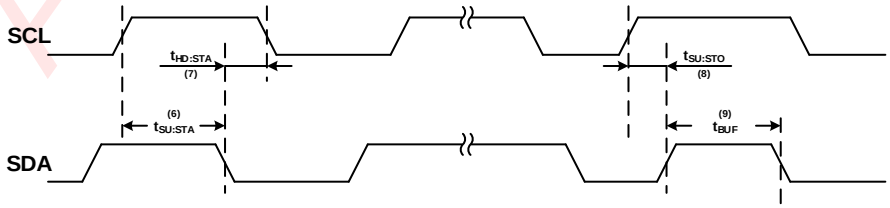


Figure 6 The timing relationship between START and STOP state

SPI Timing Feature(for slave)

Parameter			Fast mode			UNIT
No.	Sym	Name	MIN	TYP	MAX	
1	f_{SCK1}	SCLK Clock frequency(Receive only mode)			8	MHz
2	f_{SCK2}	SCLK Clock frequency(Receive and Transmit mode)			4	MHz
3	t_{DS}	MOSI data setup time	10			ns
4	t_{DH}	MOSI data hold time	60			ns
5	t_{DO}	Time of SCLK falling edge to MISO data update			60	ns
6	t_{CSH}	Time of SSB rising edge to the last edge of SCLK	50			ns
7	t_{CS2}	Time of SSB being high between 2 transmissions	120			ns
8	t_{CSS}	Time of SSB falling edge to the first edge of SCLK	210			ns
9	t_{CH}	SCLK high level Duration	40			ns
10	t_{CL}	SCLK low level Duration	40			ns

NOTE: This timing feature is tested on the basis of the system clock frequency of 48MHz.

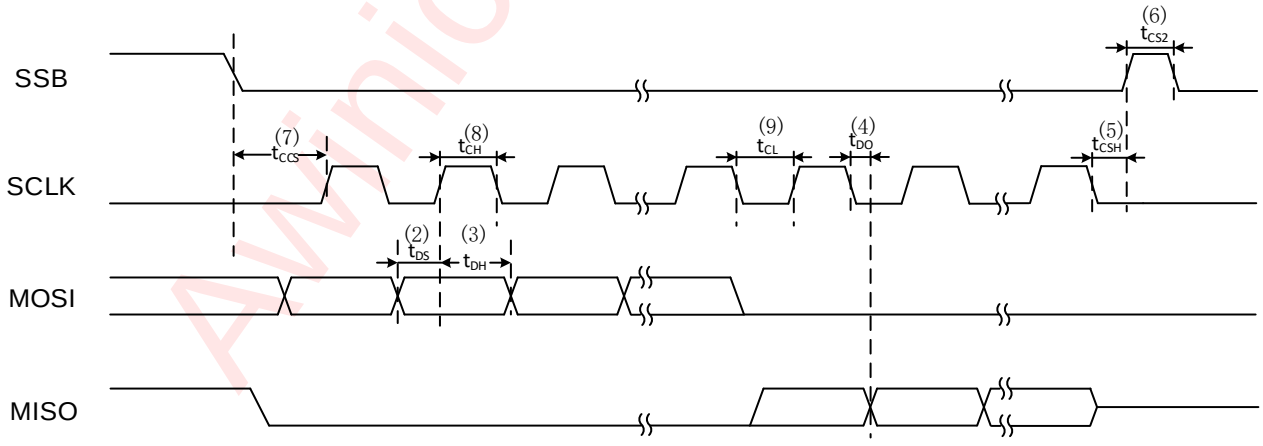


Figure 7 SPI timing diagram

SPI Timing Feature(for master)

Parameter			Fast mode			UNIT
No.	Sym	Name	MIN	TYP	MAX	
1	f_{SCK}	SCLK Clock frequency			8	MHz
2	t_{DS}	MISO data setup time	10			ns
3	t_{DH}	MISO data hold time	60			ns
4	t_{DO}	Time of SCLK falling edge to MISO data update		5		ns
5	t_{CSS}	Time of SSB falling edge to the first edge of SCLK		210		ns
6	t_{CSH}	Time of SSB rising edge to the last edge of SCLK		140		ns
7	t_{CH}	SCLK High level Duration	70			ns
8	t_{CL}	SCLK Low level Duration	70			ns

NOTE: This timing feature is tested on the basis of the system clock frequency of 48MHz.

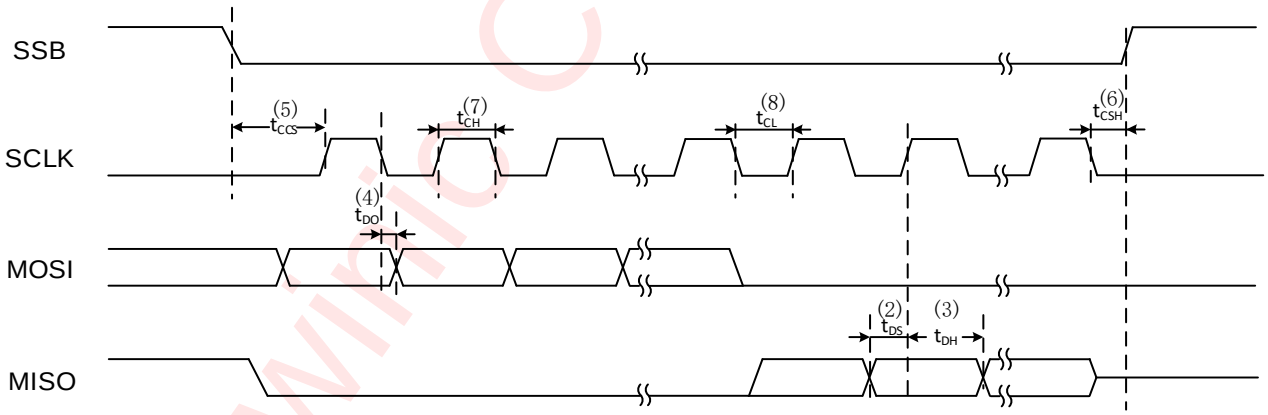


Figure 8 SPI timing diagram

Detailed Functional Description

AW86008 is a OIS controller and driver, for OIS application. A sigma-delta ADC with variable precision and sample rate is available for HALL or TMR sensor sampling. The AW86008 provide 4-ch 12-bit H-Bridge drivers with 160mA maximum drive current. For stronger computing power, we choose a Cortex-STARCU, a CPU with ARMv8 architecture which can provide 1.5DMIPS computing power pre MHz, to be chip's control unit. Independent oscillator and PLL provide a stable clock , which make this system could work at the frequency 96MHz.

WORK MODE

This chip has 4 working stages after powered on: Power-On, Boot, Operate and Standby. In Power-On stage, the chip is hold in reset status until some necessary initialization done automatically in background. After Power-On stage, by default, the chip would enter Boot stage for ISP firmware upgrading purpose.

If there is already an application program located in Flash and user doesn't issue any transmission(through I2C or SPI), Awinic Boot Loader would jump to and run that application program after 6ms. However, if no firmware upgrading is required and user wish to enter Operate stage as soon as possible, it is always able to skip the Boot stage by sending a special command to boot loader by either I2C or SPI. For more information about Awinic boot loader and ISP(In-System-Programmable) firmware upgrading, please refer to "Awinic boot loader Spec V1.0".).

The AW86008 has 2 power status: operating mode(active mode) and standby mode.

In operating mode: The MCU core and enabled peripheral work normal.

In standby mode: The OSC is disable, all analog module is off.

Application program would run in Operate stage to achieve most functions provided by the chip.

If you want to reduce the power consumption of the chip when it is idle, the chip can switch from operating mode to standby mode.

If we want AW86008 to go from operating mode to standby mode, we need to follow the following steps to operate:

- Firmware close all the analog modules.
- Close the OSC and BIAS via asynchronous I2C.

If we want AW86008 to go from standby mode to operating mode, we need to follow the following steps to operate:

- Open BIAS and OSC via asynchronous I2C.
- Reset the AW86008 via asynchronous I2C.

SYSTEM CONTROL

This chip has internal oscillator and PLL to produce clock for the whole system. And the system control module can manage the chip's clock and reset uniformly.

CLOCK

This system's clock is from oscillator, ECLK or PLL. The system clock is named SYS_CLK. HCLK is generated by SYS_CLK, and the mostly modules are in the HCLK domain, like CPU, AHB peripherals. There are several modules using other clock. The APB peripherals work in PCLK domain. The watch dog module are always in the OSC_CLK(the oscillator clock) domain.

OSC_CLK is 48MHz. If OSC_CLK does not meet the application requirements, you can use PLL as the clock source for the system's clock. The clock source of PLL is ECLK. The clock of the ECLK is input by the external

crystal oscillator via the ECLK pin. The PLL can increase the clock frequency of ECLK by 10 times, 12 times, 14 times or 16 times. The frequency of the external crystal oscillator is recommended to be 12MHz,16MHz, or 19.2MHz. The recommended clock output frequency of the PLL is 192MHz.

RESET

In this system, modules' reset are under control, they are related to the system register and the power on order of the whole chip. The system registers have control over mostly modules' reset. And the watch dog, UVLO(when enable), reset requesting from CPU, chip error status can also affect.

There are several steps between the chip powering on and beginning to work. One of these steps is check if CPU is working as expect. In mostly case, the reason which can cause the system error is wrong configuration, so it has to be set that the register which indicate CPU is work well(SYS_IMOKR) after system configuration when programming.

STARCU CORE

The main controller of this system is a 32-bit CPU, Cortex-STARCU.

FLASH MEMORY

There is a 128KByte flash memory on chip. This memory is used for storing the application program and user data. To access the flash memory, there are two ways. CPU can read data from flash memory directly through AHB bus, but cannot write. Another way is indirect access through the ISP controller module. The ISP controller module can execute the operation include write, read and erase. One write or read operation can operate up to 16 words(1 word = 4 bytes). There are two types of erasing operation: block erasing and chip erasing. One block erasing operation can erase 4KBytes data and one chip erasing operation can erase the whole 128Kbytes memory. It is illegal that write data to an area that there is data already without erasing.

BOOT ROM

There is a 8Kbytes ROM which contains the boot loader function on chip. This ROM's address is remapped to the address zero by default which mean that CPU will always boot from there after reset. In boot loader program, there are several function include initial configuration, ISP, control program jump and pause. To learn more about the protocol of boot loader, please read "Awinic Boot Loader Spec V1.0".

SPI INTERFACE

There are two SPI interface which support 3/4 wire master/slave/monitor mode. The speed of interface is up to 6MHz when PCLK is equal to 96MHz. There are four possible combinations for the serial clock phase and polarity. It is a full-duplex serial protocol when set to 4 wire mode.

MASTER

When SPI is working as a master, there are 3 CS output can select. The MISO can also be used as CS but it is feasible only in 3 wire mode. Because of having 3 CS, this master can connect up to 3 slaves and if an AW86008 is one of them this master can even set it to be a monitor or a slave through just changing the level on CS line.

This SPI support 4 transfer modes: transmit & receive mode, transmit only mode, receive only mode and EEPROM read mode. The transmit &receive mode is a full duplex transferring, there will always be a valid data is received after every frame transmit done. In the transmit(receive) only mode the receive(transmit) function will be disabled. The EEPROM read mode is just familiar to the protocol when reading a EEPROM

chip, there is no data to be received when transmitting data and no data to be transmitted when receiving data. The EEPROM read mode is unavailable possible when in salver(monitor) mode.

There are two FIFOs in SPI module, which are the basic of transferring. Data should be send to the TX FIFO when transmitting data and received data could be read from RX FIFO. How many frames the transferring will hold is determined by amount of data in TX FIFO in transmit & receive mode and transmit only mode. In the EEPROM read modes, after all the data in TX FIFO is transmitted, the number of data frames to be continuously received is determined by registers CTRL1.

SLAVE&MONITOR

When programming the SPI slave(monitor), the base address is just different from the SPI master's. The register IS_MST determines this SPI is a master or not, and is this SPI a slave or a monitor just depend on external CS input. When it is set to slave mode, it is just a standard SPI slave. When programming, it should be considered that if the time interval between two data frames is long enough for CPU processing the receive data and sending transmitted data to TX FIFO.

In OIS case, the OIS chip need to get gyro chip's data, the monitor can get the same data on SPI bus and does not affect the transferring on the bus during a SPI master is reading data from the gyro chip. For example, there are two OIS chips and only one gyro chip in the system. One OIS chip could be the SPI master and the other one could be a slave or monitor.

I2C INTERFACE

There are two I2C modules in the chip. Both I2C1 and I2C2 can be configured as master mode or slave mode. These two are both support the fast mode(1 MHz). The CPU interact with the I2C through a FIFO, CPU write data to the FIFO then I2C transmit the data out and read data from FIFO when receive data from bus. When the I2C receive a read instruction and there is no data in TX FIFO, the SCL cable will be pull down until there is valid data in FIFO. During this process, the master should wait for the SCL to become high again.

The length of deglitch can be set longer by the registers if the bus is not very stable but the speed of I2C will be affect.

ADC

There is a sigma-delta ADC whose resolution support to be configured to 12 bit, 14 bit or 16 bit. The maximum sampling rate under different resolution is 100 KSPS (12 bit), 50 KSPS (14 bit), and 25 KSPS (16 bit) respectively.

Channels

The ADC support sampling multiple channels serially. There are at most 13 channels in a sequence of sampling. These channels are divided into two groups, regular group and inject group. The channel in inject group can interrupt the conversion of channel in regular group. In other words, the channel in inject group have higher priority than the channel in regular group. If a conversion of regular group is interrupt by inject group, the conversion will restart after the conversion of inject group finish.

Trigger mode

The ADC start work when the trigger signal arise. There are two trigger mode for ADC, software mode, and timer mode. The trigger mode of inject group and regular group can be configured individually. In software mode, the trigger signal is generated when the trigger register is written. The inject group and regular group have different trigger register in software mode. In timer mode, the ADC will be triggered when the counter of

timer1 overflow.

Conversion mode

The ADC supports three conversion mode, single cycle mode, single channel mode, and continuous mode. In single cycle mode, the ADC start work after trigger and stop when all enabled channels finish converting. The channels convert analog signal in order of channel number. In single channel mode, the ADC perform conversion of only one channel after trigger. When next trigger arrive, the next enabled channel will be converted. In continuous mode, the ADC will convert all enabled channels and restart at first enabled channel when the last enabled channel finish conversion. Note that the ADC start when trigger arise, and stop when the mode register change to other mode.

Oversampling

To improve the precision of ADC, the oversampling method can be applied. The oversampling rate can be configured to 2, 4, and 8. And each channel can be configured with different oversampling rate individually. When the oversampling method is enabled, the sampling time of a channel will be multiplied by oversampling rate. The average of multiple sampling result from oversampling method is calculated by hardware and stored in ADC data register. The extreme removal method is available for noise reduction. When extreme removal enabled, the oversampling rate is added by 2. In addition, the maximum and minimum of sampling result will be discarded.

Interrupt

The ADC notify the CPU of conversion completion by interrupt. The interrupt of ADC is generated from two sub interrupt, RGL_AD_INT, IJT_AD_INT. The RGL_AD_INT interrupt is triggered after all regular channel conversions are completed. If the conversion method of the rule channel is single mode, it needs to be triggered multiple times until all rule channel conversions are completed. It will generate RGL_AD_INT interrupt. The IJT_AD_INT interrupt is generated when all injection channel conversions are completed.

Sensor bias

The sensor bias circuit provide the current or voltage for the demand of HALL sensor or TMR sensor. There are 4 channels which can be configured to be current source or voltage source individually. Four 8 bit DAC for each channel adjust the current or voltage of bias circuit output.

PGA

There are 8 PGAs for amplifying the input voltage. The 8 PGAs can work in two modes, single-ended signal and differential signal input mode. There are only 4 PGAs working in differential signal input mode. Each PGA amplify the voltage difference between two analog input pin. In single-ended signal input mode, one end of the PGA is connected to the analog input pin, while the other end is connected to $V_{BIAS}/2$. A offset voltage is added in the input of each PGA, which is adjusted by a DAC. For the better usage of voltage range of PGA and ADC, appropriate adjustment should be applied to make the output of PGA reaching the half of AVDD with zero input.

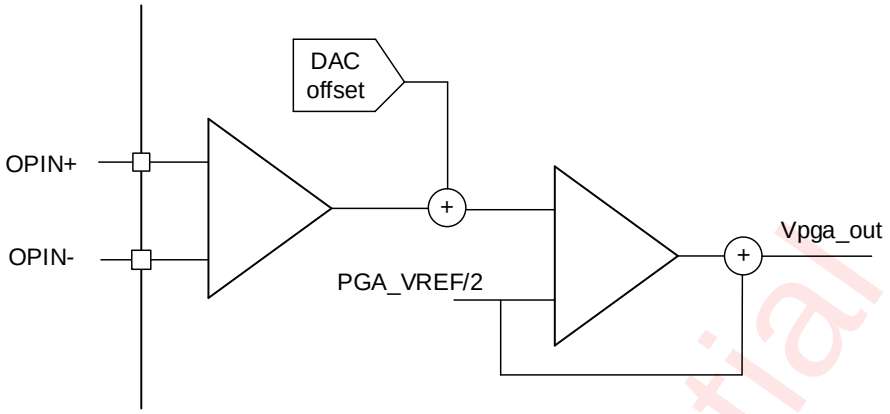


Figure 9 Differential signal input mode

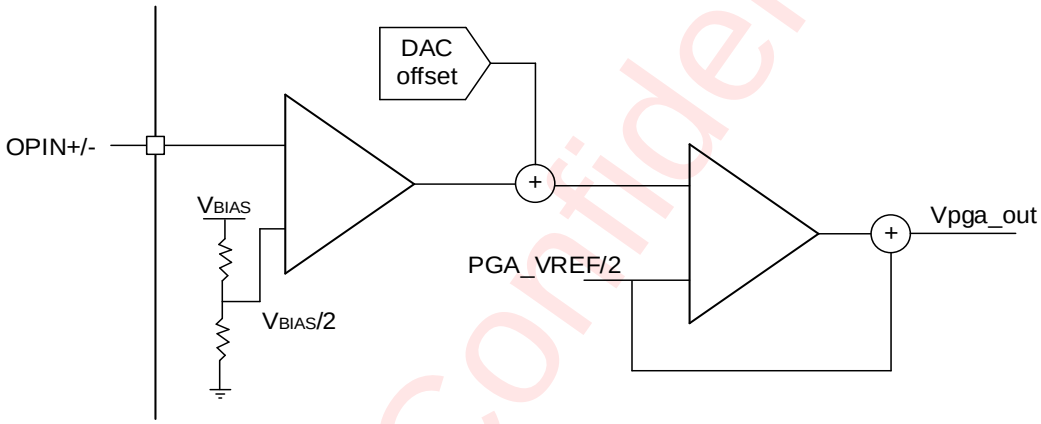


Figure 10 Single-ended signal input mode

Driver

There are 4 drivers which generate current flowing through the voice coil motor connecting with a pair of driver output pins. The currency of driver is determined by a 12 bit DAC. The bit [11] of DAC control the direction of current and other bits control the currency. The maximum current driver can provide is 160mA. PWM driver supports 4-ch current or 4-pairs voltage modulated output.

RING BUFFER

The AW86008 provide the function of hall and gyro data collection for EIS algorithm. The hall data and gyro data will be packed periodically into the ring buffer. The time interval of data packing can be configured by register. The embedded CPU can read the data from ring buffer.

Packing mode

The packing modes supported by ring buffer are hardware packing mode and software packing mode. In hardware packing mode, the hall data come from the internal ADC and the gyro data come from SPI module. The ADC and SPI module will update hall data and gyro data automatically after their data capture. In software packing mode, the hall data come from register which is updated by CPU. Therefore, the CPU should write the packed data into register before packing. The periodic packing request will generate a interrupt for CPU. In software packing mode, the interrupt should be cleared promptly as the data is actually packed when the interrupt is cleared. But in hardware mode, this interrupt can be ignore and the data will be packed automatically.

Synchronization

For the time information when the data is packed, the hardware or software synchronization mechanism is provided. If the hardware synchronization mechanism is used, the external synchronized signal should be connected to INT or SSB3 pin. A pulse of external signal is a synchronized event. The time between synchronized event and next data packing will be recorded. The application processor can use this time to calculate the time of data packing if the synchronization time is known. In addition, the packed data will be ready for reading after the synchronized event happen. If the software synchronization is used, the synchronized event is generated when the synchronized register is written.

Packed data

These types of data can be packed into ring buffer, the ADC data of hall, the angular velocity data and acceleration data. Each type of data can be configured whether be packed individually. If there is only hall data is packed, the maximum number of data package is 40. When the number of packing data exceed 40, the oldest data will be overwritten by new data. If other type of data is packed, the maximum number of data package is 10.

The data format of packed data read from ring buffer show in Table 1. The header of data package contain the information of package count and packing time. The low 6 bit of the first byte of header is the package count. The high 2 bit of the first byte of header is OIS state, which come from a register. The second byte of header indicate the time between synchronization and the first packing after synchronization. The third and fourth byte of header is the count of synchronization.

Table 1 The data format of packed data

Data area	Meaning of data area
ois_status + pack_num	header of data package
Sync time	
Vsync cnt[15:8]	
Vsync cnt[7:0]	
ADC_DATA_X[15:8] ADC_DATA _X[7:0] ADC_DATA _Y[15:8] ADC_DATA _Y[7:0] ACC_X[15:8] ACC_X[7:0]	the first data package
ACC_Y[[15:8] ACC_Y[7:0] ACC_Z[15:8] ACC_Z[7:0] GYRO_X[15:8] GYRO_X[7:0] GYRO_Y[15:8]	

Data area	Meaning of data area
GYRO_Y[7:0] GYRO_Z[15:8] GYRO_Z[7:0]	
……	the second data package
……	……
……	the pack_num data package

TIMER

This chip contain five 32-bit timers: 4 general timers and a watch dog timer.

WATCH DOG TIMER

This timer is used for reset the CPU and peripherals when program running error. This watch dog has two work modes, immediate mode and interrupt mode. In immediate mode, the reset signal is generated immediately when a timeout of the timer in watch dog occurs. The chip will be reset when the reset signal from watch dog is asserted. Kicking the watch dog by writing key to WDT_CCR can prevent timeout. The timer will restart with initial value after kicking the watch dog. In interrupt mode, a interrupt signal is asserted after the first timeout and the reset signal is asserted after the second timeout if the interrupt signal is not clear. Clearing interrupt signal or kicking the watch dog should be done before second timeout.

GENERAL TIMER

There are four general timers can be used for periodic event generation. The timer count down from initial value and generate interrupt when reach zero. The initial value can be the maximum of timer or a user-defined value. The clock of timer can be configured to PCLK or OSC_CLK.

GPIO

There are 15 digital IO pins with several functions in the chip. All of these 15 pins can be set to general-purpose IO. When working in general-purpose IO mode, they all support output, input and interrupt detection. The output function of each pin is controlled by the bit of GPIO_OER. If the bit of GPIO_OER is ‘0’, the IO pins is in input only mode with high-z state. Otherwise, the output of IO pins is determined by the bits of GPIO_ODR. Note that SCL1, SDA1, SCL2, SDA2, INT, ECLK are open-drain pins, the pull-up resistors are needed for high level output. The input level of each IO can be queried from GPIO_IDR.

UART

There is a UART in the chip. It is full duplex asynchronous communication. The programmable data bits are 5,6,7,8 bits. It can program the Parity bit. It can achieve even parity or odd parity. It can also achieve no parity bits. It can be programmed with stop bits, achieving 1 stop bit, 1.5 stop bits, or 2 stop bits. It can support break error, frame error, parity error, and receive/send buffer overflow detection functions. It can be programmed to receive and send cache trigger levels. It can independently receive/send 16 bytes of FIFO. The timing diagram of UART is shown in Figure 11.

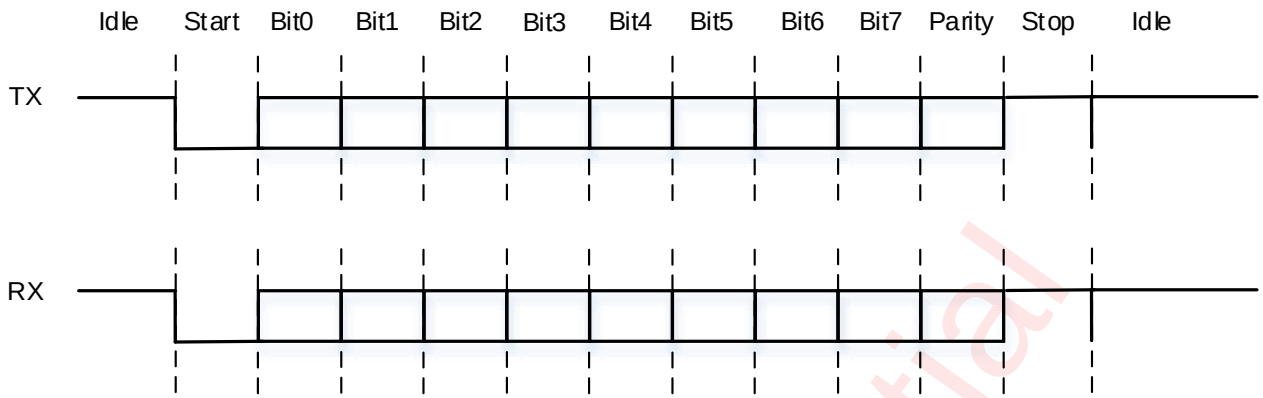


Figure 11 UART timing diagram

Hardware digital filter

There is a hardware digital filter to accelerate the signal process. The hardware digital filter support both FIR and IIR filter. The Direct-Form I structure implements of IIR filter is showed in Figure 12 and formula.

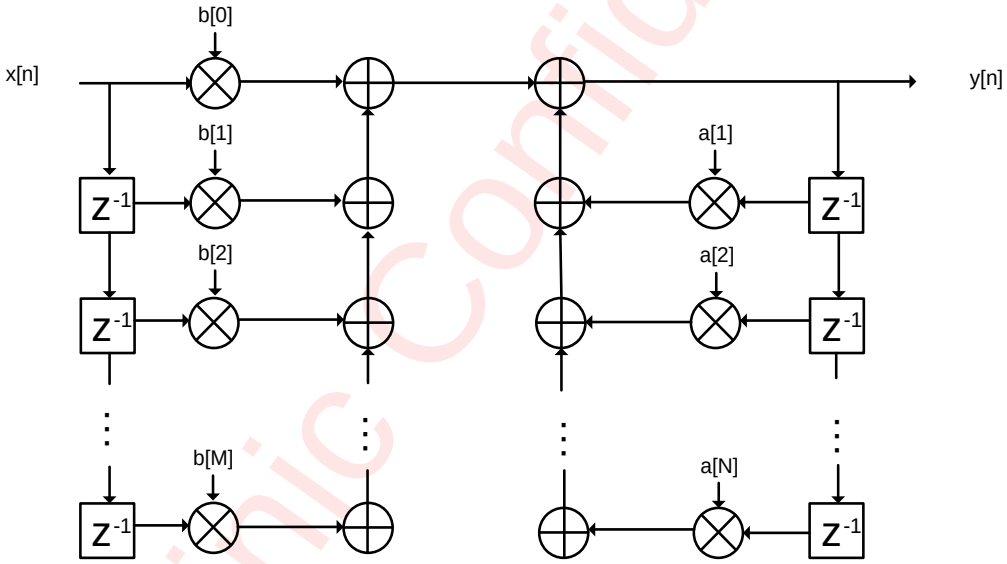


Figure 12 The Direct-Form I structure implements of IIR filter diagram

$$y[n] = \sum_{k=1}^{N} a_k y[n-k] + \sum_{k=0}^{M} b_k x[n-k]$$

The item of y[n-k] in the formula represent the poles in the transfer function of filter. And the item of x[n-k] represent the zeroes in the transfer function. The M and N represent the max order of zeroes and poles respectively. If the order of poles is equal to 0, the item of y[n-k] is not present and this filter is FIR filter. The hardware digital filter implement the Direct-Form I structure showed above. The order of poles which the hardware digital filter support is 0 to 7. The digital filter support FIR when the order of poles is configured to 0. In this case, the maximum of the order of zeros is 15. If the order of poles is configured larger than 0, the digital filter support IIR and the maximum of the order zeros is 7. The input data, calculation result, coefficients of poles and zeros is stored in register. The form of input data, output data and coefficients is 16 bit fix point number. Using the formula convert the fix point number to real number. If the number is negative, complementary number is used.

$$\text{real value} = reg\_value/2^8$$

Hardware cordic

To release the CPU from calculation of trigonometric function, a hardware cordic core is contained in our chip. There are two channels in the hardware cordic core, which support calculating in parallel.

Cordic has two calculation channels and can perform up to two calculations simultaneously. If the ch1_en (bit [30]) of CDICCR is 0, only channel 0 will be calculated. If ch1_en is 1, both channels will be calculated. Each channel has a set of input data and an output data.

The input data for channel 0 is CDICXR0, CDICYR0, CDICZR0, and the output data is CDICXOUTR0, CDICYOUTR0, and CDICZOUTR0.

The input data of channel 1 is CDICXR1, CDICYR1, CDICZR1, and the output data is CDICXOUTR1, CDICYOUTR1, and CDICZOUTR1.

The MODE0 (bit [0]) and MODE1 (bit [1]) of CDICCR respectively control the mode of one channel. If you want to calculate sin and cos, set MODE0 to 1. Taking channel 0 as an example, configure the angle (in radians) to be calculated into CDICZR0.

The form of input and output register is 32 bit fix point number. To convert the register value to real number, the formula is applied.

$$\text{real value} = reg\_value / 2^{24}$$

If the number is negative, complementary number is used.

The calculation process for sin and cos is as follows. Firstly, configure MODE0 (bit [0]) or MODE1 (bit [1]) in the CDICCR register to 1. Write the angle (in radians) to CDICZR0 or CDICZR1. Note that although CDICXR0, CDICYR0, CDICXR1, and CDICYR1 do not affect the calculation results, they cannot be set to 0. Otherwise, the calculation cannot start. Write 1 to CDICSTC to start calculation. Wait for the work_done (bit [19]) in CDICSTATUS to be 1. Obtain the calculated cos value from CDICXOUTR0 or CDICXOUTR1. Obtain the calculated sin value from CDICYOUTR0 or CDICYOUTR1.

Cordic can also be used for arctan function calculations. To calculate the arctan function, the denominator part of the tan value needs to be written to CDICXR0 or CDICXR1, and the numerator part needs to be written to CDICYR0 or CDICYR1. The calculation results are obtained from CDICZOUTR0 or CDICZOUTR1.

I3C

I3C is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCL). I3C is intended to improve upon the I2C interface, while preserving backward compatibility.

Supports I2C mode and requires static address configuration. Before I3C address allocation, static addresses are used for I2C communication, and after I3C address allocation, static addresses become invalid.

AW86008 supports the following features of I3C:

- SDR data rate up to 12.5MHz.(The system work at the frequency 96MHz.)
- Dynamic address allocation.
- Common Command Code (CCC).
- Supports configuring the size of TX and RX FIFO. (The maximum FIFO size is 16 bytes.)
- Support automatic processing of I3C address allocation.

The AW86008 always operates as an I3C slave device when communicating to the system processor, which thus acts as the I3C master. I3C master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C master.

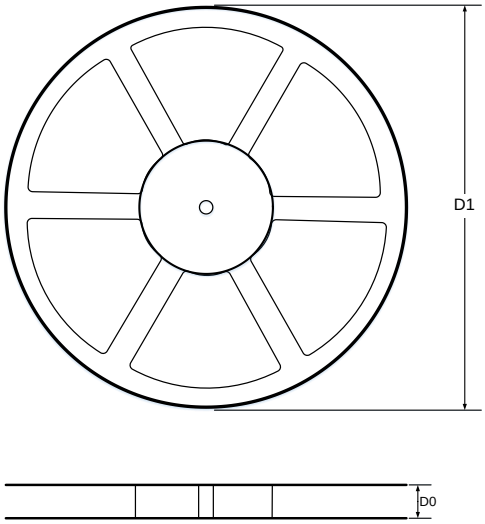
PCB Layout Consideration

AW86008 is a OIS driver chip, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

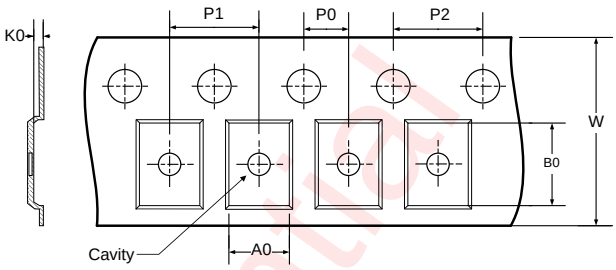
1. All peripheral components should be placed as close to the chip as possible. C1, C2, C3, C4, C5 should be close to VREF, LDPO, AVDD, VM1 / VM2, IOVDD pins respectively. Avoid to connect device and chip pins with two different layers of copper, use the same layer of copper instead. And the connection lines should be as short and wide as possible, to reduce noise and EMI interference.
2. The red line in typical application circuit mean these are large current in these lines. The max current of OUTA1, OUTA2, OUTB1, OUTB2, OUTC1, OUTC2, OUTD1, OUTD2 is 160mA. VM1 and VM2 are the power supply for drivers.
3. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient via below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.
4. The PCB wire length of SPI bus should be equal and there should be appropriate shielding for clock and data wire to avoid interference between signals.
5. The PCB wire length of I3C bus should be equal and there should be appropriate shielding for clock and data wire to avoid interference between signals.

Tape And Reel Information

REEL DIMENSIONS

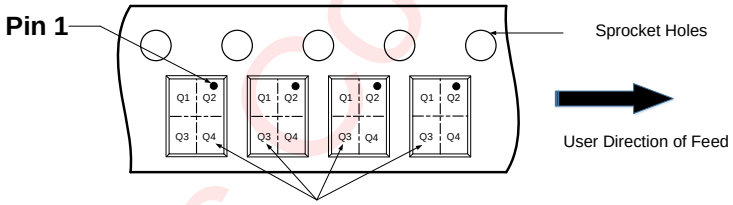


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

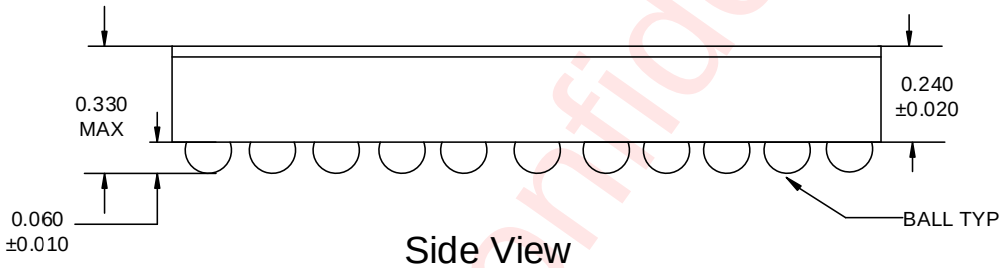
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.5	1.88	4.58	0.5	2	4	4	12	Q2

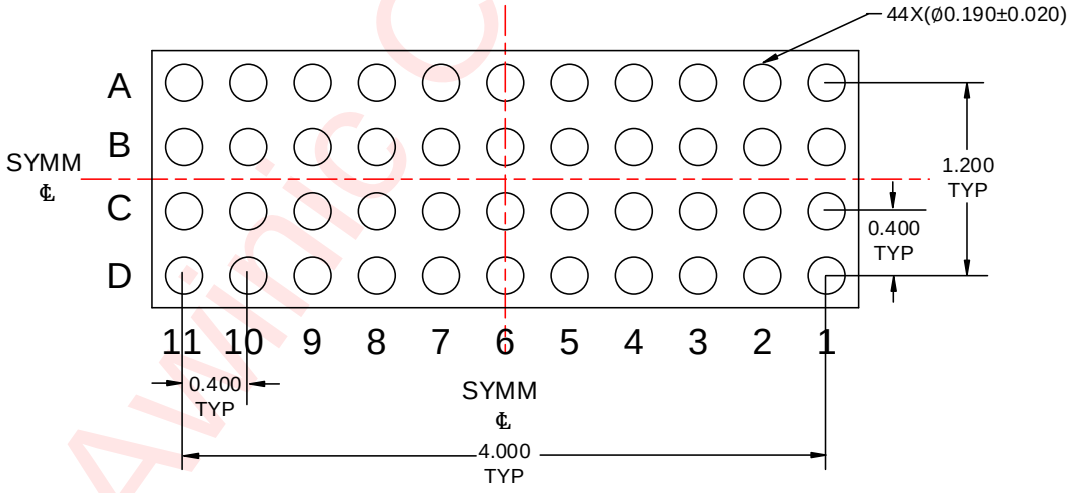
All dimensions are nominal

Package Description

Top View



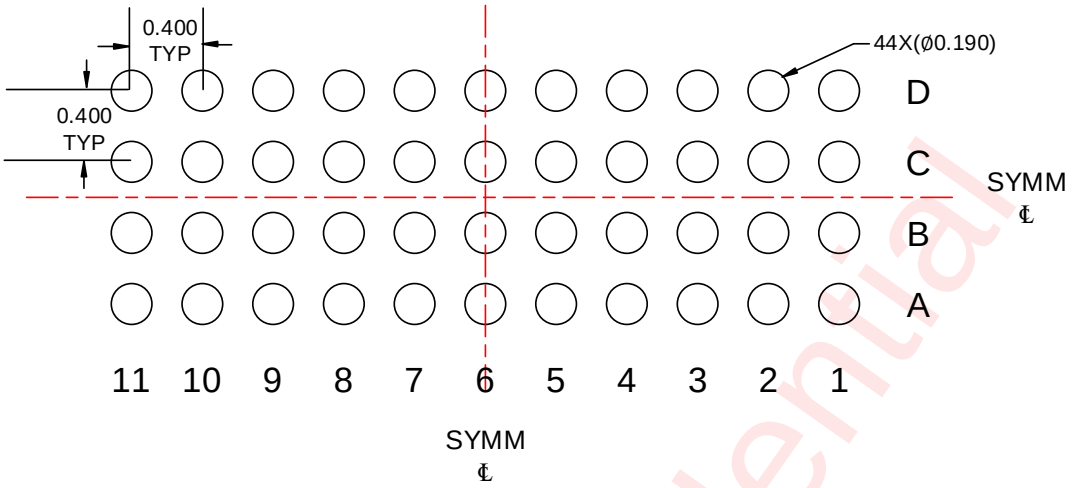
Side View

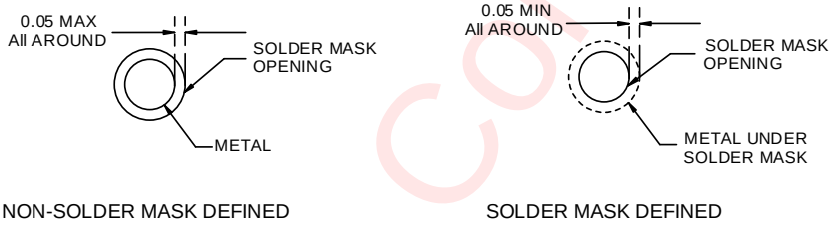


Bottom View

Unit: mm

Land Pattern Data





NON-SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Oct 2023	1. Officially released.
V1.1	Nov 2023	1. Add type to the pin definition. 2. Modify the typical application circuit figure. 3. Add notices for typical application circuits. 4. Add the description of input/output voltage to absolute maximum ratings. 5. Modify the electrical characteristic table. 6. Modify the SPI timing feature table. 7. Added the description of chip power consumption in standby mode, and the switch between active mode and standby mode. 8. Added a description of the chip's input clock function via ECLK. 9. The recommended PLL output frequency is 192MHz.
V1.2	Dec 2023	1. Modify the features.
V1.3	Mar 2024	1. Modify the description of detailed functional description.
V1.4	Mar 2024	1. Modify the description of detailed functional description. 2. Modify the description of features. 3. Modify the description of general description. 4. Modify the description of functional block diagram. 5. Modify the description of the electrical characteristics.
V1.5	Apr 2024	1. Modify the description of pin definition.

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