PA119CE • PA119CEA

Video Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- Very Fast Slew Rate — 900 V/µs
- Power MOS Technology — 4A peak rating
- Low Internal Losses — 0.75 V at 2A
- Protected Output Stage — Thermal Shutoff
- Wide Supply Range — ±15 V to ±40 V

APPLICATIONS

- Video Distribution And Amplification
- High Speed Deflection Circuits
- Power Transducers up to 5 MHz
- Modulation of Rf Power Stages
- Power LED or Laser Diode Excitation

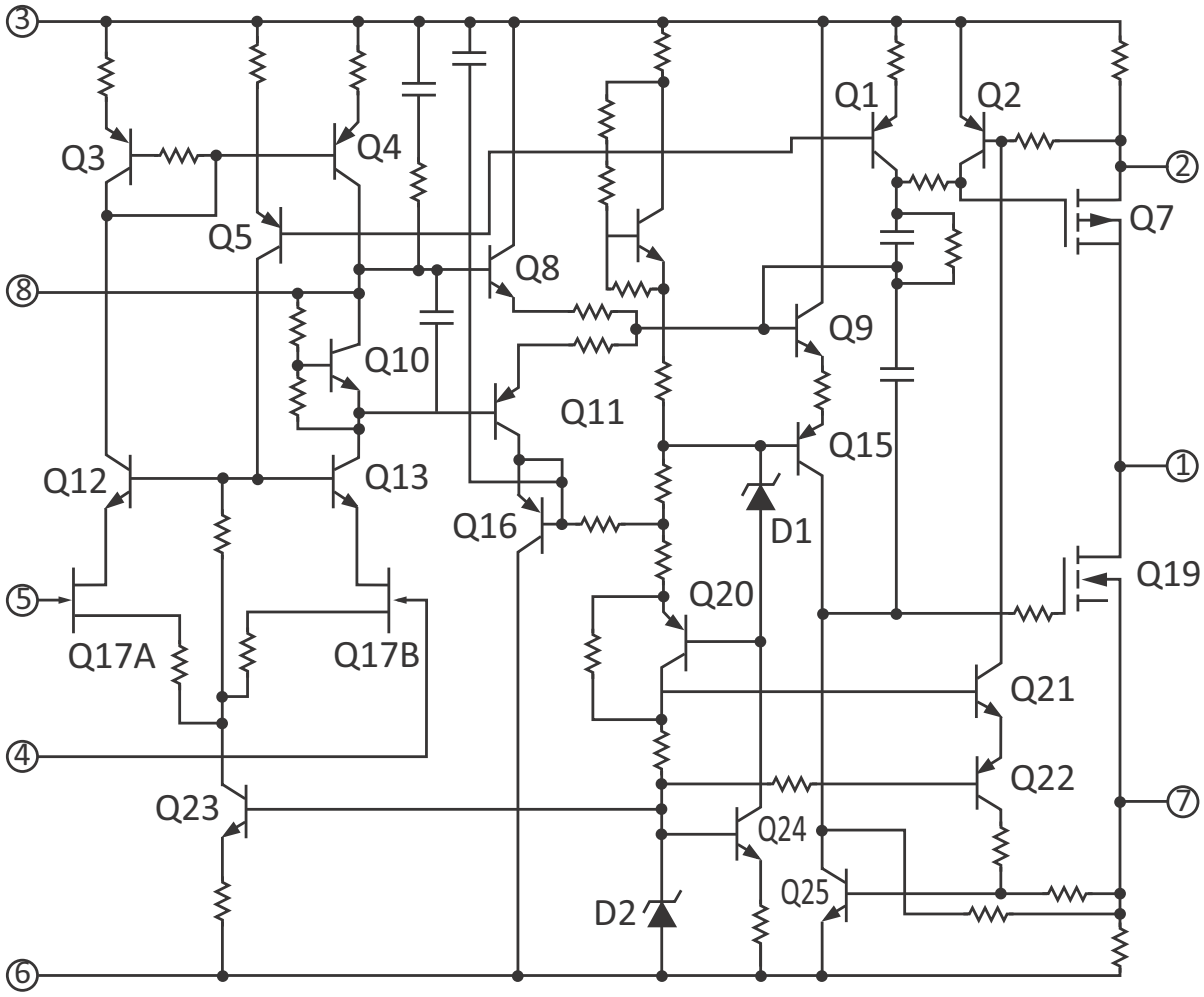
DESCRIPTION

The PA119 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascaded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA119 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary power MOS output stage. For optimum linearity, especially at low levels, the power MOS transistors are biased in a class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit of 0.5A can be increased with the addition of two external resistors. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. A heatsink of proper rating is recommended.

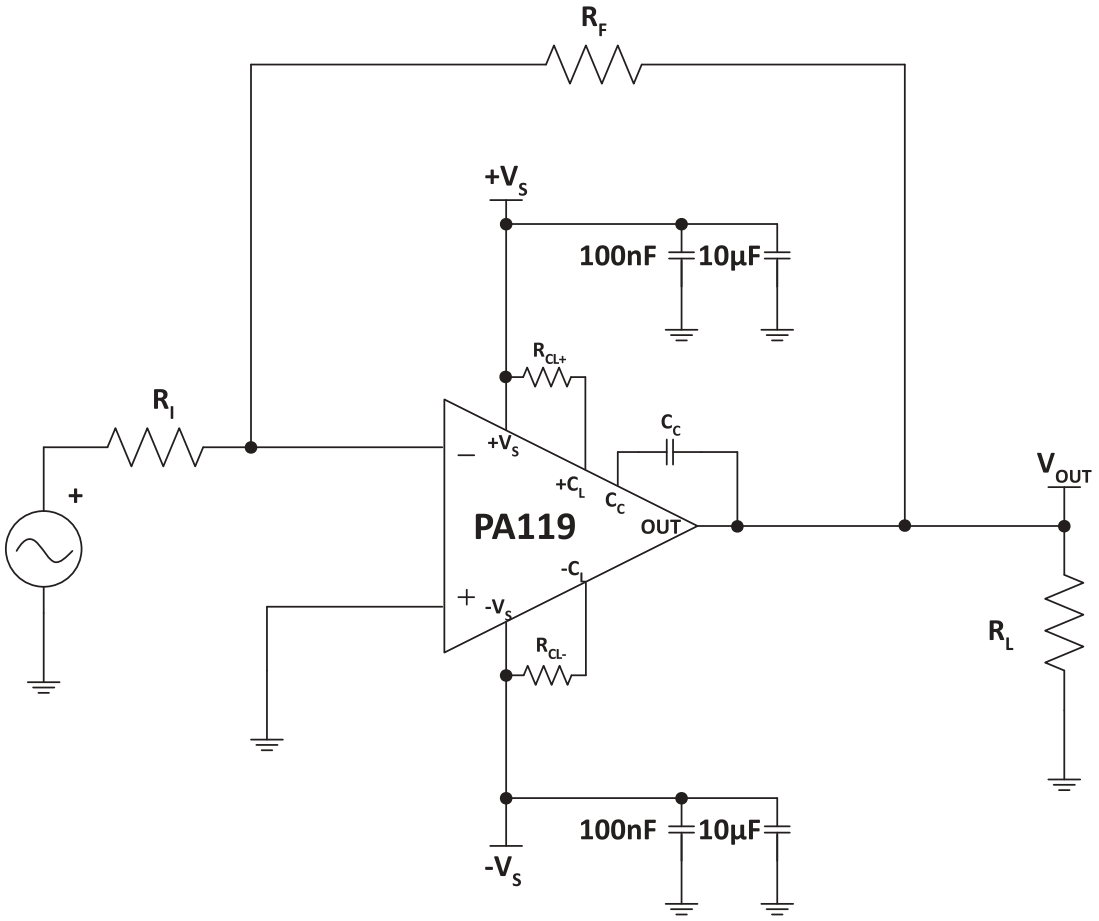
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see Application Note 1 “General Operating Considerations.”

Figure 1: Equivalent Schematic



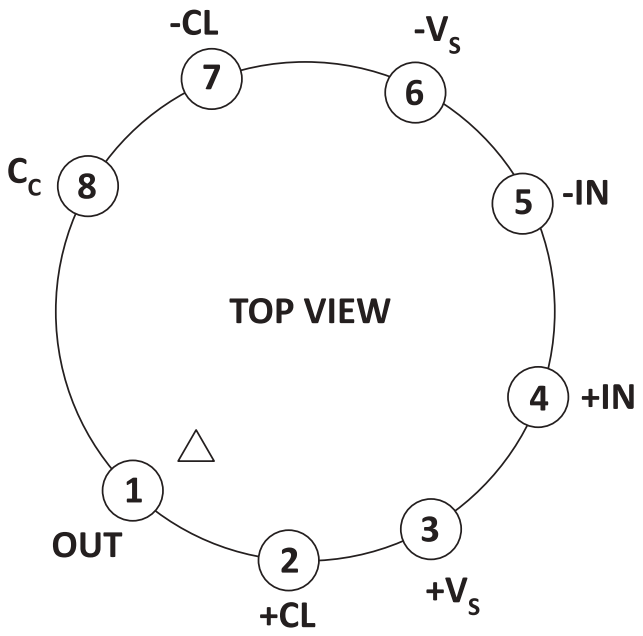
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+CL	Connect to the sourcing current limit resistor, and then the +Vs pin. Power supply current flows into this pin through R_{CL+}.
3	+Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	-CL	Connect to the sinking current limit resistor, and then the -Vs pin. Power supply current flows out of this pin through R_{CL-}.
8	CC	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, DC input specifications are ± value given. Power supply voltage is typical rating. R_C = 100, C_C = 220pF.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		80	V
Output Current, within SOA	I_O		5	A
Power Dissipation, internal	P_D		75	W
Input Voltage, differential	$V_{IN\ (Diff)}$		40	V
Input Voltage, common mode	V_{cm}	$-V_S$	$+V_S$	V
Temperature, pin solder, 10s			350	°C
Temperature, junction [1]	T_J		175	°C
Temperature, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA119			PA119A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial	T_C = 25°C		±0.5	±3		±0.35	±0.75	mV
Offset Voltage vs. temperature	T_C=25°C to 85°C		10	30		5	15	µV/°C
Offset Voltage vs. supply	T_C = 25°C		10			*		µV/V
Offset Voltage vs. power	T_C=25°C to 85°C		20			*		µV/W
Bias Current, initial	T_C = 25°C		10	200		5	50	pA
Bias Current vs. supply	T_C = 25°C		0.01			*		pA/V
Offset Current, initial	T_C = 25°C		5	100		3	25	pA
Input Impedance, DC	T_C = 25°C		10^{11}			*		Ω
Input Capacitance	T_C = 25°C		6			*		pF
Common Mode Voltage Range[1]	T_C=25°C to 85°C	$\pm V_S$–15	$\pm V_S$–12		*	*		V
Common Mode Rejection, DC	T_C=25°C to 85°C V_{CM} = ±20V	70	104		*	*		dB

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.

GAIN

Parameter	Test Conditions	PA119			PA119A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain at 10 Hz	T_C = 25°C, R_L = 1 kΩ		111			*		dB
Open Loop Gain at 10 Hz	T_C = 25°C, R_L = 15 Ω	74	88		*	*		dB
Gain Bandwidth Product @ 1 MHz	T_C = 25°C, C_C = 2.2pF		100			*		MHz
Power Bandwidth, A_V = 100	T_C = 25°C, C_C = 2.2pF		3.5			*		MHz
Power Bandwidth, A_V = 1	T_C = 25°C, C_C = 330pF		250			*		kHz

OUTPUT

Parameter	Test Conditions	PA119			PA119A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	T_C=25°C, I_O = 4A	$\pm V_S$–5	$\pm V_S$–1.5		*	*		V
Voltage Swing [1]	T_C=25°C to 85°C, I_O = 2A	$\pm V_S$–3	$\pm V_S$–.75		*	*		V
Voltage Swing [1]	T_C=25°C to 85°C, I_O = 78mA	$\pm V_S$–1	$\pm V_S$–.5		*	*		V
Settling Time to 0.1%	T_C=25°C, 2V step		0.3			*		µs
Settling Time to 0.01%	T_C=25°C, 2V step		1.2			*		µs
Slew Rate, A_V = 100	T_C = 25°C, C_C = 2.2pF	600	900		750	*		V/µs
Slew Rate, A_V = 10	T_C = 25°C, C_C = 22pF		650			*		V/µs

1. $+V_S$ and $–V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $–V_S$.

POWER SUPPLY

Parameter	Test Conditions	PA119			PA119A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	T_C=25°C to 85°C	±15	±35	±40	*	*	*	V
Current, quiescent	T_C = 25°C		100	120	*	*		mA

THERMAL

Parameter	Test Conditions	PA119			PA119A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case[1]	T_C=25°C to 85°C, F > 60 Hz		1.46	1.64		*	*	°C/W
Resistance, DC, junction to case	T_C=25°C to 85°C, F < 60 Hz		1.84	2.0		*	*	°C/W
Resistance, junction to air	T_C=25°C to 85°C		30			*		°C/W
Temperature Range, case	Meets full range specs	-25		+85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: * The specification of PA119A is identical to the specification for PA119 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

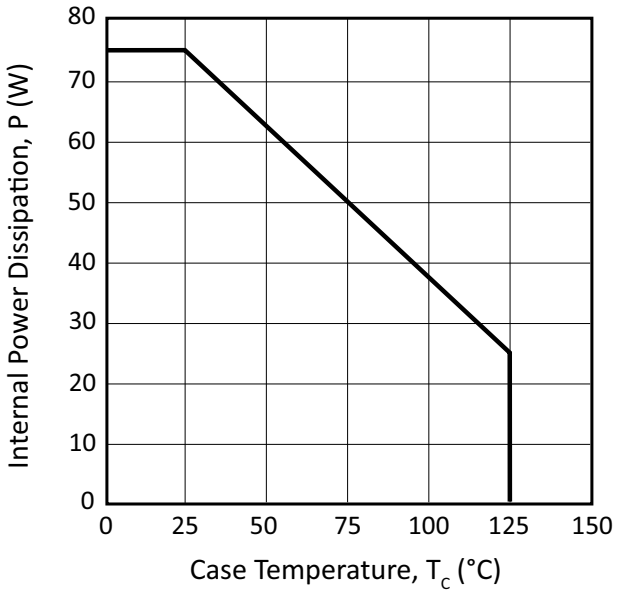


Figure 5: Current Limit

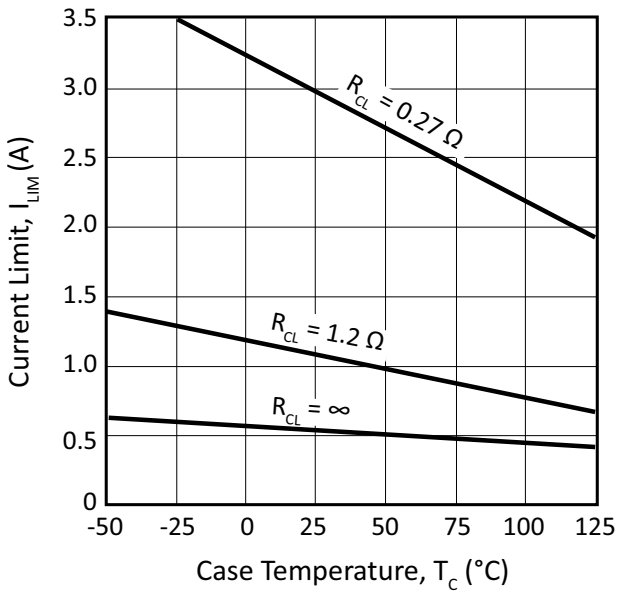


Figure 6: Quiescent Current

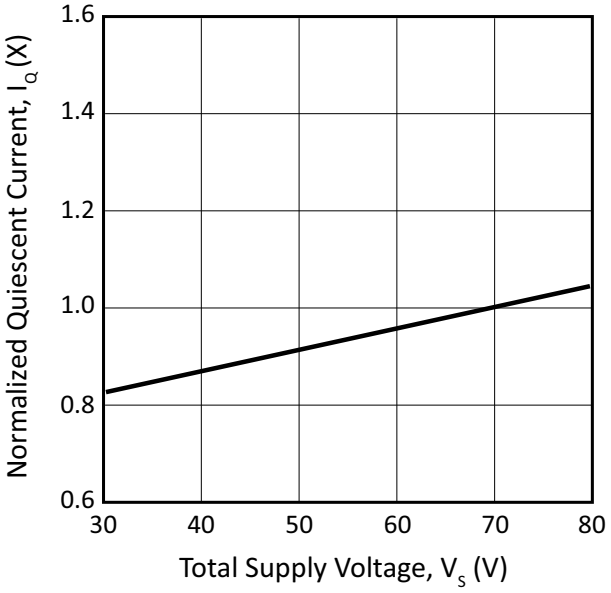


Figure 7: Small Signal Response

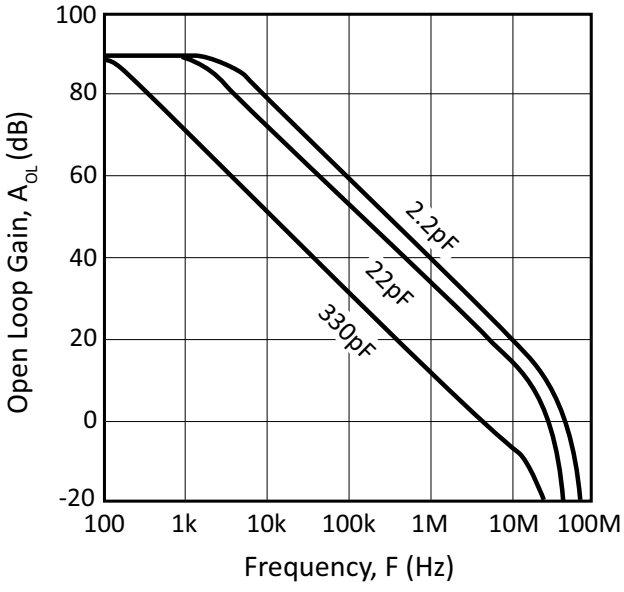


Figure 8: Output Voltage Swing

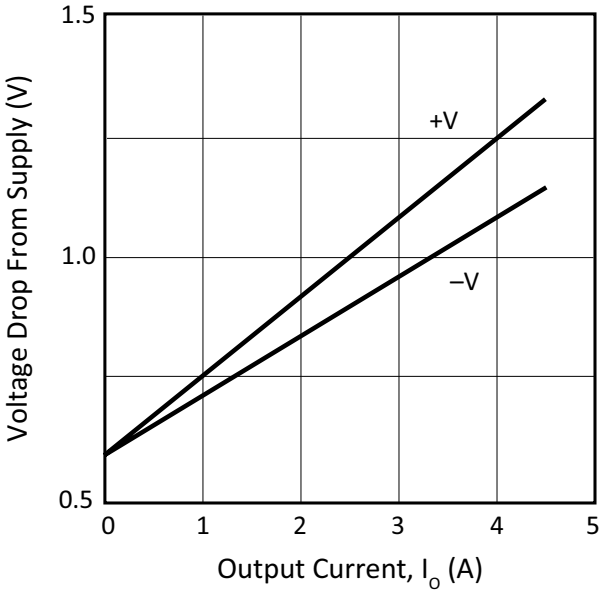


Figure 9: Power Response

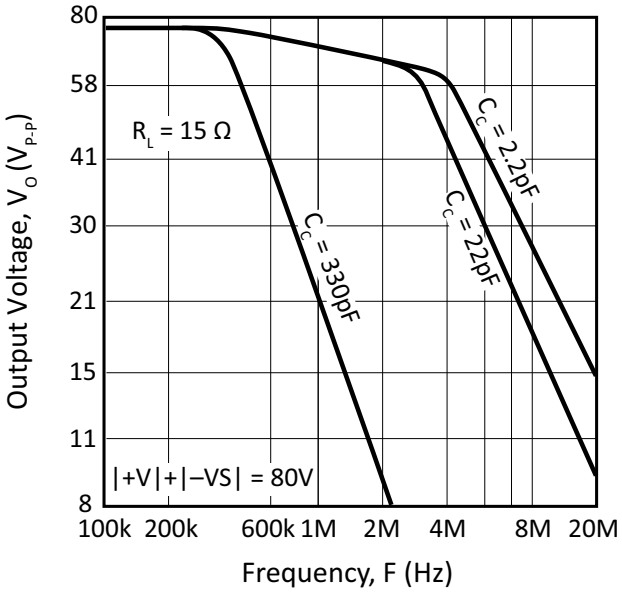


Figure 10: Slew Rate vs. Comp.

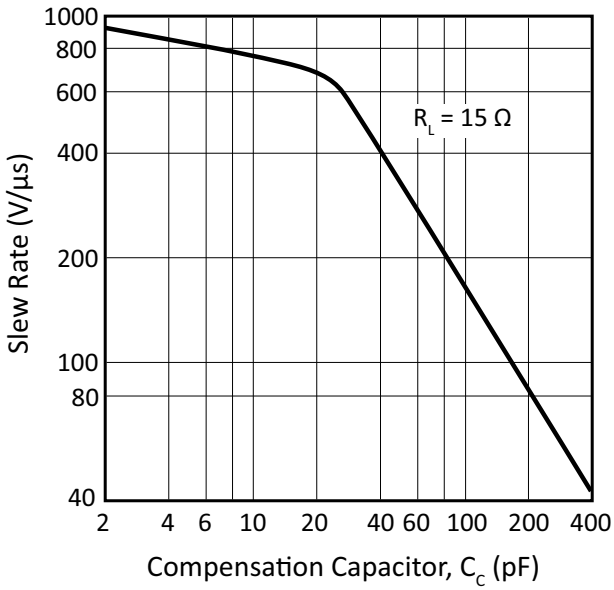


Figure 11: Pulse Response

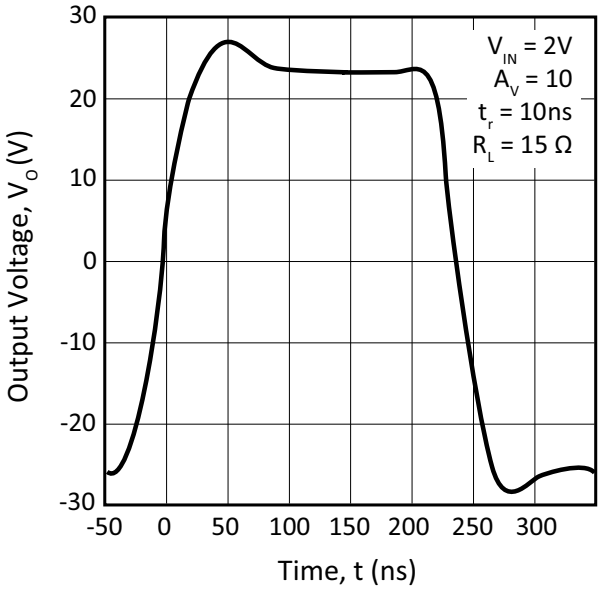


Figure 12: Input Noise

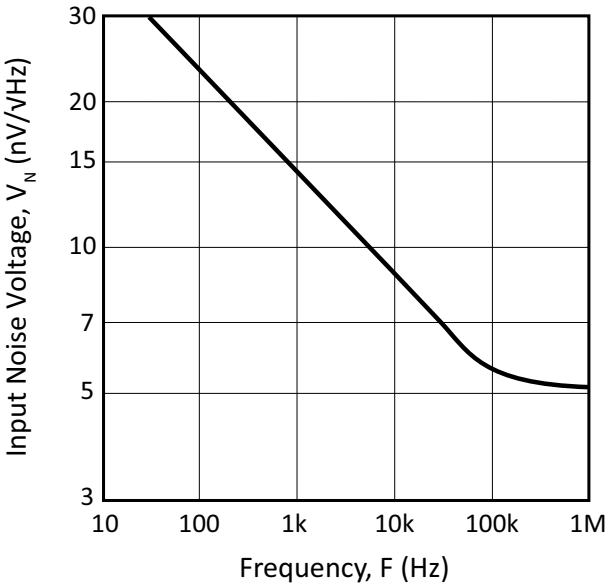


Figure 13: Common Mode Rejection

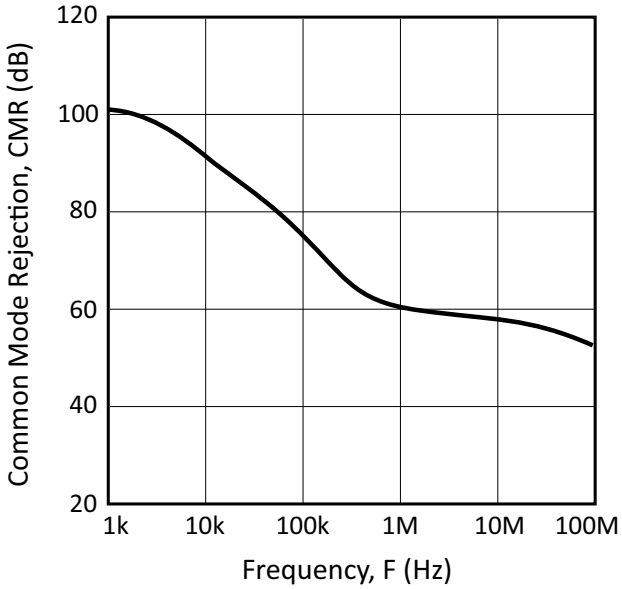


Figure 14: Power Supply Rejection

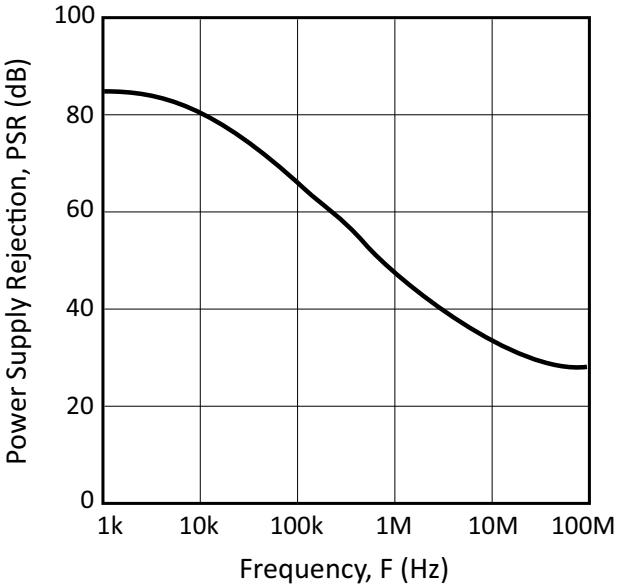
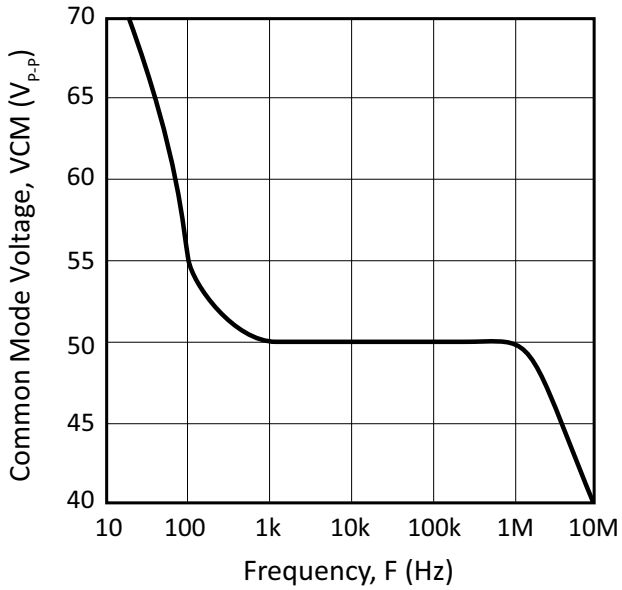


Figure 15: Common Mode Voltage

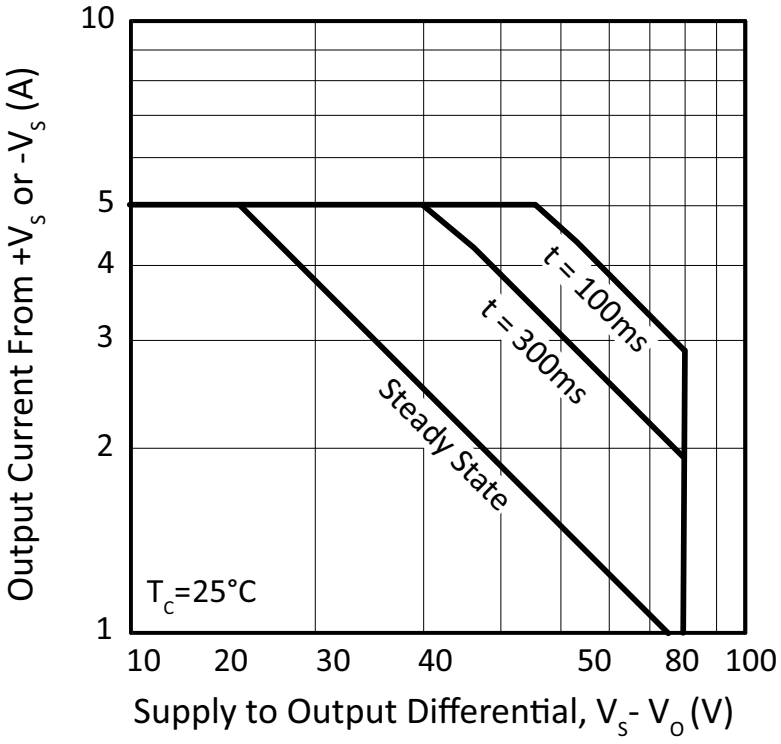


SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Figure 16: SOA



The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

±V_S	Capacitive Load	Inductive Load
40 V	0.1µF	11 mH
30 V	500µF	24 mH
20 V	2500µF	75 mH
15 V	∞	100 mH

2. Safe short circuit combinations of voltage and current are limited to a power level of 100W.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

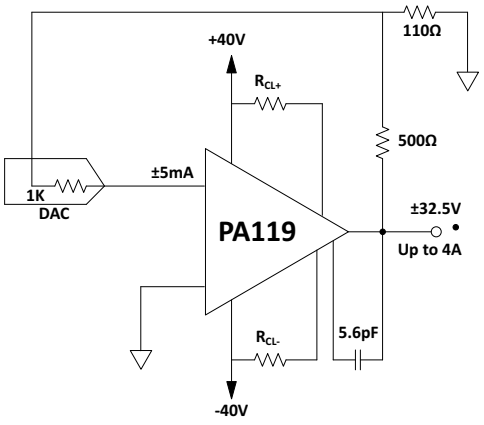
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

This fast power driver utilizes the 900V/µs slew rate of the PA119 and provides a unique interface with a current output DAC. By using the DAC’s internal 1 kΩ feedback resistor, temperature drift errors are minimized, since the temperature drift coefficients of the internal current source and the internal feedback resistor of the DAC are closely matched. Gain of V_{OUT} to I_{IN} is –6.5/ mA. The DAC’s internal 1k resistor together with the external 500 Ω and 110 Ω form a “tee network” in the feedback path around the PA119. This effective resistance equals 6.5 kΩ. Therefore the entire circuit can be modeled as 6.5 kΩ feedback resistor from output to inverting input and a 5mA current source into the inverting input of the PA119. Now we see the familiar current to voltage conversion for a DAC where $V_{OUT} = -I_{IN} \times R_{FEEDBACK}$

Figure 17: Typical Application



PA119 as a Fast Power Driver

CURRENT LIMIT

Q2 (and Q25) limit output current by turning on and removing gate drive when voltage on pin 2 (pin 7) exceeds 0.65V differential from the positive (negative) supply rail. With internal resistors equal to 1.2 Ω, current limits are approximately 0.5A with no external current limit resistors. With the addition of external resistors current limit will be:

To determine values of external current limit resistors:

$$I_{LIM}(A) = \frac{0.65V}{R_{CL}(\Omega)} + 0.54A$$

$$R_{CL}(\Omega) = \frac{0.65V}{I_{CL}(A) - 0.54A}$$

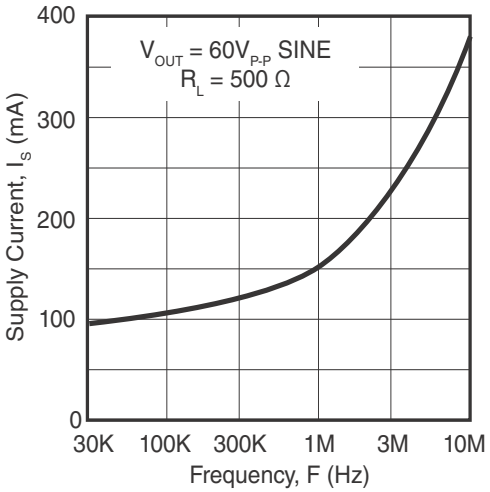
PHASE COMPENSATION

At low gain settings, an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered when determining gain settings. The capacitance values listed in the external connection diagram, along with good high frequency layout practice, will insure stability. Interpolate values for intermediate gain settings.

SUPPLY CURRENT

The PA119 features a class A/B driver stage to charge and discharge gate capacitance of Q7 and Q19. As these currents approach 0.5A, the savings of quiescent current over that of a class A driver stage is considerable. However, supply current drawn by the PA119, even with no load, varies with slew rate of the output signal as shown below.

Figure 18: Supply Current



OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductances, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows the heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the steady state boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

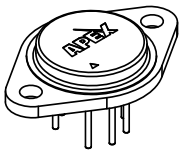
STABILITY

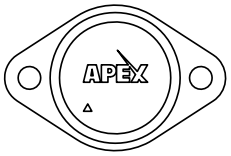
Due to its large bandwidth, the PA119 is more likely to oscillate than lower bandwidth power operational amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a larger capacitor at the expense of slew rate. Total physical length (pins of the PA119, capacitor leads plus printed circuit traces) should be limited to a maximum of 3.5 inches.
2. Keep the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500 Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or by bypassing the feedback resistor.
3. Connect the case to any AC ground potential.

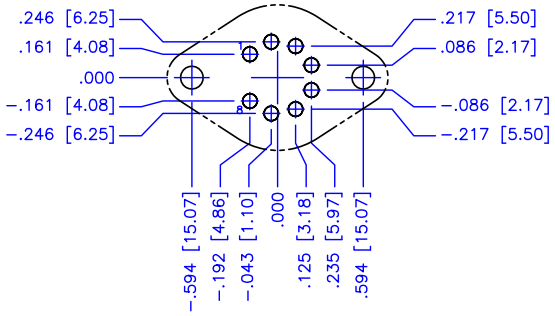
PACKAGE OPTIONS

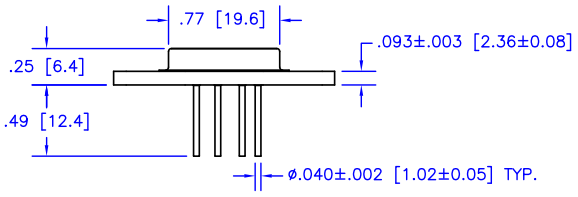
PACKAGE STYLE CE

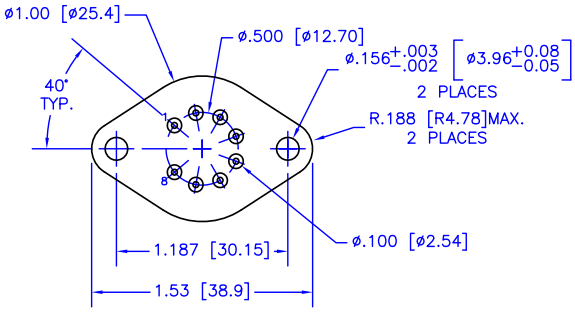




Ordinate dimensions for CAD layout







NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel−plated Alloy 52.
6. Header material: Nickel−plated cold−rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

For all Apex Microtechnology product questions and inquiries, call toll free 800-546-2739 in North America. For inquiries via email, please contact apex.support@apexanalog.com. International customers can also request support by contacting their local Apex Microtechnology Sales Representative. To find the one nearest to you, go to www.apexanalog.com