CD64

High Voltage Power Booster

RoHS COMPLIANT

FEATURES

- Wide Supply Range – ±25 V to ±75 V
- High Output Current – Up to 3.5 A Continuous
- Programmable Gain
- Separate Supplies for Amplifier Core and Output Stage
- High Slew Rate – 400 V/µs Typical
- Programmable Output Current Limit
- High Power Bandwidth – 600 kHz
- Low Quiescent Current – 10 mA per Channel
- Two Amplifier Channels, Fully Independent

APPLICATIONS

- LED Test Equipment
- LCD Test Equipment
- Semiconductor Test Equipment
- High Voltage Instrumentation
- Electrostatic Transducers and Deflection
- Piezoelectric Positioning and Actuation
- Programmable Power Supplies

DESCRIPTION

The CD64 is a dual high voltage, high current booster amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output current capability of the booster.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Junction Transistors. Although the booster can be configured quite simply, enormous flexibility is provided through the choice of driver amplifier, current limit and supply voltage.

The CD64's design is based on the PB64 and is a cost-effective alternative. The SMT construction allows for a low production cost that rivals the much more expensive hybrid option for a fraction of the price. It is built on a thermally conductive but electrically isolated substrate with a footprint of 5.69 in² (36.7 cm²) for both channels, which can be mounted to a heatsink.

TYPICAL CONNECTION

Figure 1: Typical Connection (Composite Configuration)

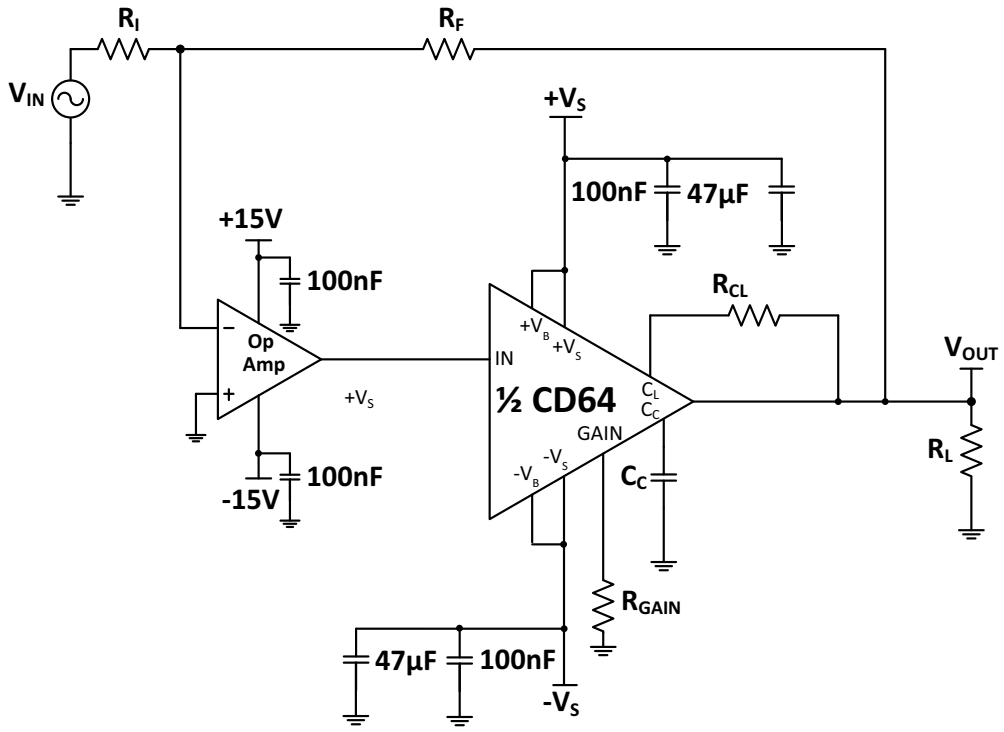
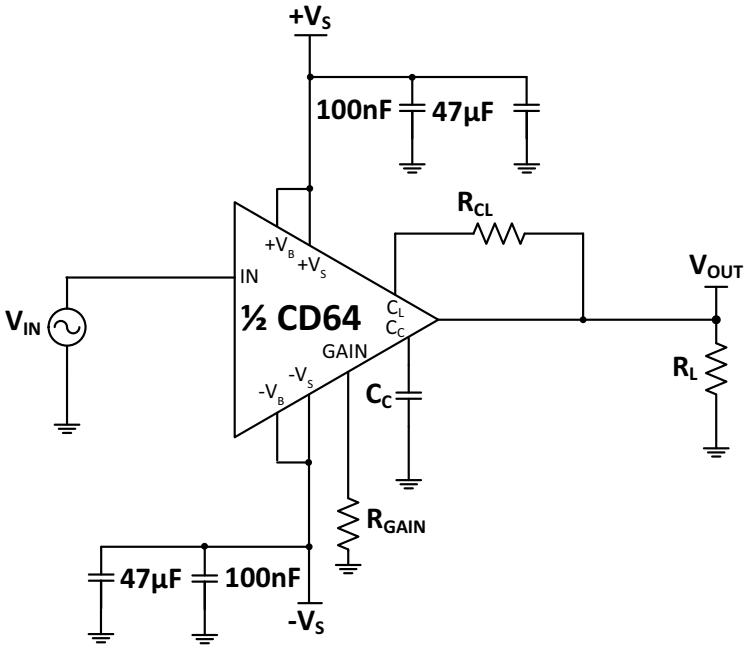
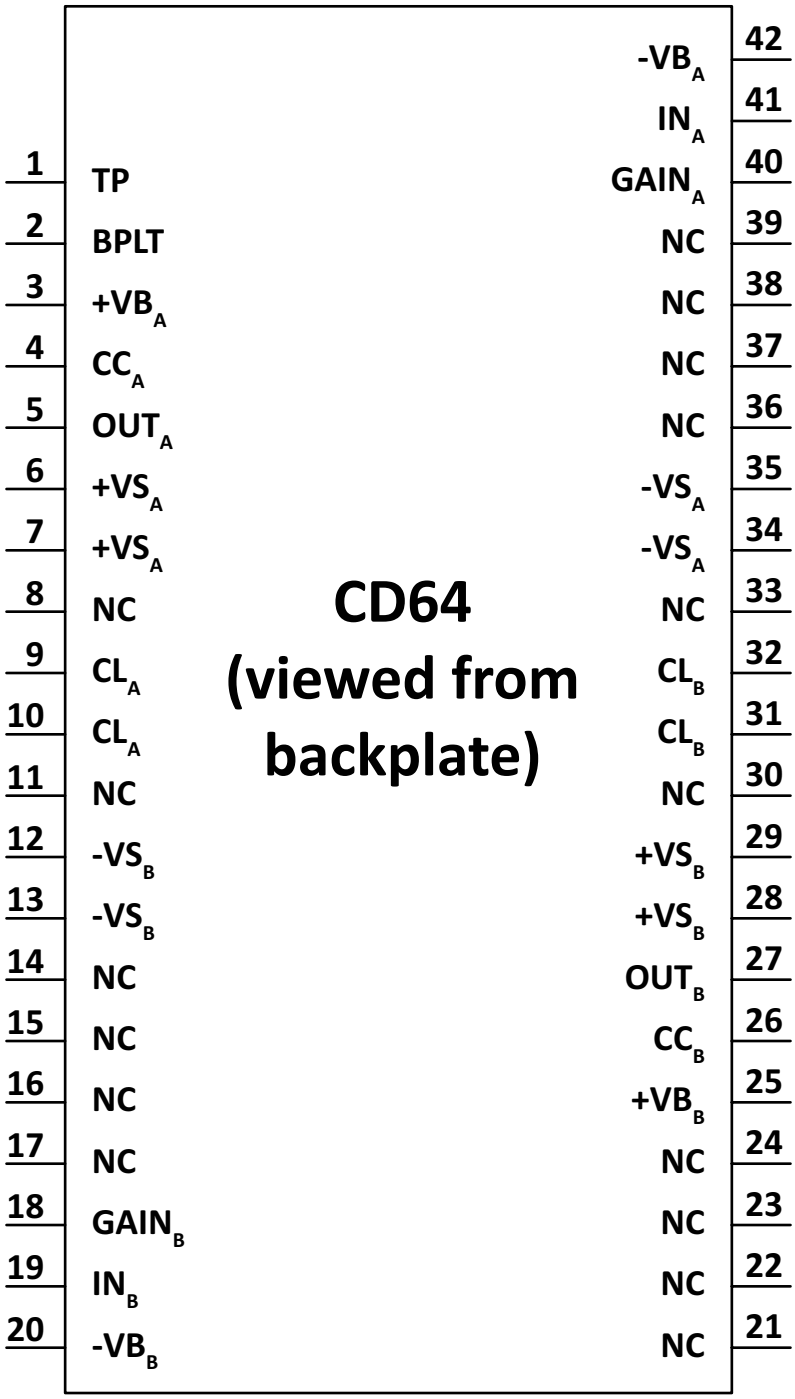


Figure 2: Typical Connection (Standalone Configuration)



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	TP	Apex test pin. Do not connect
2	BPLT	AC coupling to backplate. Connect to signal ground.
3	$+VB_A$	The positive boost supply rail for channel A. Short to $+VS_A$
4	CC_A	Compensation capacitor connection for channel A. Select value based on the desired phase compensation. See applicable section.
5	OUT_A	The output for channel A. Connect this pin to load and to the feedback resistors.
6, 7	$+VS_A$	The positive supply rail for channel A. Short to $+VB_A$
8, 11, 14, 15, 16, 17, 21, 22, 23, 24, 30, 33, 36, 37, 38, 39	NC	Not connected.
9, 10	CL_A	Connect to the current limit resistor of channel B. Output current flows into/out of these pins through $R_{CL,A}$. The output pin and the load are connected to the other side of $R_{CL,A}$.
12, 13	$-VS_B$	The negative supply rail for channel B. Short to $-VB_B$
18	$GAIN_B$	Gain resistor pin for channel B. Connect $R_{GAIN,B}$ between $GAIN_B$ and ground. This will specify the gain for the power booster itself, not the composite amplifier. See applicable section.
19	IN_B	The input for channel B.
20	$-VB_B$	The negative boost supply rail for channel B. Short to $-VS_B$
25	$+VB_B$	The positive boost supply rail for channel B. Short to $+VS_B$
26	CC_B	Compensation capacitor connection for channel B. Select value based on the desired phase compensation. See applicable section.
27	OUT_B	The output for channel B. Connect this pin to load and to the feedback resistors.
28, 29	$+VS_B$	The positive supply rail for channel B. Short to $+VB_B$
31, 32	CL_B	Connect to the current limit resistor of channel B. Output current flows into/out of these pins through $R_{CL,B}$. The output pin and the load are connected to the other side of $R_{CL,B}$.
34, 35	$-VS_A$	The negative supply rail for channel A. Short to $-VB_A$
40	$GAIN_A$	Gain resistor pin for channel A. Connect $R_{GAIN,A}$ between $GAIN_A$ and ground. This will specify the gain for the power booster itself, not the composite amplifier. See applicable section.
41	IN_A	The input for channel A.
42	$-VB_A$	The negative boost supply rail for channel A. Short to $-VS_A$

SPECIFICATIONS (PER AMPLIFIER)

All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_C = 25°C.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	+VS to -VS		200	V
Positive Supply Voltage	+VB	+VS	+VS+10	V
Negative Supply Voltage	-VB	-VS-10	-VS	V
Output Current, peak, per channel within SOA	I_O		11	A
Power Dissipation, internal DC, 1 channel			36	W
Power Dissipation, internal DC, 2 channel [1]			41	W
Input Voltage, referred to common	V_{IN}	(-VS + 10V) / A_V	(+VS - 10V) / A_V	V
Temperature, pin solder, 10s max.			260	°C
Temperature, junction [2]	T_J		150	°C
Temperature Range, storage		-55	+125	°C
Operating Temperature Range, case	T_C	-25	+85	°C

1. Rating applies when power dissipation is equal in each amplifier.
2. Long term operation at the maximum junction temperature will result in reduced product life. De-rate power dissipation to achieve high MTTF.

CAUTION The CD64 is constructed from MOSFET devices. ESD handling procedures must be observed.

INPUT (EACH CHANNEL)

Parameter	Test Conditions	CD64			CD64A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial		-20	±10	+20	*	*	*	mV
Offset Voltage vs. Temperature	Full temp range		+0.04			*		mV/°C
Input Bias Current		-50	±4	+50	-25	*	+25	µA
Input Resistance, DC			97			*		MΩ
Input Capacitance			3			*		pF
Noise	f = 10 kHz		25			*		nV/√Hz
DC Power Supply Rejection			97		*	*		dB
DC Common Mode Rejection			85		*	*		dB

GAIN (EACH CHANNEL)

Parameter	Test Conditions	CD64			CD64A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain	DC		92			*		dB
Power Bandwidth, $100V_{p-p}$	A_V = 5V/V, R_L = 50 Ω		600			*		kHz

OUTPUT (EACH CHANNEL)

Parameter	Test Conditions	CD64			CD64A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing +VS = +VB -VS = -VB	I_O = 2A	|VS| - 11.9	|VS| -7		*	*		V
	I_O = 0.5A		|VS| - 5.5			*		V
Voltage Swing +VS = +VB-15 V -VS = -VB+15 V	I_O = 2A		|VS| - 2.9			*		V
	I_O = 0.5A		|VS| - 0.6			*		V
Current, peak, continuous	Per Channel		3.5					A
Slew Rate, Resistive	R_L = 50 Ω, $10V_{P-P}$ input step, A_V = 10V/V		400			*		V/µs
Slew Rate, Capacitive	R_L = 4 Ω, C_L = 30 nF, $10V_{P-P}$ input step, A_V = 10V/V		200			*		V/µs
Capacitive Load, 25% Overshoot	$4V_{P-P}$ input step, A_V = 5V/V		10			*		nF
Settling Time to 0.1%	R_L = 50 Ω, $4V_{P-P}$ input step, A_V=5V/V		800			*		ns

POWER SUPPLY (EACH CHANNEL)

Parameter [1]	Test Conditions	CD64			CD64A			Units
		Min	Typ	Max	Min	Typ	Max	
Boost Voltage, ±VB		±25	±65	±75				V
Supply Voltage, +VS		+VB-10		+VB				V
Supply Voltage, -VS		-VB		-VB+10				V
Current, quiescent, VS supply	Each Channel		2.6					mA
Current, quiescent, VB supply	Each Channel		6.5					mA

1. +VS and −VS denote the positive and negative supply voltages.

THERMAL

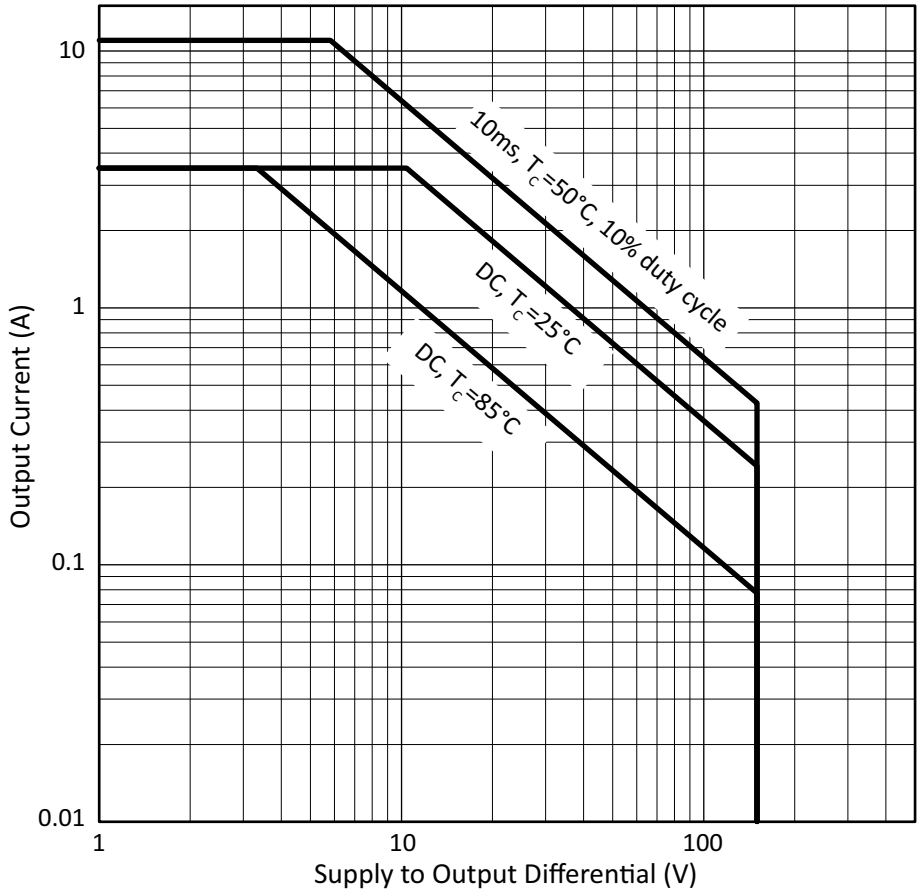
Parameter	Test Conditions	CD64			CD64A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, DC junction to case, 1 amplifier	Full temp range, f < 60 Hz		2.86	3.44		*	*	°C/W
Resistance, DC junction to case, 2 amplifier [1]	Full temp range, f < 60 Hz		2.52	3.03		*	*	°C/W
Resistance, AC junction to case, 1 amplifier [2]	Full temp range, f ≥ 60 Hz		2.29			*		°C/W
Resistance, AC junction to case, 2 amplifier [1 2]	Full temp range, f ≥ 60 Hz		1.79			*		°C/W
Resistance, junction to air	Full temp range		10.1			*		°C/W
Operating Temperature Range, case		-25	25	85				°C

1. Rating applies when power dissipation is equal in each amplifier.
2. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

SOA

The MOSFET output stage of the CD64 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast recovery diodes must be used.

Figure 4: SOA GRAPH



TYPICAL PERFORMANCE GRAPHS

Figure 5: Power De-Rating

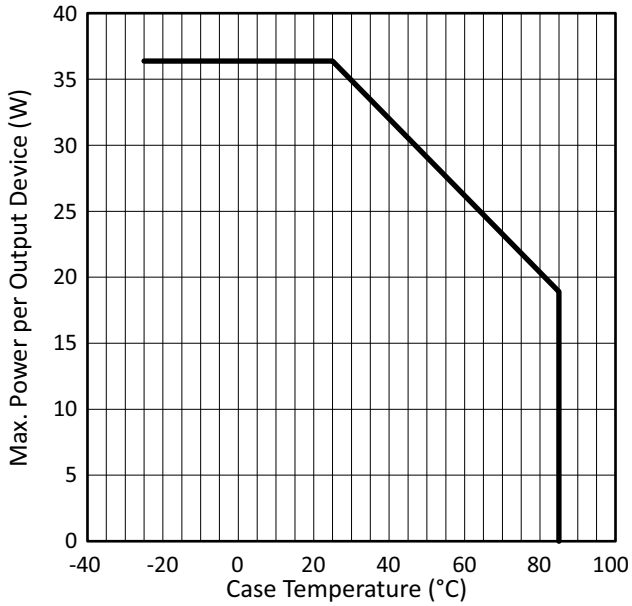


Figure 6: Pulse Response

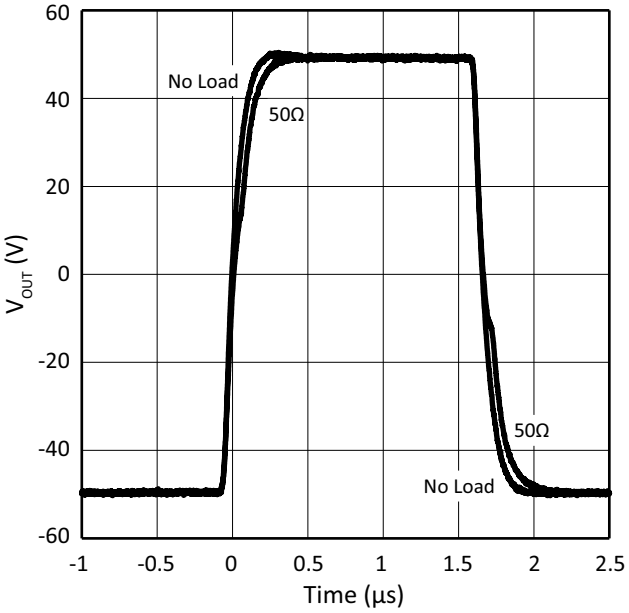


Figure 7: Output Voltage Swing

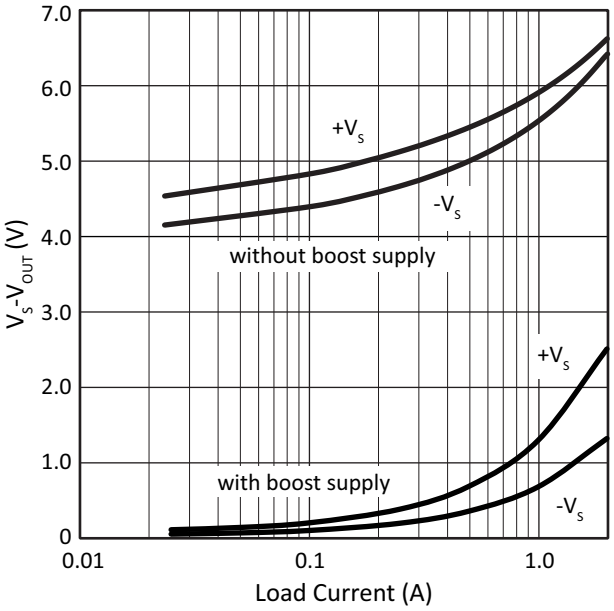


Figure 8: THD vs. Frequency

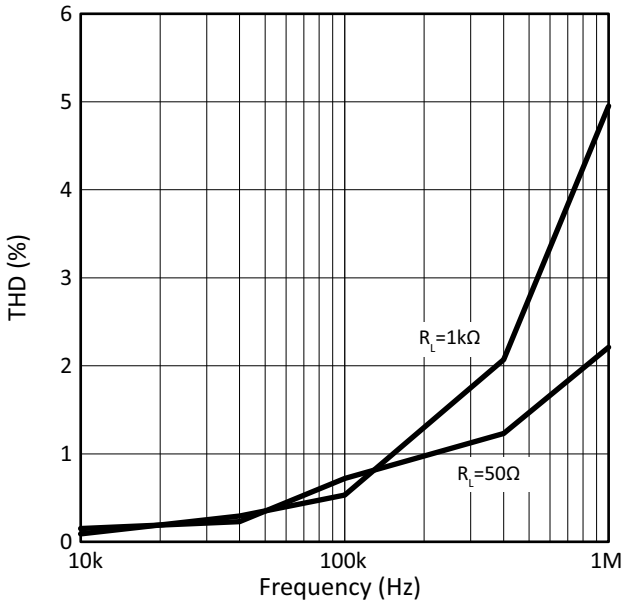


Figure 9: Small Signal Closed Loop Gain (Gain)

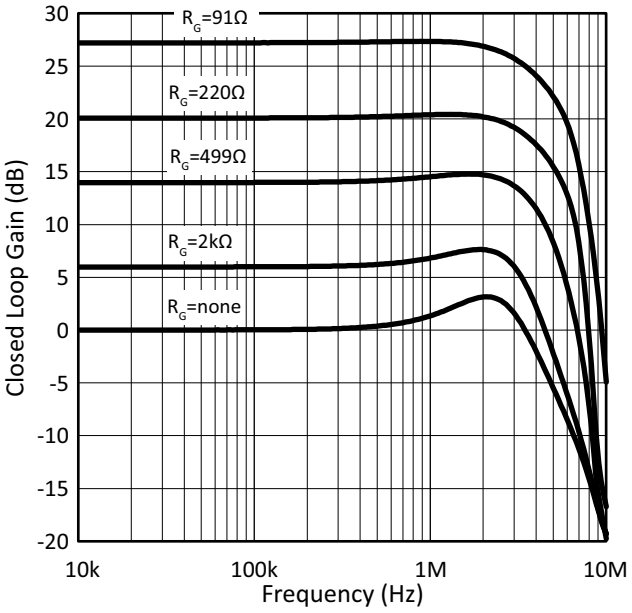


Figure 10: Small Signal Closed Loop Phase (Gain)

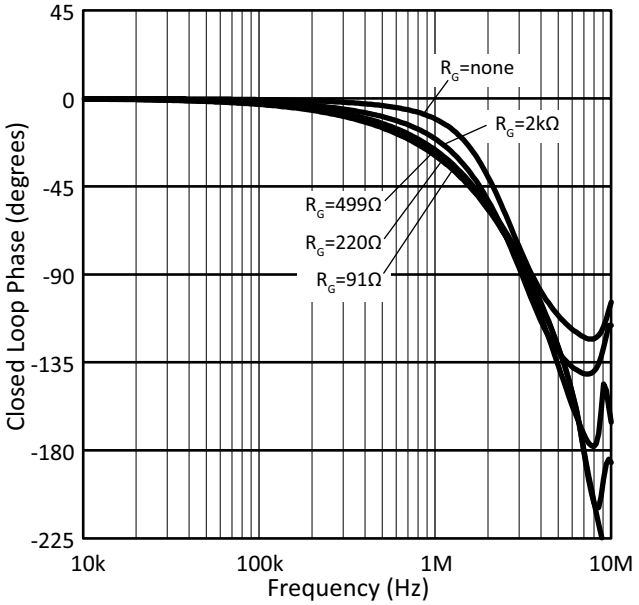


Figure 11: Small Signal Closed Loop Gain (Load)

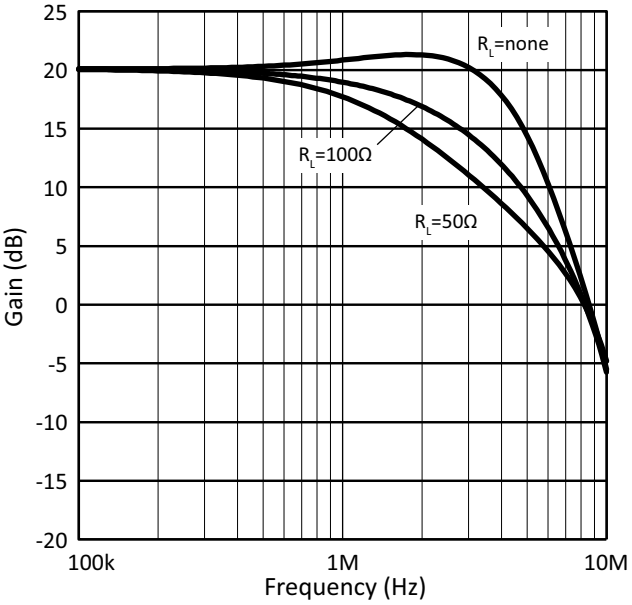


Figure 12: Small Signal Closed Loop Phase (Load)

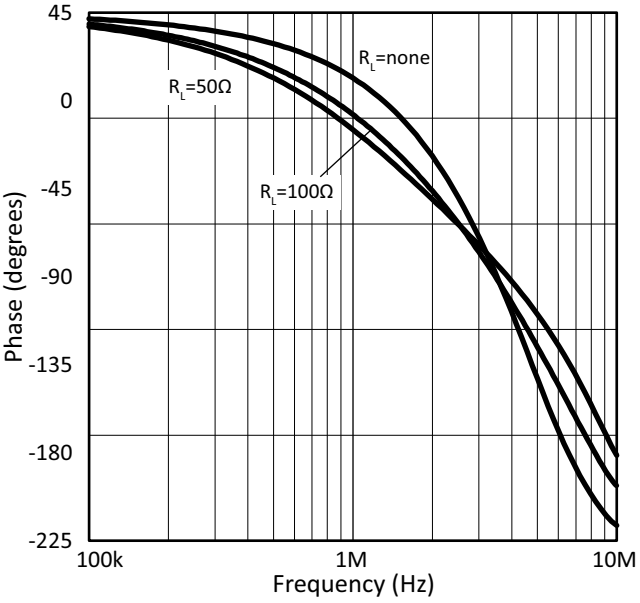


Figure 13: Small Signal Closed Loop Gain (Compensation)

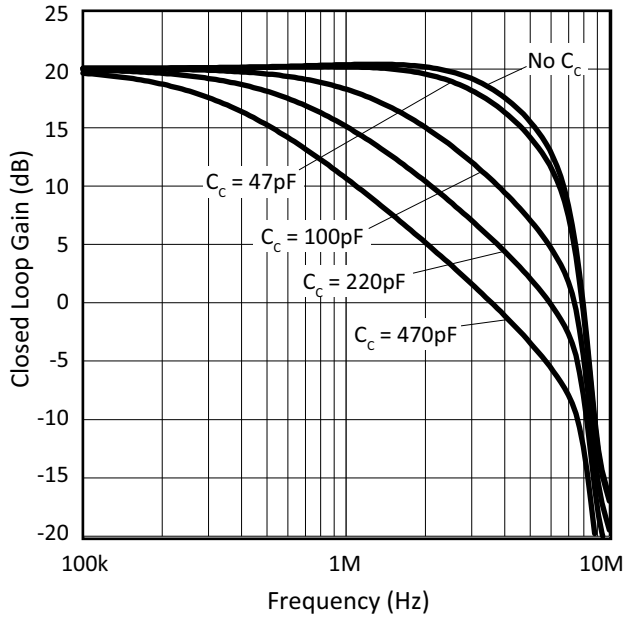


Figure 14: Small Signal Closed Loop Phase (Compensation)

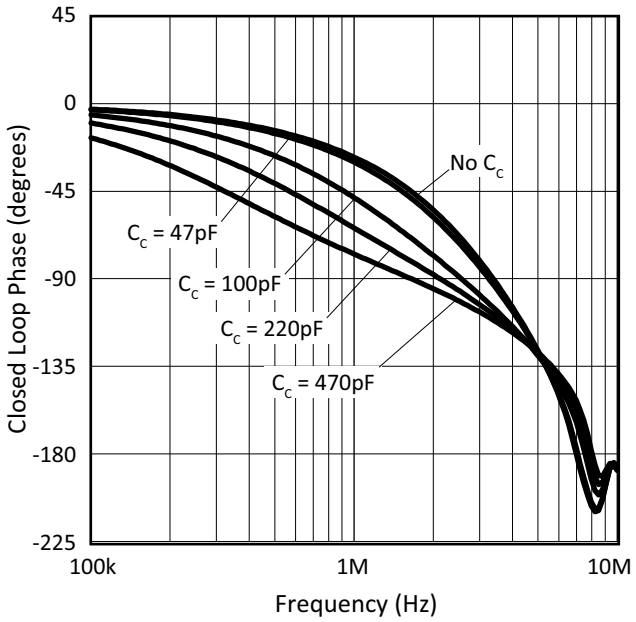


Figure 15: Quiescent Current

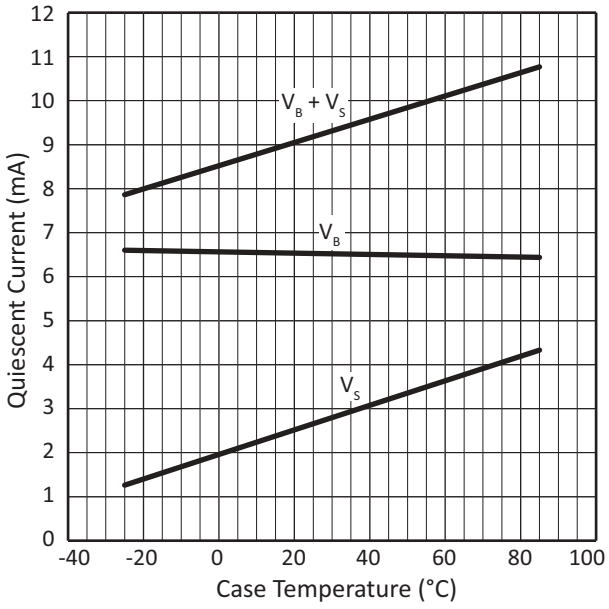


Figure 16: Current Limit

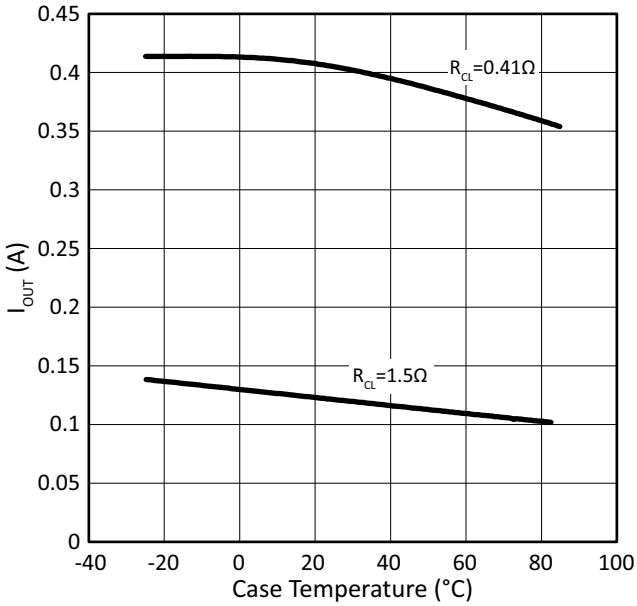


Figure 17: PSRR

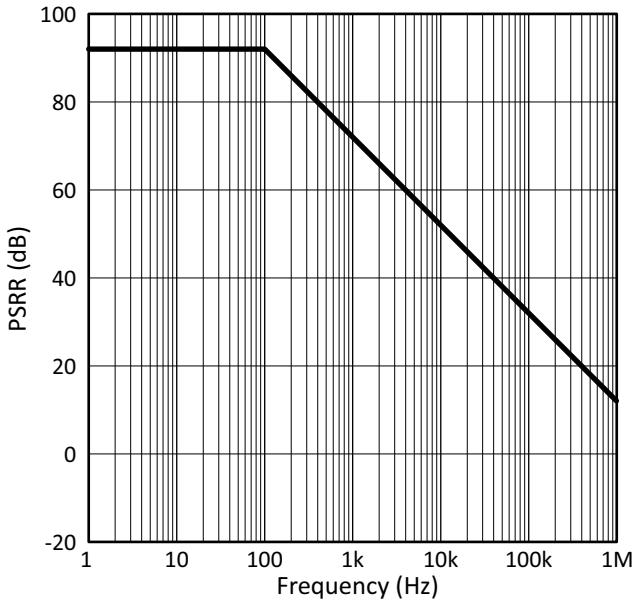


Figure 18: CHANNEL SEPARATION

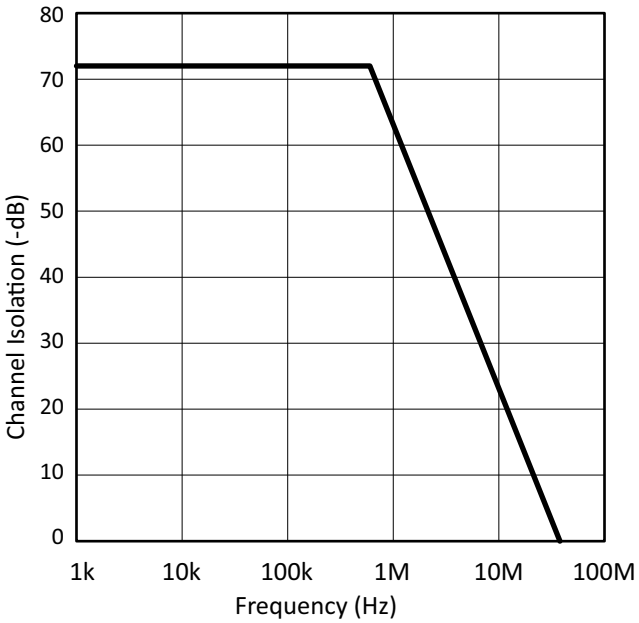
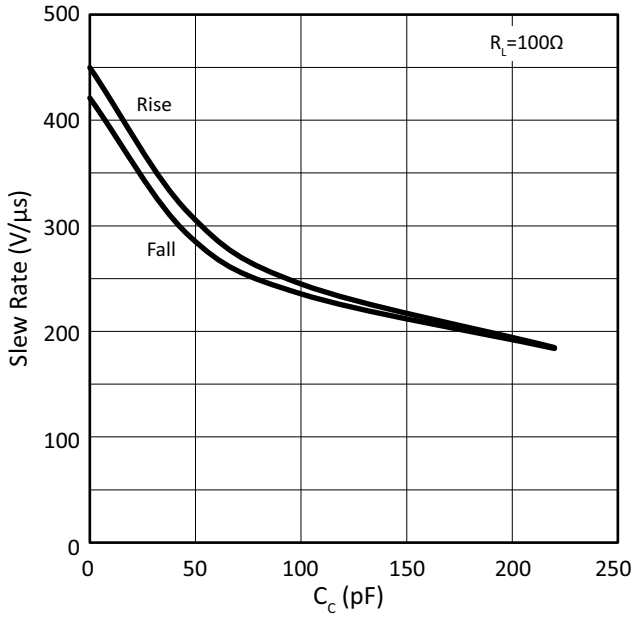


Figure 19: SLEW RATE vs. COMPENSATION

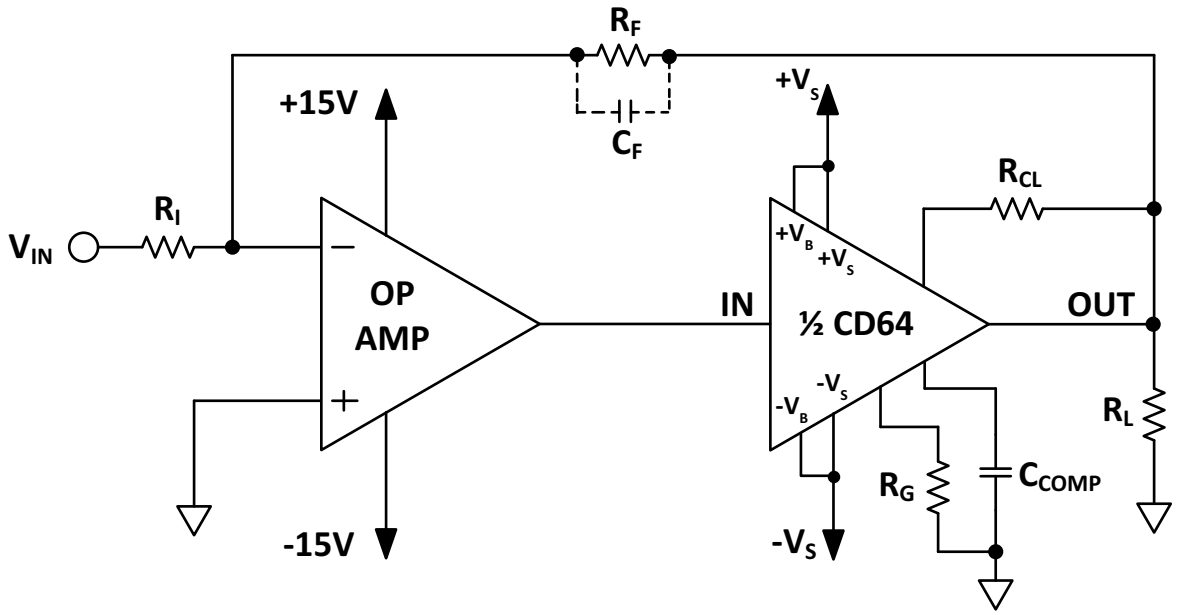


GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Figure 20: Typical Application (Inverting Composite Amplifier) with Single Supply



COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver.

STABILITY

Stability can be maximized by observing the following guidelines:

1. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster. Use the lowest possible booster gain.
2. Minimize phase shift within the loop.

A good compromise is to set total (composite) gain at least a factor of 3 times booster gain. Phase shift within the loop is minimized through use of loop compensation capacitor C_F when required. Typical values are 5 pF to 33 pF. Stability is the most difficult to achieve in a configuration where driver effective gain is unity (i.e.; total gain = booster gain).

BOOSTER GAIN

The gain of each section may be set independently by selecting a value for the gain setting resistor R_G according to the relation:

$$GAIN = 1 + \frac{2000\Omega}{R_G}$$

where R_G is in ohms. Recommended gain range is A_V = 3 V/V to A_V = 25 V/V.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The offset voltage of the booster over temperature must be taken into account. Note also that effects of booster gain accuracy should be considered when calculating maximum available driver swing.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the PB64. Use capacitors of at least 10 µF for each supply. Bypass the large capacitors with high quality ceramic capacitors (X7R) of 0.1 µF or greater.

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. +VB and -VB are connected to the small signal stages and +VS and -VS are connected to the high current output stage. An additional 5V on the +VB and -VB pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required, but 10V is recommended. When the boost feature is not needed, +VS and -VS are connected to the +VB and -VB pins respectively. The +VB and -VB pins must not be operated at supply voltages less than +VS and -VS respectively.

POWER SUPPLY SEQUENCING

If separate boost supplies are not used, then connect +VB to +VS and -VB to -VS. If separate boost supplies are used, then use the following sequence:

Turn ON Sequence: ±VS, ±VB

Turn OFF Sequence: ±VB, ±VS

To make sure ±VB are not less than 1 diode drop below ±VS, Apex recommends (small signal) diodes to be connected between +VS (anode) and +VB (cathode) and between -VS (cathode) and -VB (anode). Alternatively, replacing these diodes with 15V, 1W Zener diodes allows for the use of power supply sequencing when switching on and off. These Zener diodes will prevent voltage difference between VB and VS greater than

|15V| under either power supply sequence. With ±VB turned on before ±VS, the voltage difference between the two power supply pins will not exceed approximately 15V. This is well within the limit. With the standard power supply sequence, ±VS will still be clamped at 1 diode voltage drop below ±VB.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{LIM}) must be connected as shown in the typical connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms. The current limit function can be disabled by shorting the CL pin to the OUT pin.

$$R_{LIM}(\Omega) = \frac{0.7V}{I_{LIM}(A)}$$

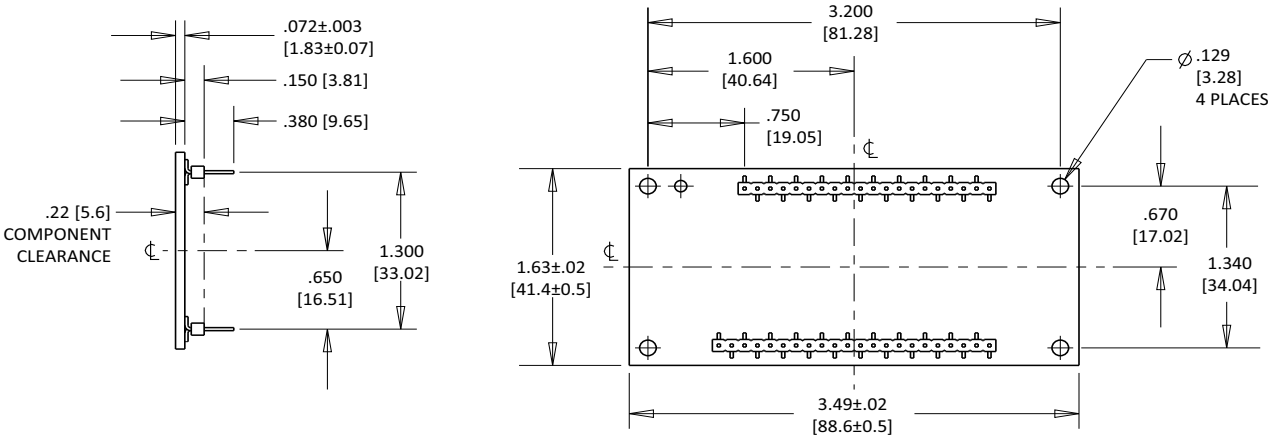
POWER SUPPLY PROTECTION

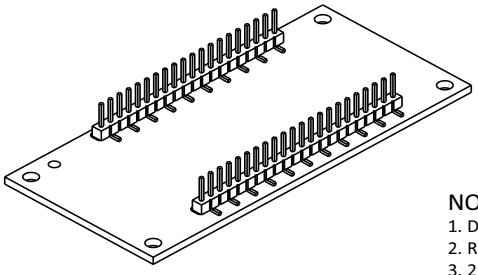
Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzorbs prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

PACKAGE OPTIONS

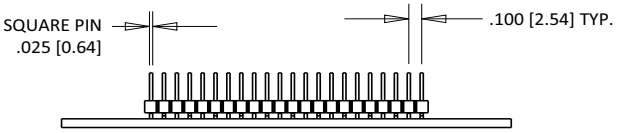
Part Number	Apex Package Style	Description
CD64GT	GT	42-pin Open Frame
CD64GTA	GT	42-pin Open Frame

PACKAGE STYLE GT





ISOMETRIC VIEW FOR REFERENCE ONLY



NOTES:
1. Dimensions are inches [mm].
2. Recommended PCB hole diameter for pins: 0.050 [1.27].
3. 2 oz copper over 600V dielectric aluminum substrate.
4. Tin over nickel plated phosphor bronze pins.
5. Package weight: 23 g (.81 oz).
6. Mount with #4 or equivalent screws.
7. It is not recommended that package mounting rely on the pins for mechanical support.

NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

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