



MDDG10R08G

100V N-Channel Enhancement Mode MOSFET

1. Description

This N-Channel MV MOSFET is produced using MDD Semiconductor's advanced Power Trench process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

2. Features

- Max $R_{DS(on)}$ = 8 m Ω at V_{GS} = 10 V, I_D = 35 A
- Extremely Low Reverse Recovery Charge, Q_{rr}
- 100% UIS Tested
- RoHS Compliant

3. Application

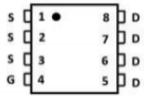
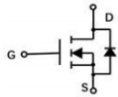
- Synchronous Rectification for AC / DC Quick Charger
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter
- Battery management System

4. Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	75	A
Pulsed Drain Current (Note 2)	I_{DM}	240	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	130	mJ
Thermal Resistance, steady-state	$R_{\theta JA}$	50	$^{\circ}\text{C}/\text{W}$
Power Dissipation	P_D	69	W
Junction Temperature	T_J	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	$-55 \sim +150$	$^{\circ}\text{C}$

Note: 1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating, pulse width limited by max. junction temperature.
3) E_{AS} condition : $T_J=25^{\circ}\text{C}$, $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $L=0.5\text{mH}$, $R_g=25\Omega$, $I_{AS}=23\text{A}$.

5. Pinning information

Pin	Symbol	Description	Simplified outline	Equivalent Circuit	Marking	Package
4	G	Gate			MDD G10R08G	PDFN5*6-8L
5-8	D	Drain				
1-3	S	Source				

6. T_A=25°C unless otherwise specified

Symbol	Parameter		Condition	Min	Typ	Max	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage		V _{GS} =0V, I _D =250μA	100	—	—	V
I _{SS}	Gate-Source Leakage Current	Forward	V _{GS} =20V	—	—	100	nA
		Reverse	V _{GS} =-20V	—	—	-100	nA
I _{DSS}	Drain-Source Leakage Current		V _{DS} =100V, V _{GS} =0V	—	—	1	μA
V _{GS(TH)}	Gate Threshold Voltage		V _{DS} =V _{GS} , I _D =250μA	1.5	2.0	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance		V _{GS} =10V, I _D =35A	—	6.0	8	mΩ
			V _{GS} =4.5V, I _D =30A	—	7.7	11	mΩ

7. Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C _{iss}	Input Capacitance	V _{GS} =0V	—	2000	—	pF
C _{oss}	Output Capacitance	V _{DS} =50V	—	638	—	pF
C _{rss}	Reverse Transfer Capacitance	f=1MHz	—	21	—	pF
Q _g	Total Gate Charge	V _{GS} =10V	—	41	—	nC
Q _{gs}	Gate Source Charge	V _{DS} =50V	—	10.3	—	nC
Q _{gd}	Gate Drain Charge	I _D =30A	—	7.5	—	nC

8. Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t _{d(on)}	Turn on Delay Time	V _{GS} =10V V _{DD} =50V I _D =30A R _G =2.7Ω	—	11	—	ns
t _r	Turn on Rise Time		—	36	—	ns
t _{d(off)}	Turn Off Delay Time		—	33	—	ns
t _f	Turn Off Fall Time		—	10	—	ns

9. Source Drain Diode Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{SD}	Drain-Source Diode Forward Voltage	I _S =30A, V _{GS} =0V	—	0.85	—	V
t _{rr}	Body Diode Reverse Recovery Time	I _F =30A	—	50	—	ns
Q _{rr}	Body Diode Reverse Recovery Charge	di/dt=100A/μs	—	71	—	nC

10. Test Circuits And Waveforms

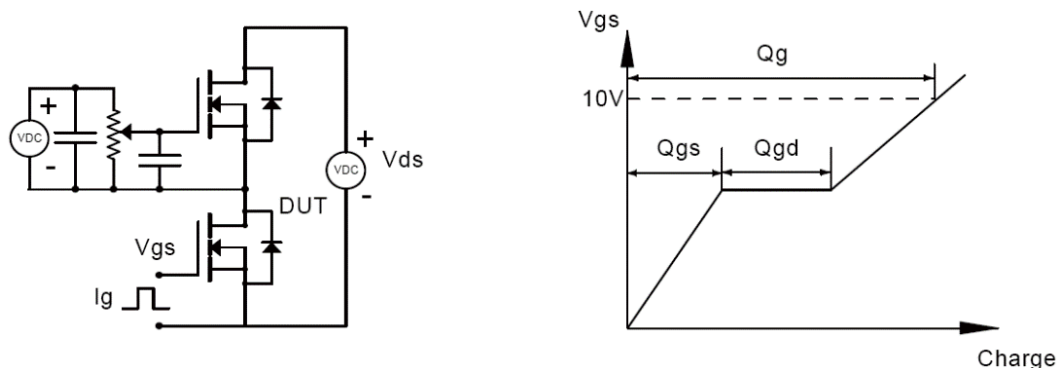


Figure 1. Gate charge test circuit & waveform

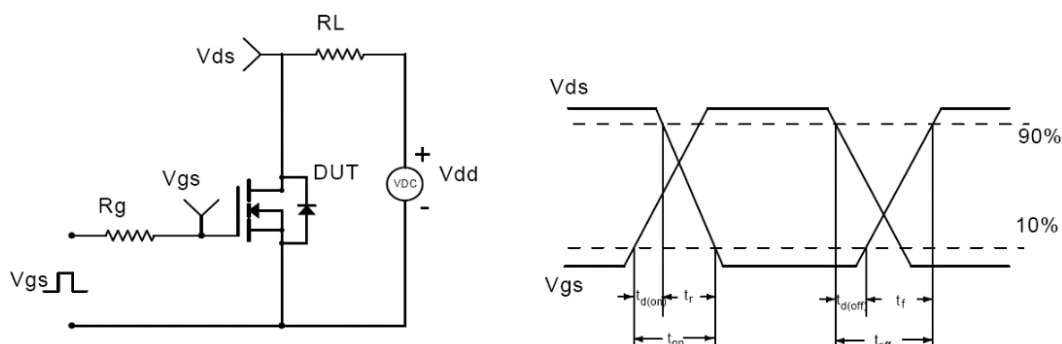


Figure 2. Switching time test circuit & waveforms

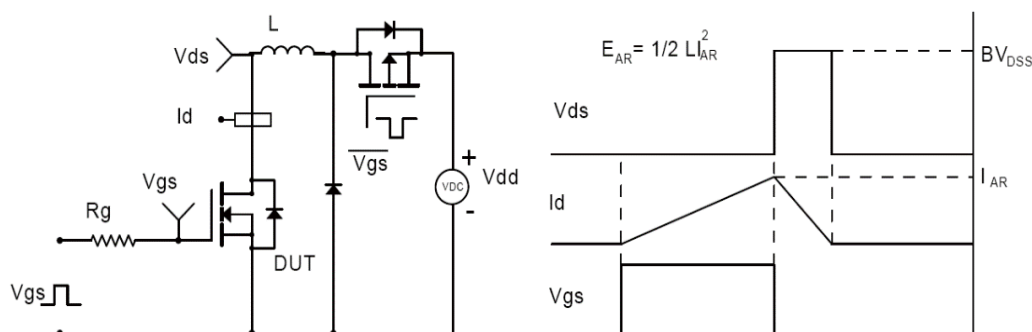


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

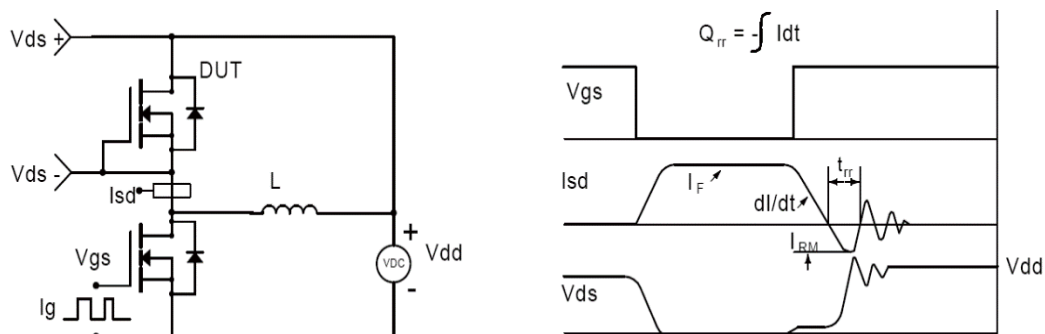


Figure 4. Diode reverse recovery test circuit & waveforms

II. Electrical Characteristics Diagrams

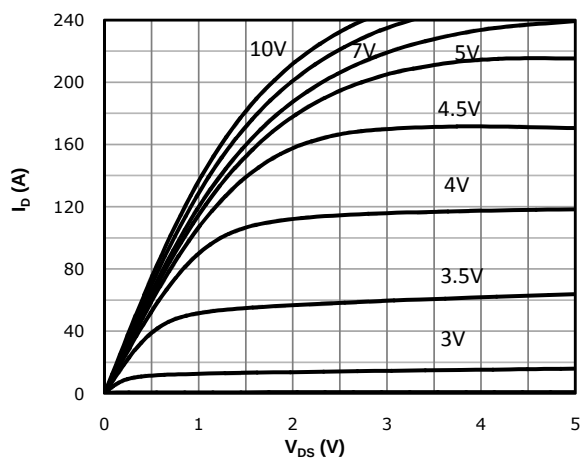


Figure 1. Typ. output characteristics

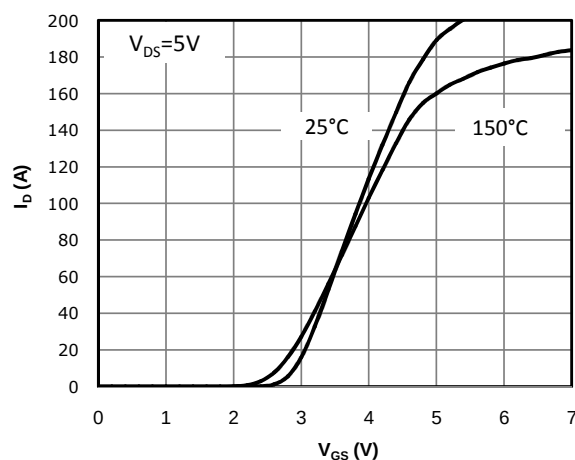


Figure 2. Typ. transfer characteristics

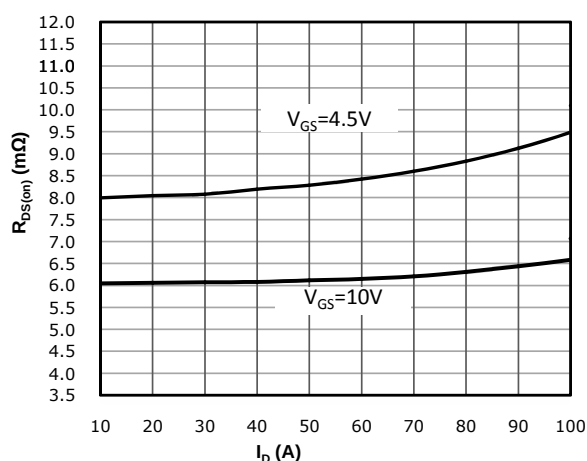


Figure 3. On-Resistance vs. Drain Current

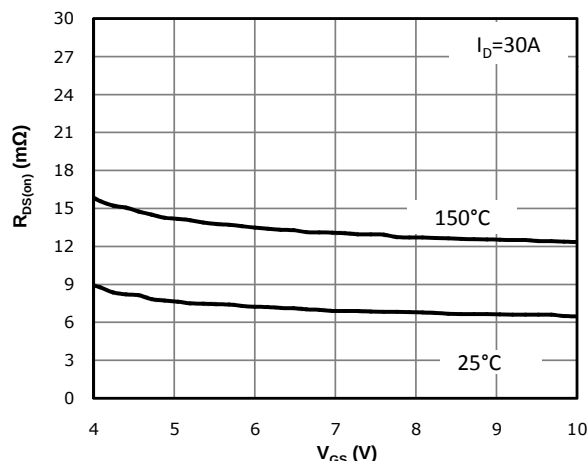


Figure 4. On-Resistance vs. Gate Voltage

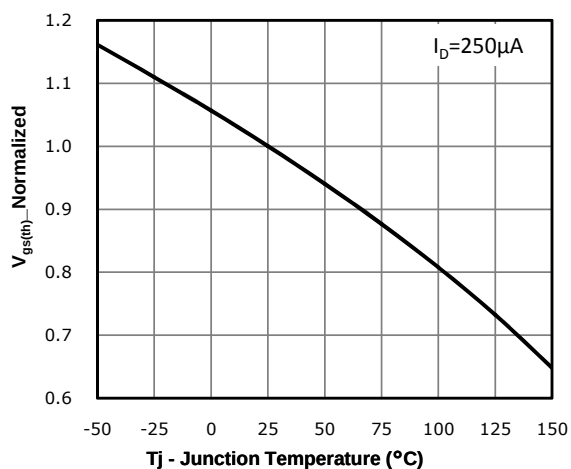


Figure 5. Normalized Threshold Voltage vs. Junction Temperature

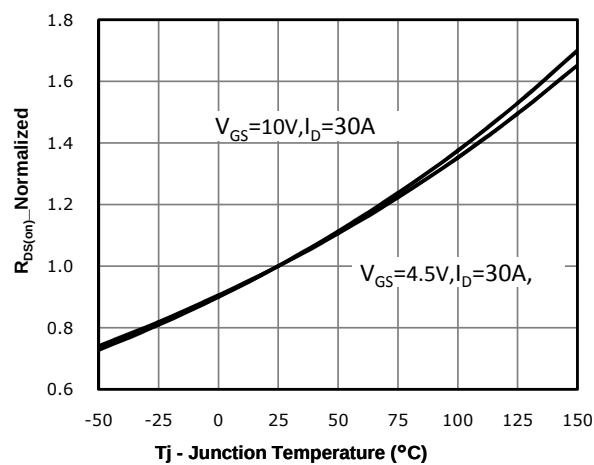
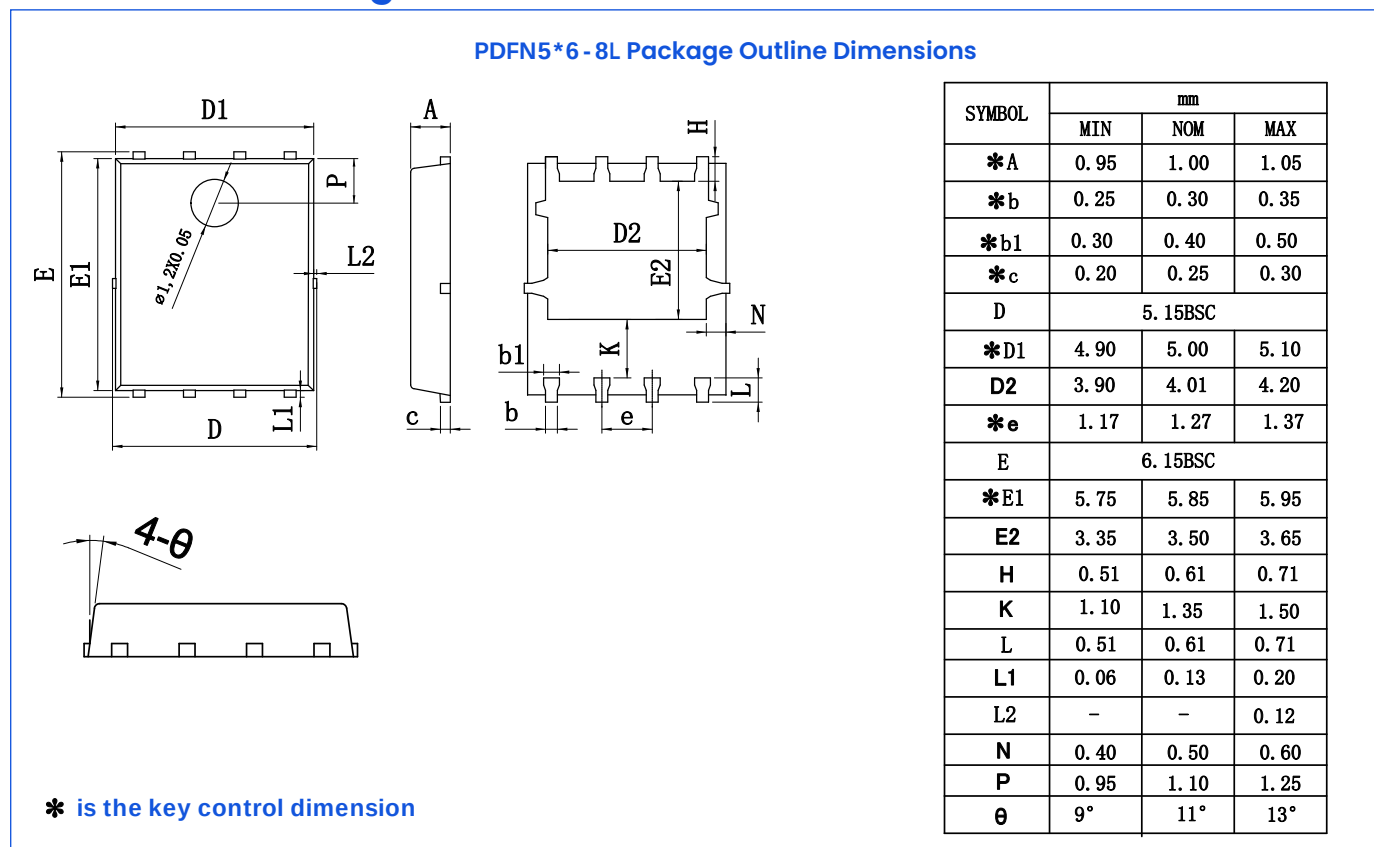


Figure 6. Forward characteristic of body diode

12. Outline Drawing



13. Important Notice and Disclaimer

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