PA04 • PA04A

Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- High Internal Dissipation — 200 Watts
- High Voltage, High Current — 200V, 20A
- High Slew Rate — 50V/µs
- 4 Wire Current Limit Sensing
- Low Distortion
- External Sleep Mode Control
- Optional Boost Voltage Inputs
- Evaluation Kit — See EK45

APPLICATIONS

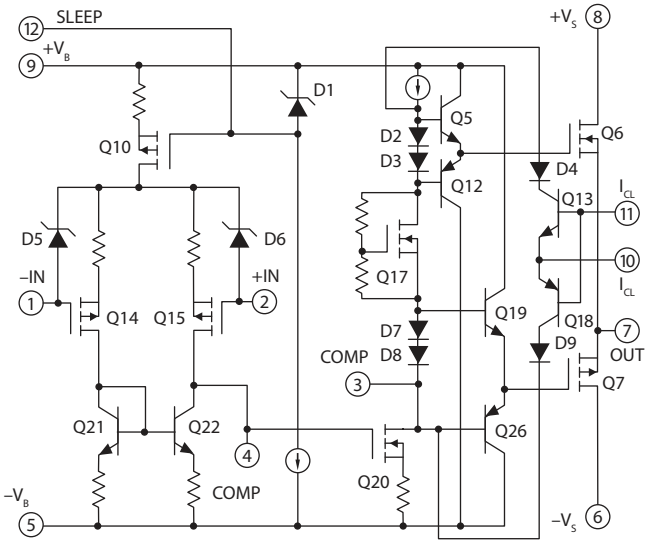
- Sonar Transducer Driver
- Linear and Rotary Motor Drives
- Yoke/Magnetic Field Excitation
- Programmable Power Supplies to ±95V
- Audio up to 400W

DESCRIPTION

The PA04 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

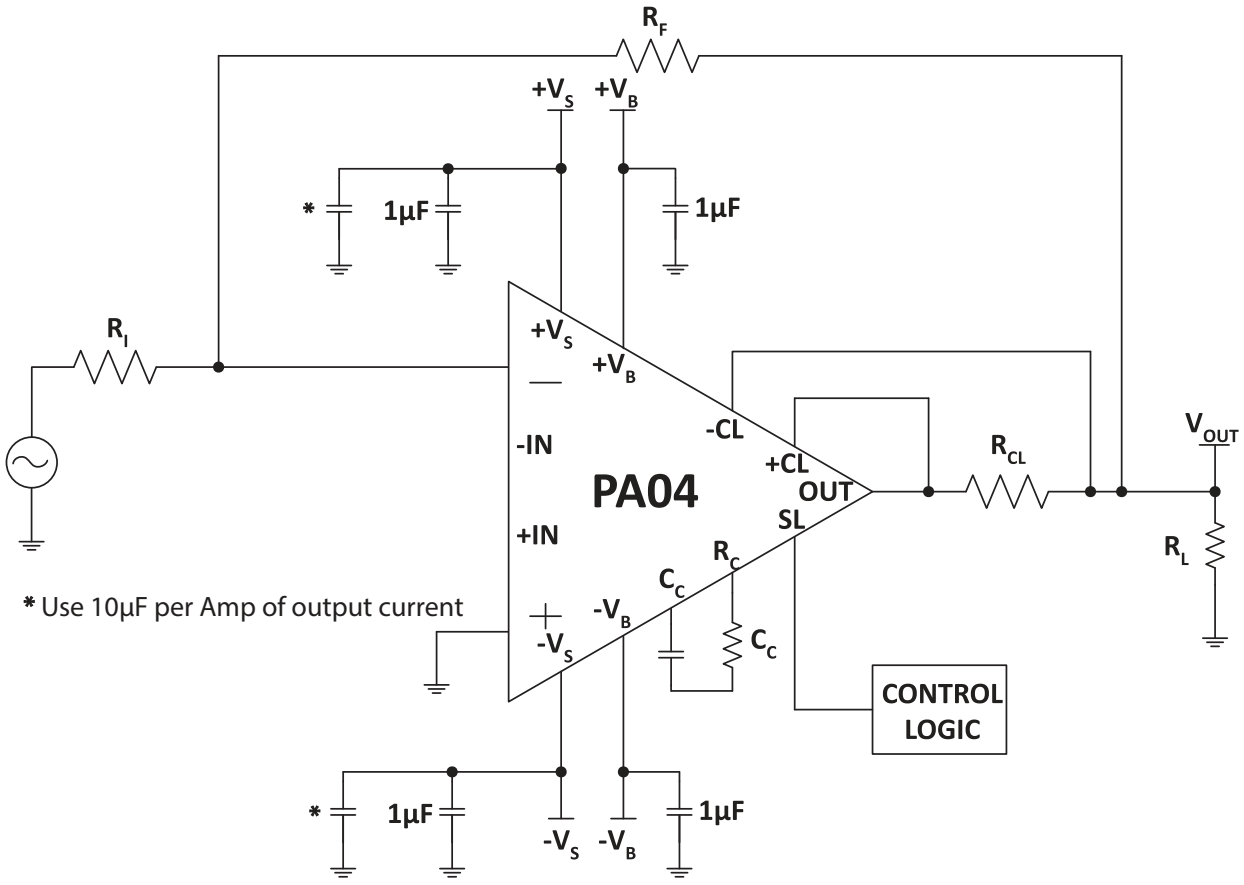
The PA04 is a highly flexible amplifier. The sleep mode feature allows ultra-low quiescent current for standby operation or load protection by disabling the entire amplifier. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external mΩ parasitic resistance in the output line.
The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible thermal washers will void product warranty.

Figure 1: Equivalent Schematic



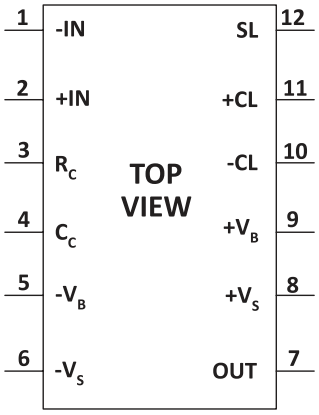
TYPICAL CONNECTION

Figure 2: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 3: External Connections



Pin Number	Name	Description
1	-IN	The inverting input.
2	+IN	The non-inverting input.
3	R_C	Compensation resistor connection. Select value based on Phase Compensation. See applicable section.
4	C_C	Compensation capacitor connection. Select value based on Phase Compensation. See applicable section.
5	$-V_B$	The negative boost supply rail. Short to $-V_S$ if unused. See applicable section.
6	$-V_S$	The negative supply rail.
7	OUT	The output. Connect this pin to load and to the feedback resistors through R_{CL}.
8	$+V_S$	The positive supply rail.
9	$+V_B$	The positive boost supply rail. Short to $+V_S$ if unused. See applicable section.
10	-CL	Connect to the load side of the current limit resistor. Current limit will activate as the voltage across R_{CL} increases.
11	+CL	Connect to the OUT side of the current limit resistor. Current limit will activate as the voltage across R_{CL} increases.
12	SL	The sleep mode activation pin. See applicable section.

SPECIFICATIONS

Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 Ω. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_B = \pm V_S$.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_s$ to $-V_s$		200	V
Boost Voltage	$\pm V_B$		$\pm V_S \pm 20V$	V
Output Current, within SOA	I_{OUT}		20	A
Power Dissipation, internal	P_D		200	W
Input Voltage, differential	$V_{IN\ (Diff)}$	-20	20	V
Input Voltage, common mode	V_{CM}	$-V_S$	V_S	V
Temperature, pin solder, 10s			350	°C
Temperature, junction [1]	T_J		150	°C
Temperature, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.

CAUTION The PA04 is constructed from MOSFET transistors. ESD handling procedures must be observed. The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA04			PA04A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial			5	10		2	5	mV
Offset Voltage vs. temperature	Full temp range		30	50		10	30	µV/°C
Offset Voltage vs. supply			15			*		µV/V
Offset Voltage vs. power	Full temp range		30			10		µV/W
Bias Current, initial			10	50		5	20	pA
Bias Current vs. supply			0.01			*		pA/V
Offset Current, initial			10	50		5	20	pA
Input Impedance, DC			10^{11}			*		Ω
Input Capacitance			13			*		pF
Common Mode Voltage Range	Full temp range	$\pm V_B$-8			*			V
Common Mode Rejection, DC	Full temp range, V_{CM} = ±20V	86	98		*	*		dB
Input Noise	100 kHz BW, R_I = 1 kΩ		10			*		µVrms

GAIN

Parameter	Test Conditions	PA04			PA04A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop, @ 15 Hz	Full temp range, C_C = 100pF	94	102		*	*		dB
Gain Bandwidth Product	I_{OUT} = 10A		2			*		MHz
Power Bandwidth	R_L=4.5 Ω, V_{OUT} = 180V p-p C_C=100pF, R_C=120 Ω		90			*		kHz
Phase Margin	Full temp range		60			*		°

OUTPUT

Parameter	Test Conditions	PA04			PA04A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing	I_{OUT} = 15A	$\pm V_S$-8.8	$\pm V_S$-7.5		*	*		V
Voltage Swing	V_B= Vs + 5V, I_{OUT} = 20A	$\pm V_S$-6.8	$\pm V_S$-5.5		*	*		V
Current, peak		20			*			A
Settling Time to 0.1%	A_V = 1, 10V step, R_L = 4 Ω		2.5			*		µs
Slew Rate	A_V = 10, C_C= 100pF, R_C=120 Ω	40	50		*	*		V/µs
Capacitive Load	Full temp range, A_V = +1	10			*			nF
Resistance			2			*		Ω

POWER SUPPLY

Parameter	Test Conditions	PA04			PA04A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±15	±75	±100	*	*	*	V
Current, quiescent, boost supply			30	40		*	*	mA
Current, quiescent, total			70	90		*	*	mA
Current, quiescent, total, sleep mode	Full temp range		3	5		*	*	mA

THERMAL

Parameter	Test Conditions	PA04			PA04A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case[1]	Full temp range, F>60 Hz		0.3	0.4		*	*	°C/W
Resistance, DC, junction to case	Full temp range, F<60 Hz		0.5	0.6		*	*	°C/W
Resistance[2], junction to air	Full temp range		12			*		°C/W
Temperature Range, case	Meets full range specification	-25		85	*		*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
2. The PA04 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

Note: *The specification of PA04A is identical to the specification for PA04 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 4: Power Derating

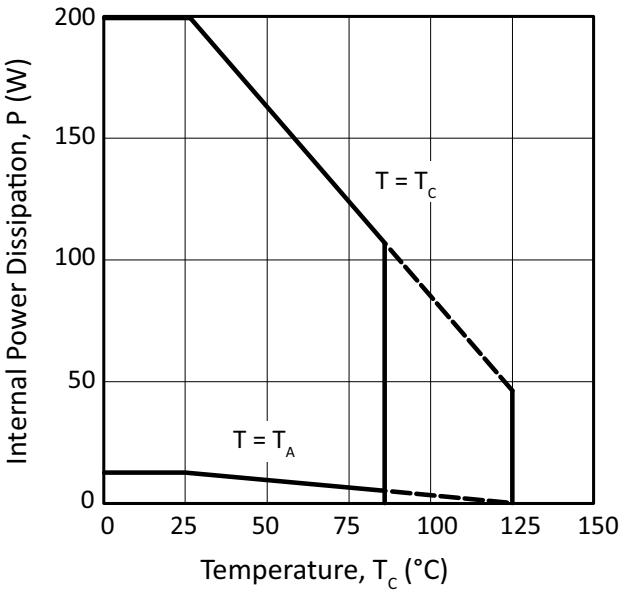


Figure 5: Power Supply Rejection

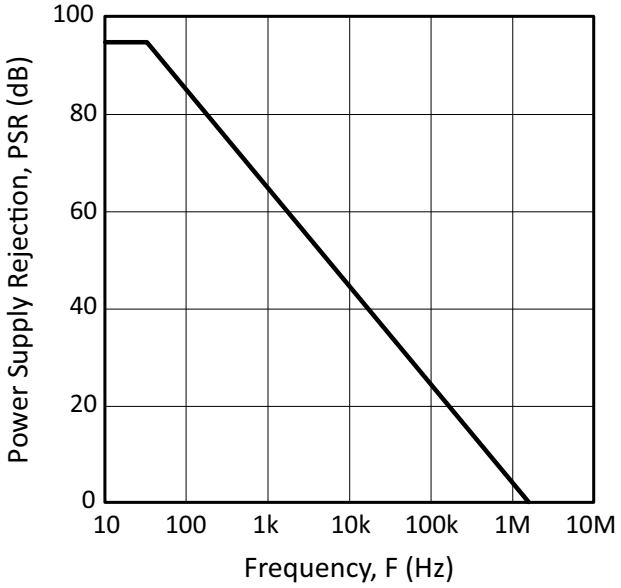


Figure 6: Small Signal Gain

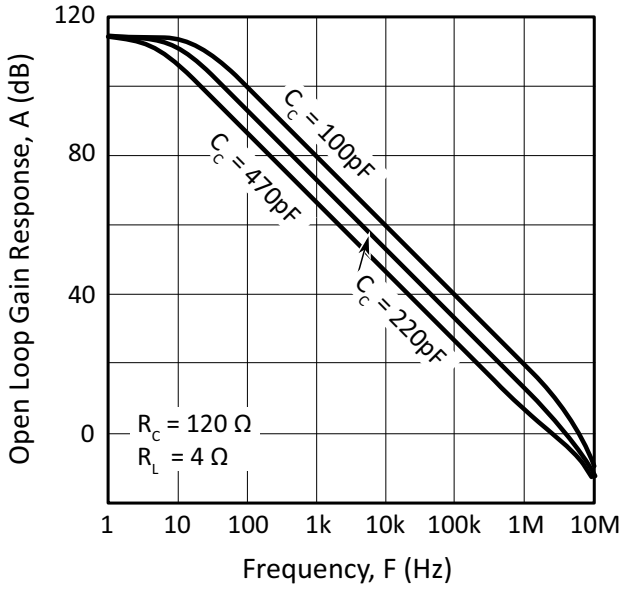


Figure 7: Small Signal Phase

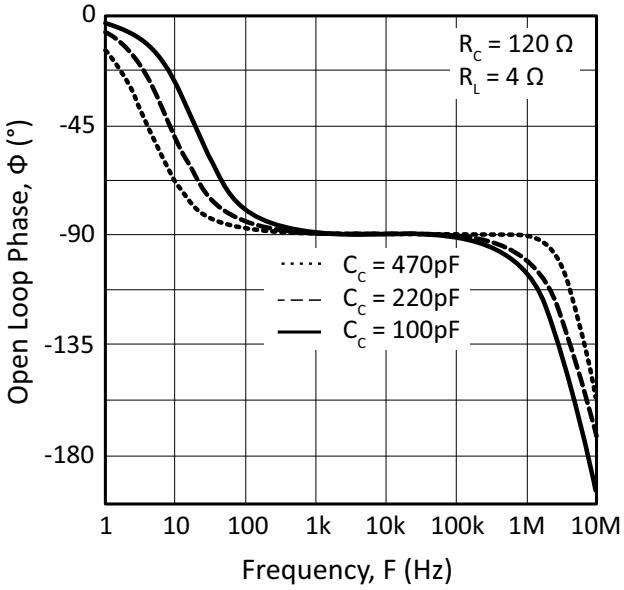


Figure 8: Slew Rate

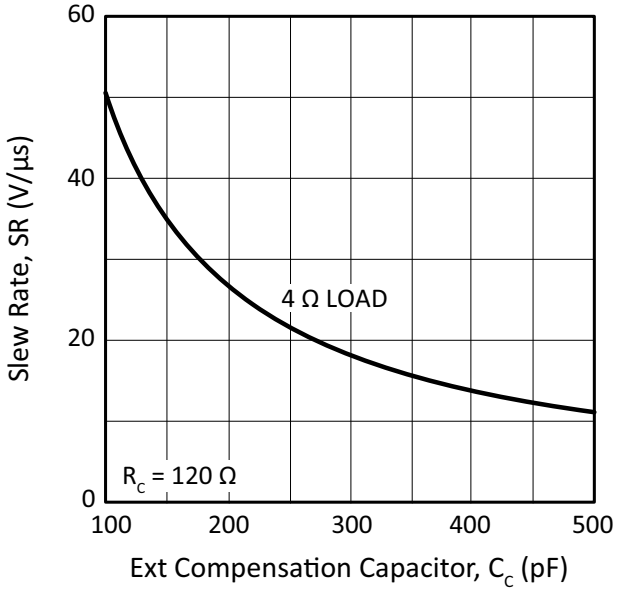


Figure 9: Output Voltage Swing

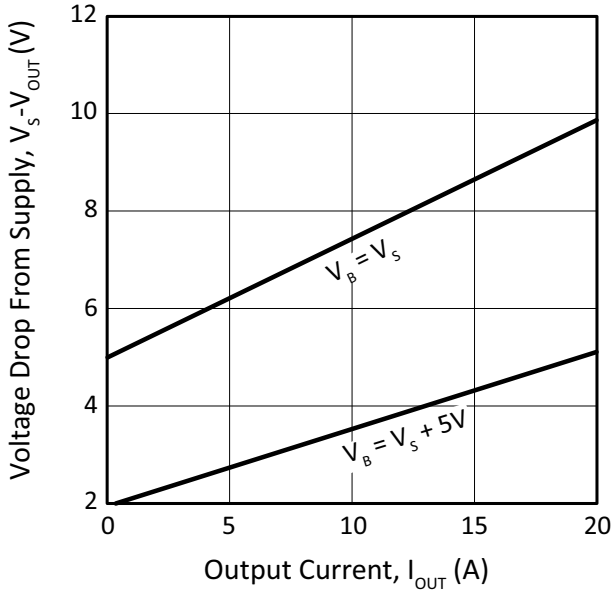


Figure 10: Common Mode Rejection

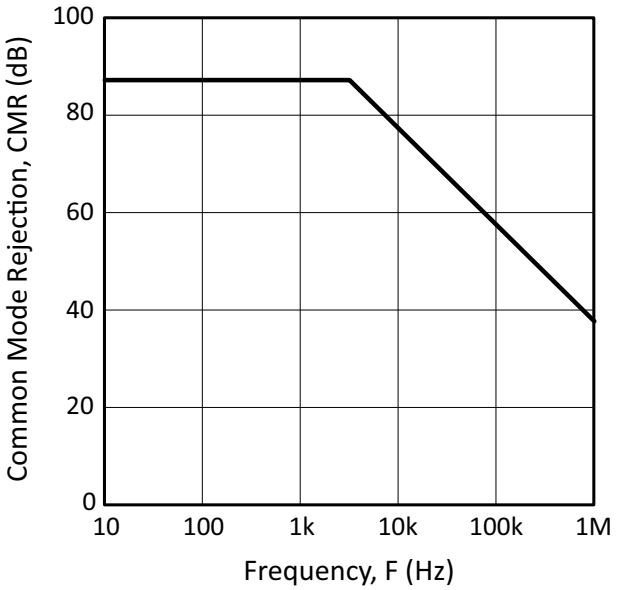


Figure 11: Pulse Response

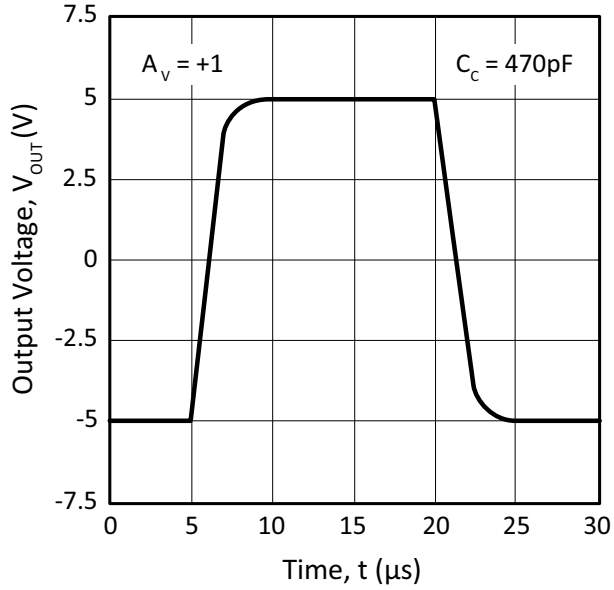


Figure 12: Current Limit

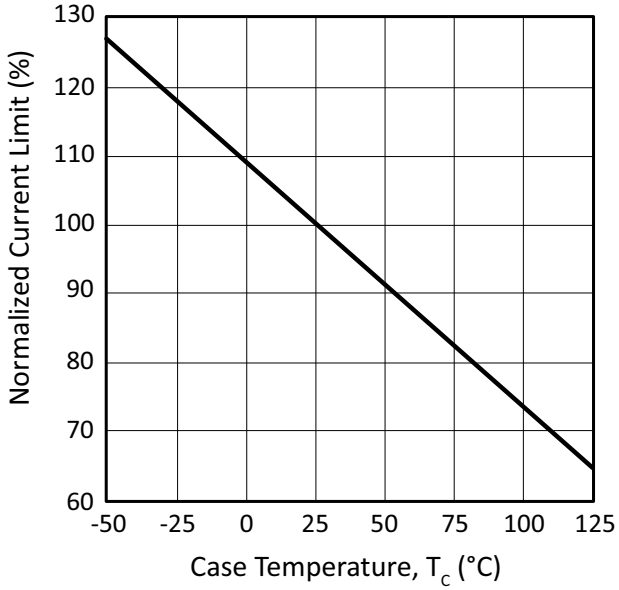


Figure 13: Harmonic Distortion

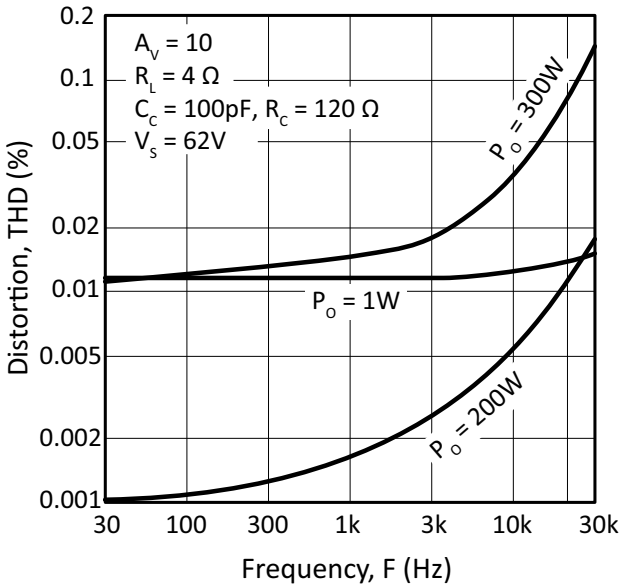


Figure 14: Quiescent Current

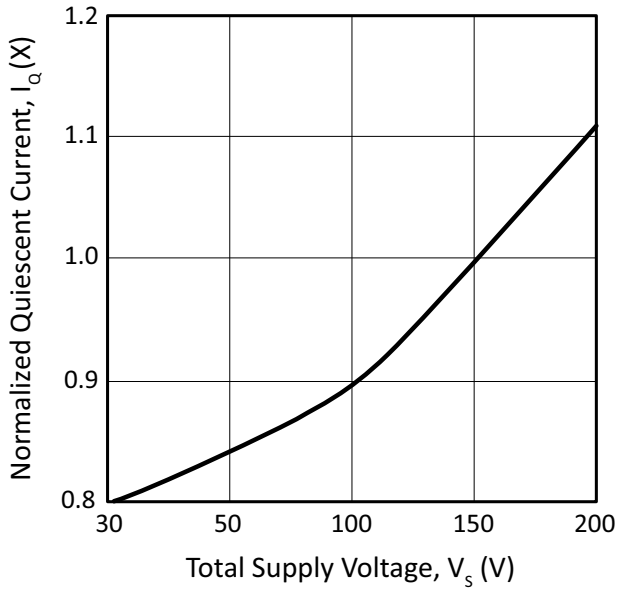
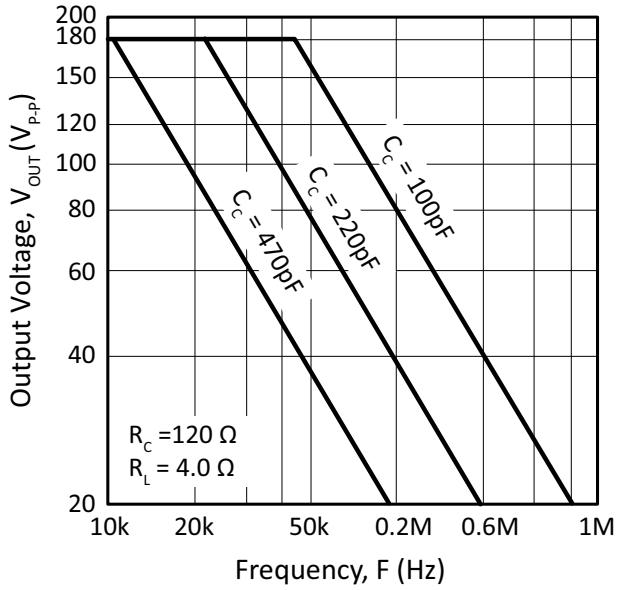


Figure 15: Power Response



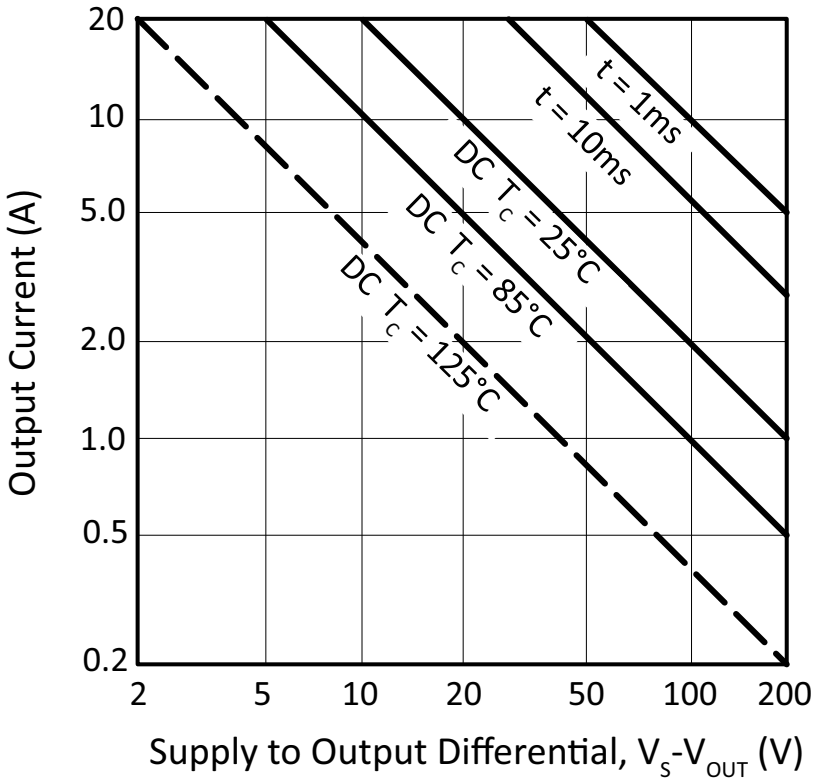
SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

Note: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 16: SOA

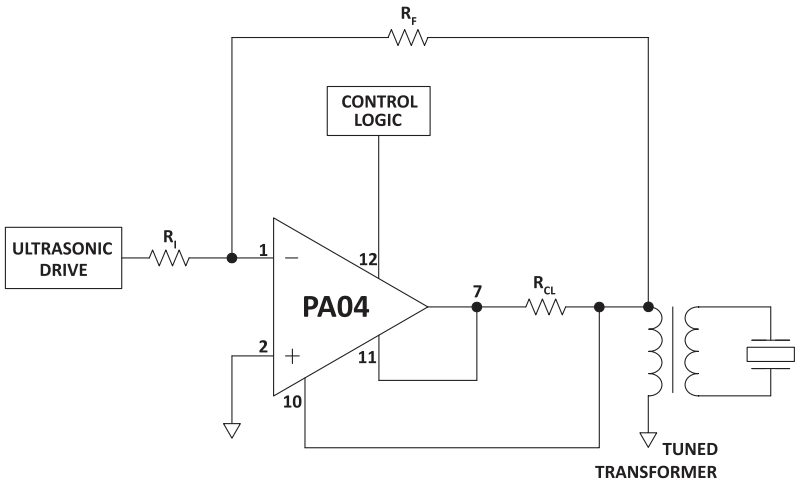


GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Figure 17: Typical Application (Sonar Transducer Driver)



The high power bandwidth and high voltage output of the PA04 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA04. Control logic turns off the amplifier in sleep mode.

PHASE COMPENSATION

Gain	C_C*	R_C
≥1	470pF	120 Ω
≥3	220pF	120 Ω
≥10	100pF	120 Ω

C_C Rated For Full Supply Voltage

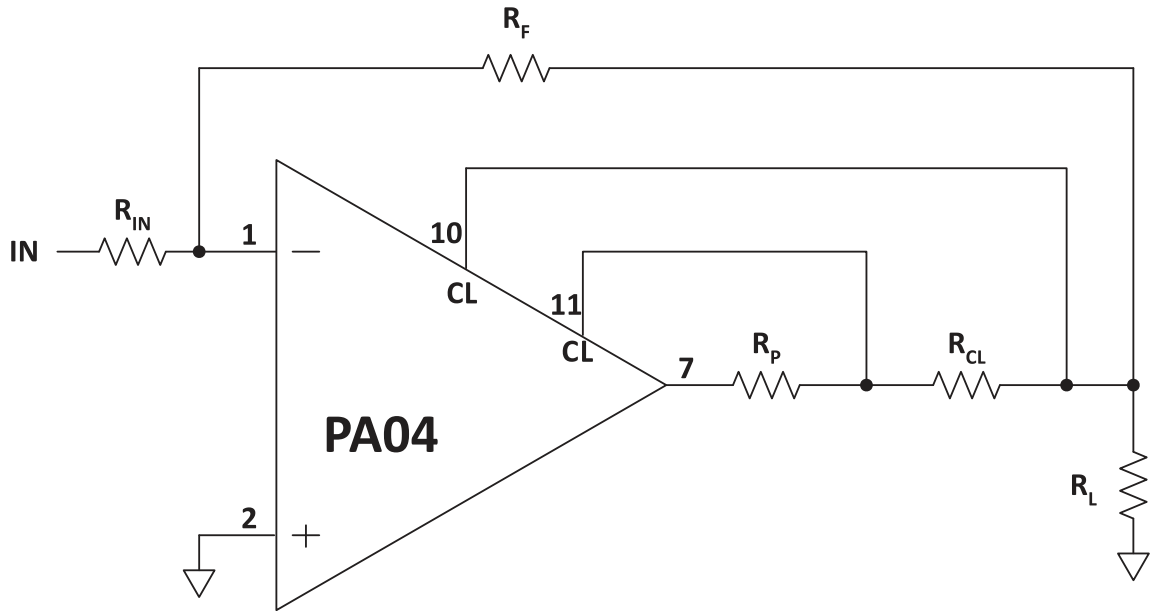
*See “BOOST OPERATION” paragraph.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 18. This connection will bypass any parasitic resistances, R_P, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 18.
The value of the current limit resistor can be calculated as follows:

$$R_{CL}(\Omega) = \frac{0.76V}{I_{CL}(A)}$$

Figure 18: Current Limit



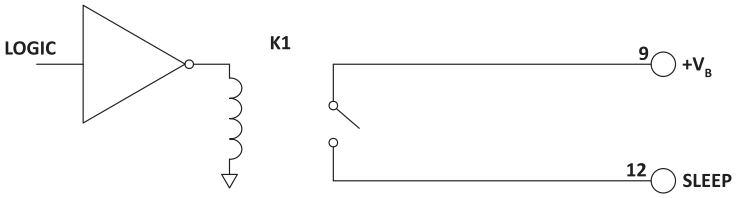
SLEEP MODE OPERATION

To activate sleep mode, connect pin 12 (sleep) to pin 9 ($+V_B$). This disables the amplifier's internal reference and the amplifier shuts down except for a trickle current of 3 mA which flows into pin 12. Pin 12 should be left open if the sleep mode is not required.

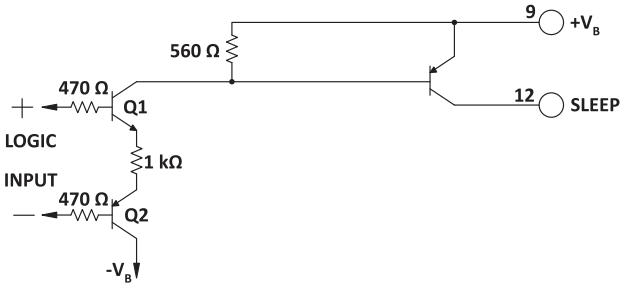
Several possible circuits can be built to take advantage of this mode. In Figure 19a a small signal relay is driven by a logic gate. This removes the requirement to deal with the common mode voltage that exists on the shutoff circuitry since the sleep mode is referenced to the $+V_B$ voltage.

In Figure 19b, circuitry is used to level translate the sleep mode input signal. The differential input activates sleep mode with a differential logic level signal and allows common mode voltages to $\pm V_B$.

Figure 19: Sleep Mode Current



a. Sleep Mode Circuit



b. Sleep Mode Circuit

BOOST OPERATION

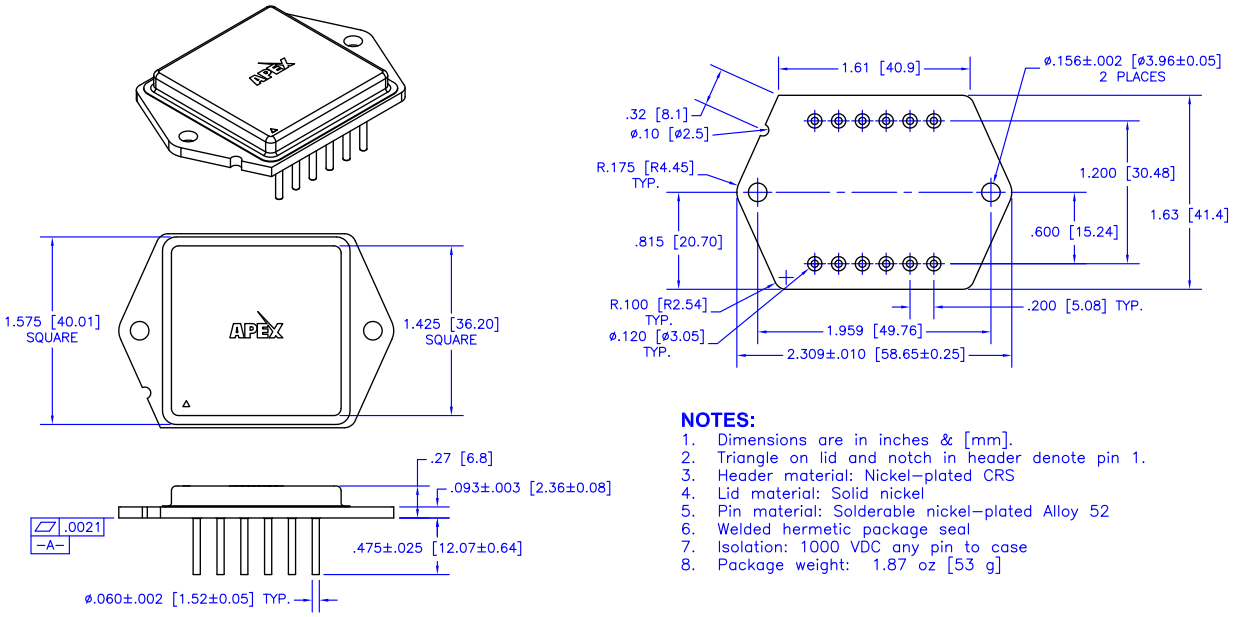
With the V_B feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_B$ (pin 9) and $-V_B$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_B pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_B$ and $+V_S$ pins must be strapped together as well as the $-V_B$ and $-V_S$ pins. The V_B pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

PACKAGE DESIGN

PACKAGE STYLE CR



NOTES:

1. Dimensions are in inches & [mm].
2. Triangle on lid and notch in header denote pin 1.
3. Header material: Nickel–plated CRS
4. Lid material: Solid nickel
5. Pin material: Solderable nickel–plated Alloy 52
6. Welded hermetic package seal
7. Isolation: 1000 VDC any pin to case
8. Package weight: 1.87 oz [53 g]