

Features

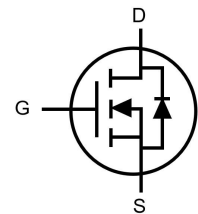
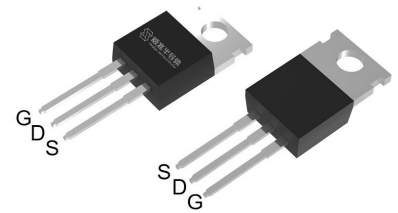
- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® II Technology
- 100% Avalanche Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses



Part ID	Package Type	Marking	Packing
VST002N06MS-K	TO-220AB	002N06M	50pcs/Tube

V_{DS}	60	V
$R_{DS(on),TYP@ V_{GS}=10V}$	2.2	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	3.3	mΩ
$I_D(\text{Wire bond limited})$	180	A

TO-220AB



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		60	V
V_{GS}	Gate-Source voltage		± 20	V
I_S	Diode continuous forward current (Wire bond limited)	$T_C = 25^\circ\text{C}$	180	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	180	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 100^\circ\text{C}$	141	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	800	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	20	A
		$T_A = 70^\circ\text{C}$	16	A
E_{AS}	Maximum Avalanche energy, single pulsed ②		289	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$	214	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$	2.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.6	0.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	50	60	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j =25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	—	—	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =60V,V _{GS} =0V	—	—	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)⑦	V _{DS} =60V,V _{GS} =0V	—	—	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	—	—	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	1.3	1.8	2.4	V
R _{DS(on)}	Drain-Source On-State Resistance ⑧	V _{GS} =10V, I _D =40A	—	2.2	2.75	mΩ
		(T _j =100°C) ⑦	—	3.2	—	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ⑧	V _{GS} =4.5V, I _D =30A	—	3.3	4.3	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance ⑦	V _{DS} =30V,V _{GS} =0V, f=100KHz	—	3180	—	pF
C _{oss}	Output Capacitance ⑦		—	895	—	pF
C _{rss}	Reverse Transfer Capacitance ⑦		—	30	—	pF
R _g	Gate Resistance ⑦	f=1MHz	—	1	—	Ω
Q _g (10V)	Total Gate Charge ⑦	V _{DS} =30V,I _D =40A, V _{GS} =10V	—	52	—	nC
Q _g (4.5V)	Total Gate Charge ⑦		—	26	—	nC
Q _{gs}	Gate-Source Charge ⑦		—	9.8	—	nC
Q _{gd}	Gate-Drain Charge ⑦		—	9.5	—	nC
Switching Characteristics ⑦						
T _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =40A, R _G =3Ω, V _{GS} =10V	—	11	—	ns
T _r	Turn-on Rise Time		—	62	—	ns
T _{d(off)}	Turn-Off Delay Time		—	40	—	ns
T _f	Turn-Off Fall Time		—	47	—	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A,V _{GS} =0V	—	0.83	1	V
T _{rr}	Reverse Recovery Time ⑦	V _{DD} =30V I _{sd} =40A, V _{GS} =0V	—	43	—	ns
Q _{rr}	Reverse Recovery Charge ⑦	di/dt=100A/μs	—	36	—	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② This maximum value is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 34A, V_{GS} = 10V; 100% FT tested at L = 0.5mH, I_{AS} = 24A.
- ③ The power dissipation Pd is based on T_j(max), using junction-to-case thermal resistance RθJC.
- ④ The power dissipation Pdsm is based on T_j(max), using junction-to-ambient thermal resistance RθJA.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
- ⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

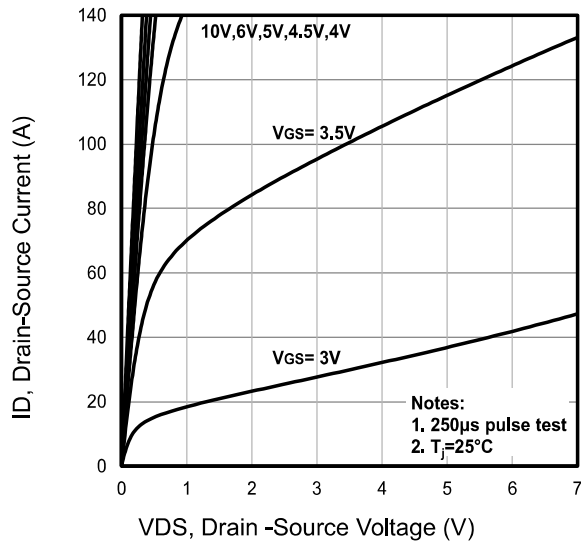


Fig1. Typical Output Characteristics

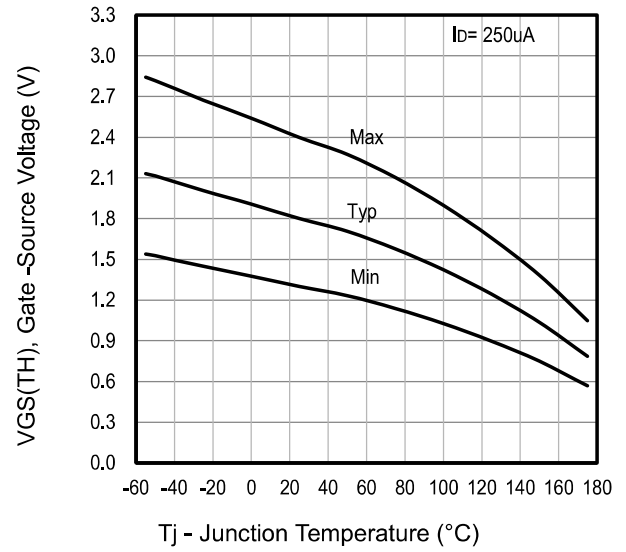


Fig2. Typical $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

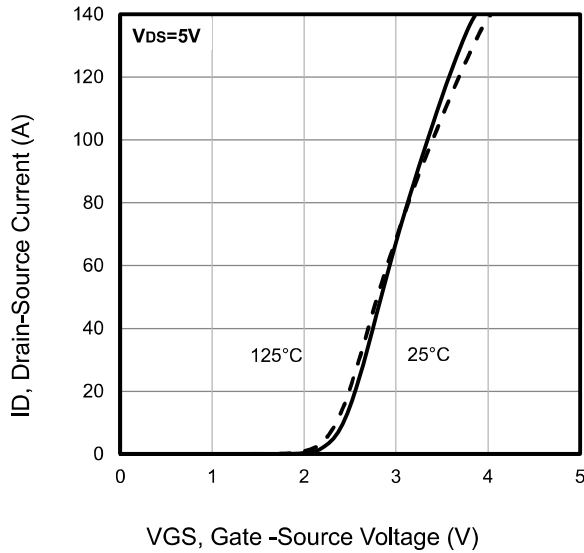


Fig3. Typical Transfer Characteristics

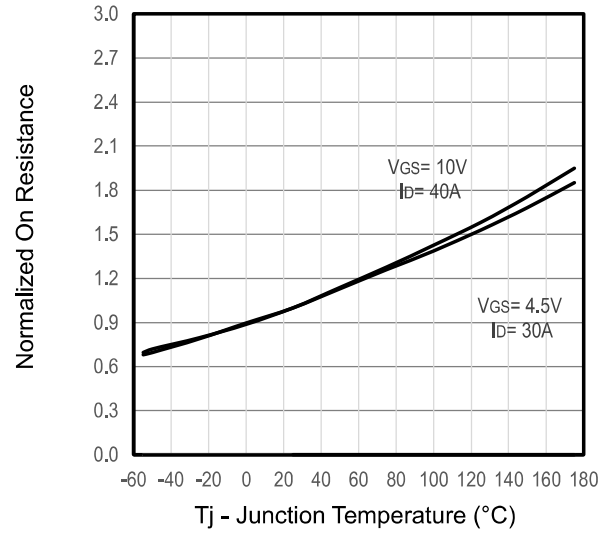


Fig4. Typical Normalized On-Resistance Vs. T_j

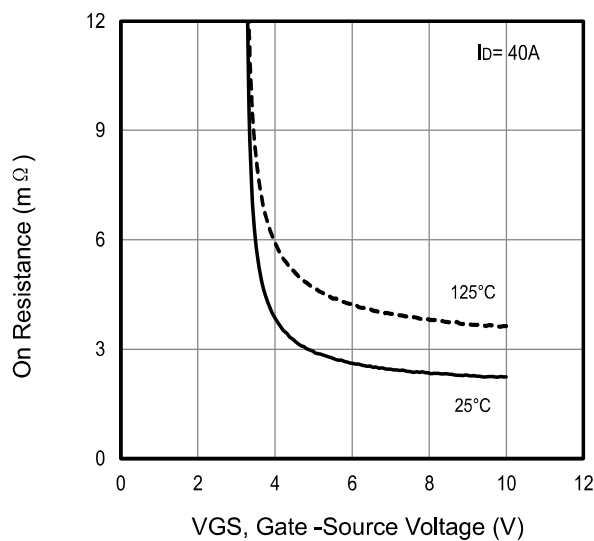


Fig5. Typical On Resistance Vs Gate-Source Voltage

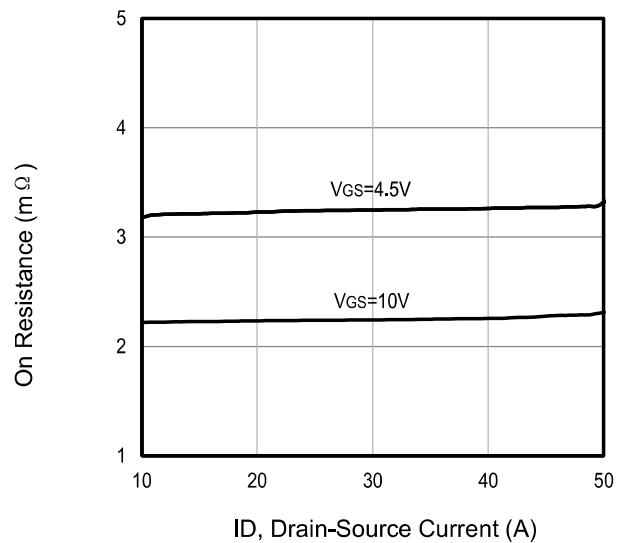


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

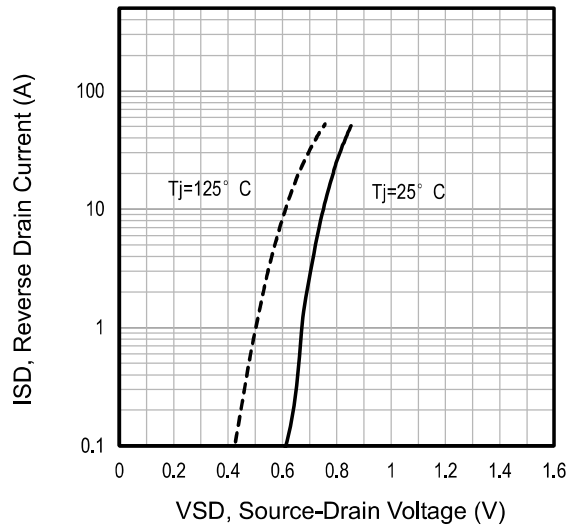


Fig7. Typical Source-Drain Diode Forward Voltage

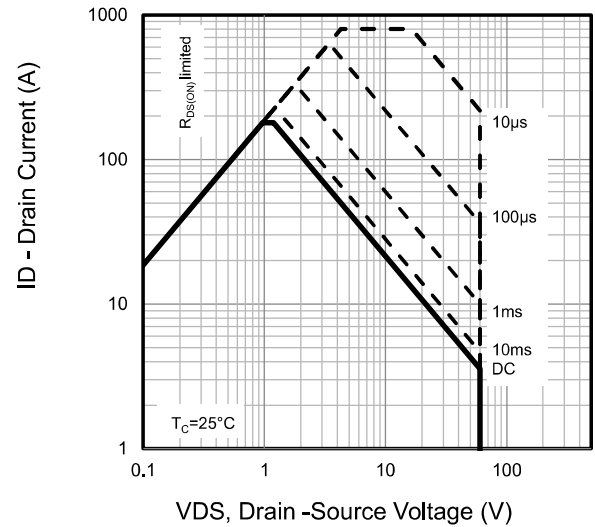


Fig8. Maximum Safe Operating Area

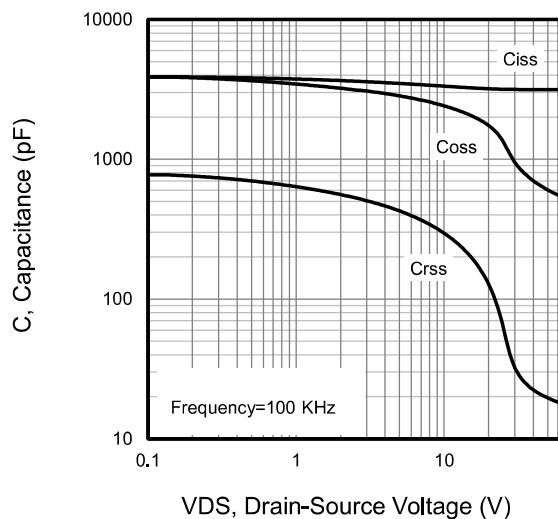


Fig9. Typical Capacitance Vs. Drain-Source Voltage

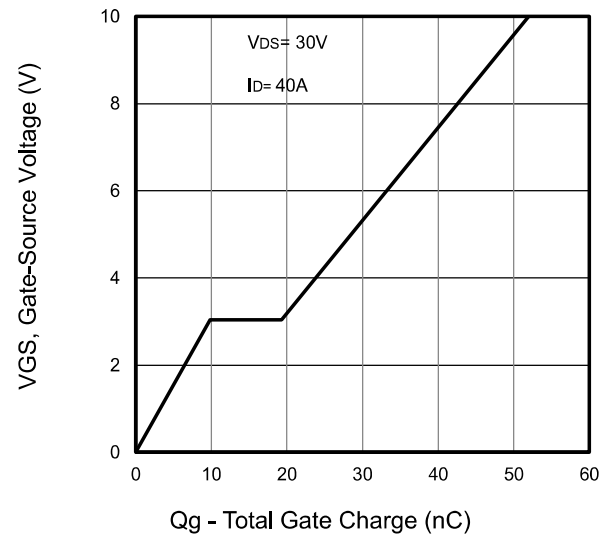


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

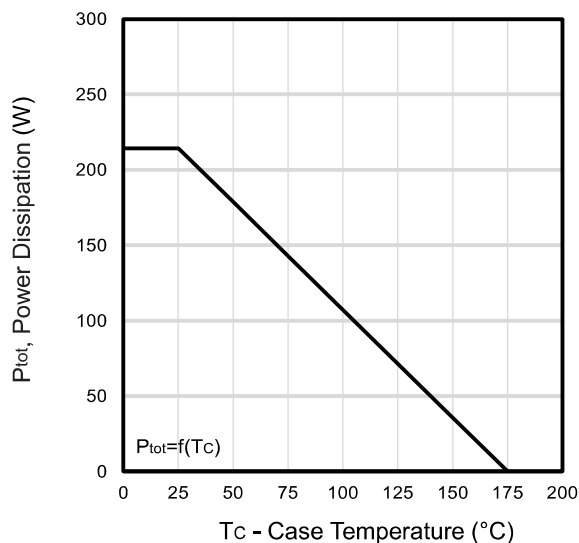


Fig11. Power Dissipation Vs. Case Temperature

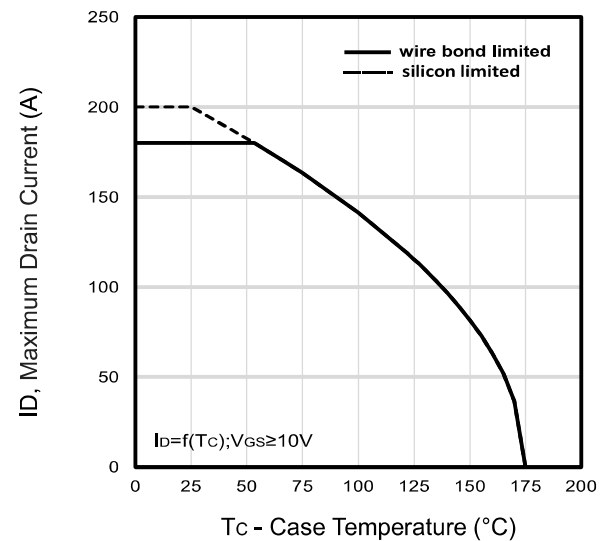


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

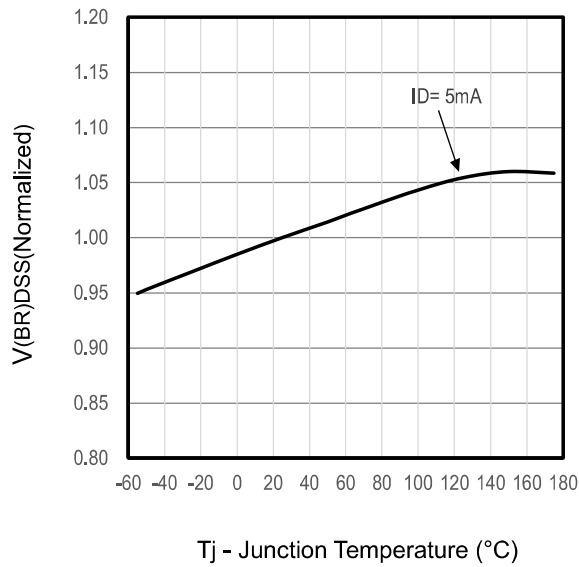


Fig13. Typical V(BR)DSS Vs Tj

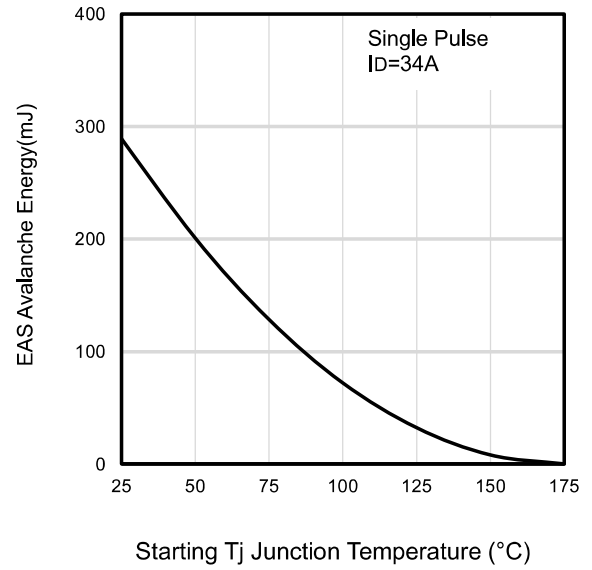


Fig14. Maximum Avalanche Energy vs Temperature (°C)

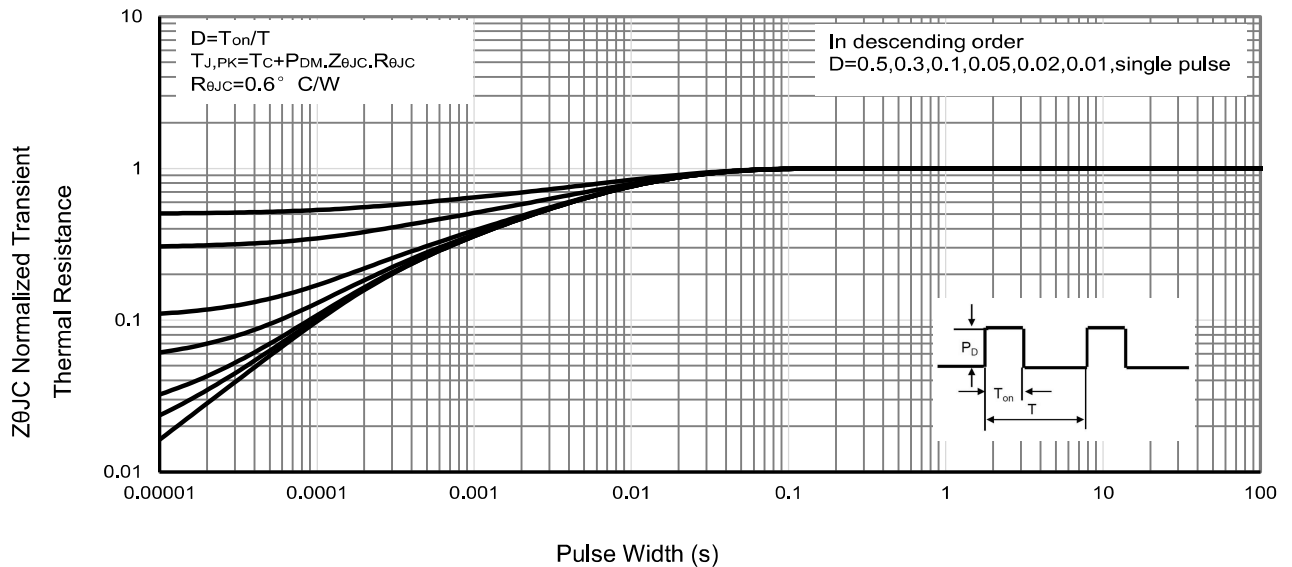


Fig15 . Normalized Maximum Transient Thermal Impedance

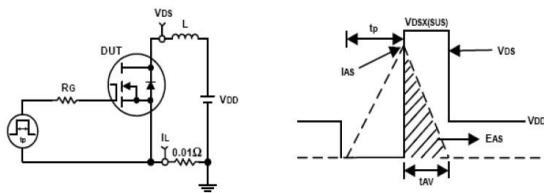


Fig16. Unclamped Inductive Test Circuit and waveforms

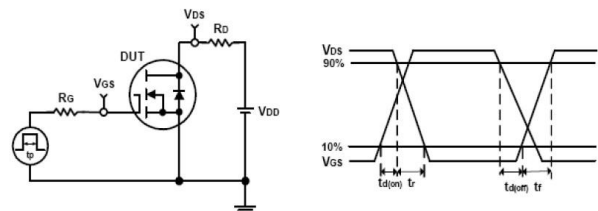
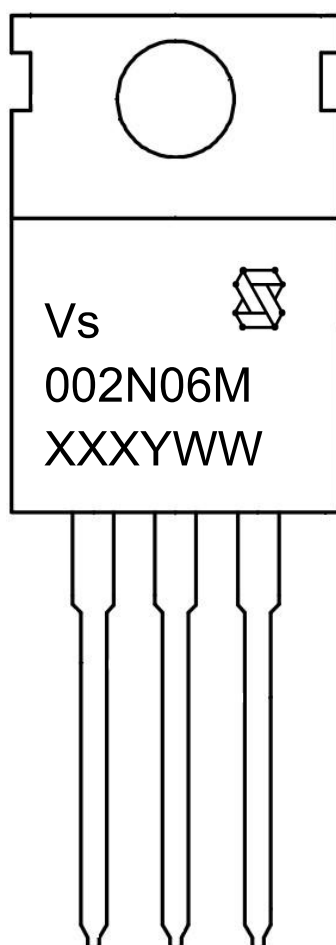


Fig17. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (002N06M)

3rd line: Date code (XXXYWW)

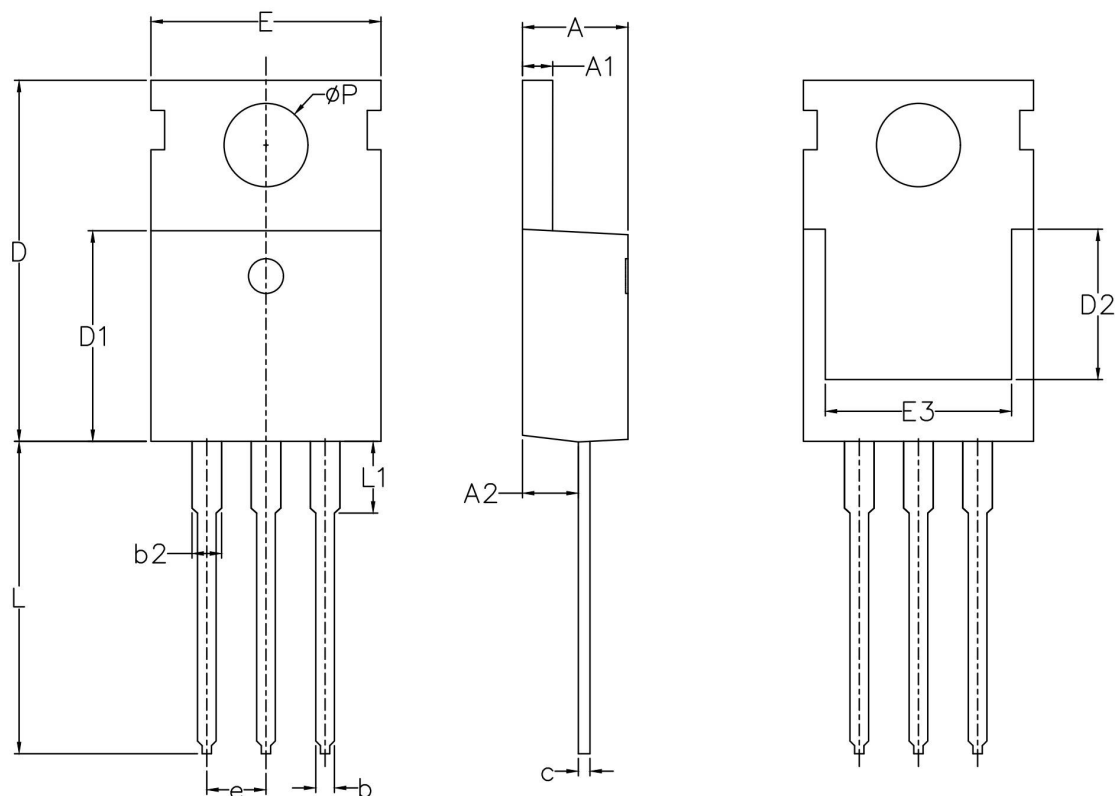
XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.35	4.57	4.70
A1	1.25	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.27	1.47
c	0.45	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	--	--
E	9.70	10.00	10.30
E3	7.00	--	--
e	2.54 BSC		
L	12.75	13.50	13.85
L1	--	3.10	3.40
ϕP	3.40	3.60	3.80

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash.
Mold flash shall not exceed 0.127mm per side.
3. Thermal pad contour optional within dimensions E,H1,D2&E1.
4. Dimension E2&H1 define A zone where stamping and singulation irregularities are allowed.