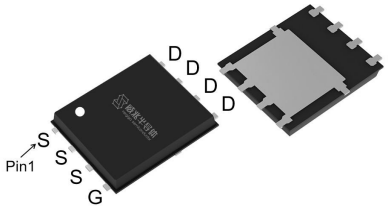
Features

V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	3.8	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	5.6	mΩ
$I_{D(Wire\ bond\ limited)}$	120	A

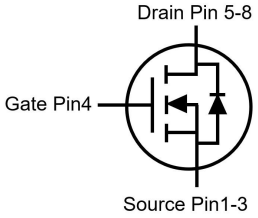
- Enhancement mode
- Low RDS(on) to minimize conduction losses
- VitoMOS® Ⅱ Technology
- 100% Avalanche tested, 100% Rg tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

PDFN5x6



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS18208GPM	PDFN5x6	18208GPM	3000pcs/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		100	V
V_{GS}	Gate-source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	T_C = 25°C	120	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	120	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	85	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	515	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	16	A
		T_A = 70°C	13	A
EAS	Maximum avalanche energy, single pulsed ②		420	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	174	W
		T_C = 100°C	69	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	2.6	W
		T_A = 70°C	1.7	W
T_J,T_{STG}	Operating junction and storage temperature range		-55 to 150	°C

Thermal characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑤	0.6	0.72	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑥	40	48	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250μA	100	–	–	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=100V,V_{GS}=0V	–	–	1	μA
	Zero gate voltage drain current(Tj=125℃)⑦	V_{DS}=100V,V_{GS}=0V	–	–	100	μA
I_{GSS}	Gate-body leakage current	V_{GS}=±20V,V_{DS}=0V	–	–	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=250μA	1.6	2.1	2.7	V
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=10V, I_D=40A	–	3.8	5.3	mΩ
		Tj=100℃ ⑦	–	5.6	–	mΩ
$R_{DS(on)}$	Drain-source on-state resistance ⑧	V_{GS}=4.5V, I_D=30A	–	5.6	7.5	mΩ
G_{FS}	Forward transconductance	V_{DS}=5V, I_D=40A	–	57	–	S
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑦	V_{DS}=50V,V_{GS}=0V, f=100kHz	–	4010	–	pF
Coss	Output capacitance ⑦		–	995	–	pF
Crss	Reverse transfer capacitance ⑦		–	25	–	pF
Rg	Gate resistance	f=1MHz	–	1.5	–	Ω
Qg(10V)	Total gate charge ⑦	V_{DS}=50V,I_D=40A, V_{GS}=10V	–	58	–	nC
Qg(4.5V)	Total gate charge ⑦		–	27	–	nC
Qgs	Gate-source charge ⑦		–	14	–	nC
Qgd	Gate-drain charge ⑦		–	8	–	nC
Switching Characteristics ⑦						
Td(on)	Turn-on delay Time	V_{DD}=50V, I_D=40A, R_G=3Ω, V_{GS}=10V	–	13	–	ns
Tr	Turn-on rise Time		–	37	–	ns
Td(off)	Turn-off delay Time		–	41	–	ns
Tf	Turn-off fall Time		–	37	–	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	–	0.85	1	V
Trr	Reverse recovery time ⑦	V_{DD}=50V I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	–	44	–	ns
Qrr	Reverse recovery charge ⑦		–	43	–	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② This maximum value is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 41A, V_{GS} =10V； 100% FT tested at L = 0.1mH, I_{AS} = 50A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cold plate.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

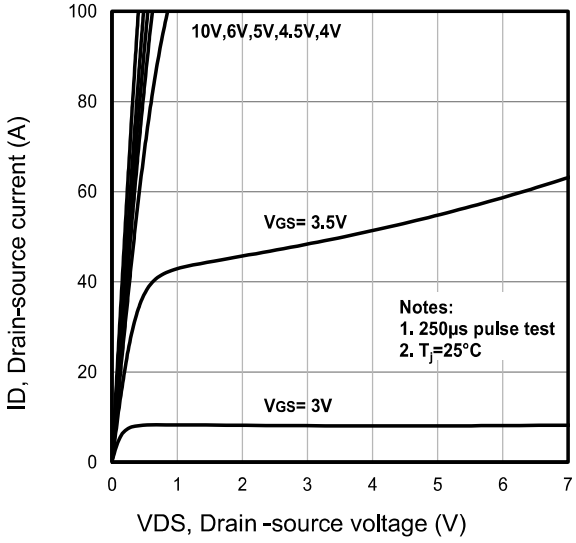


Fig1. Typical output characteristics

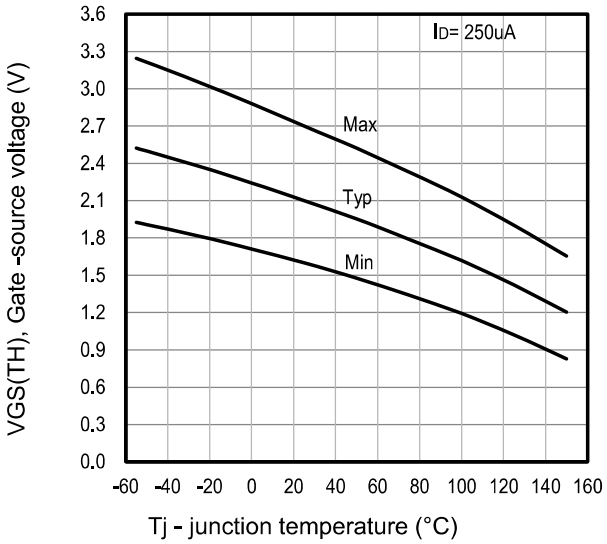


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

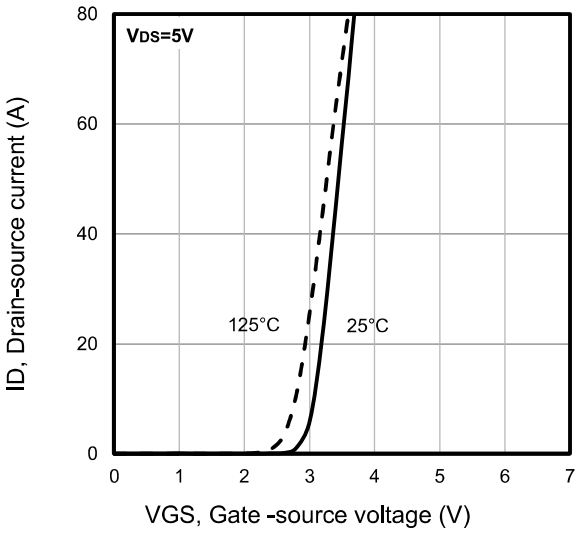


Fig3. Typical transfer characteristics

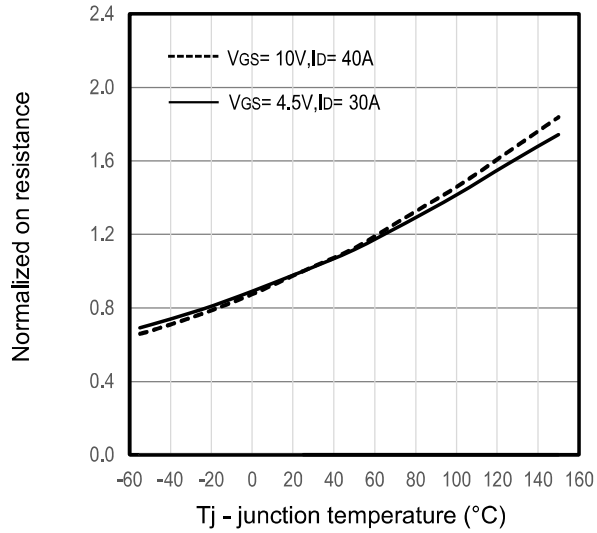


Fig4. Typical normalized on-resistance Vs. Tj

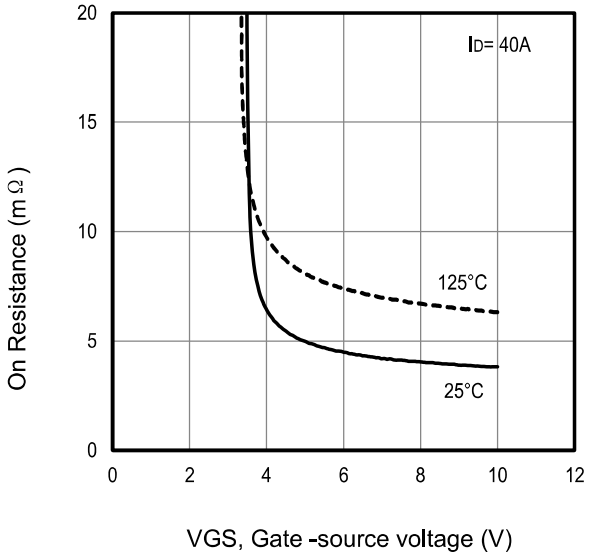


Fig5. Typical on resistance Vs gate -source voltage

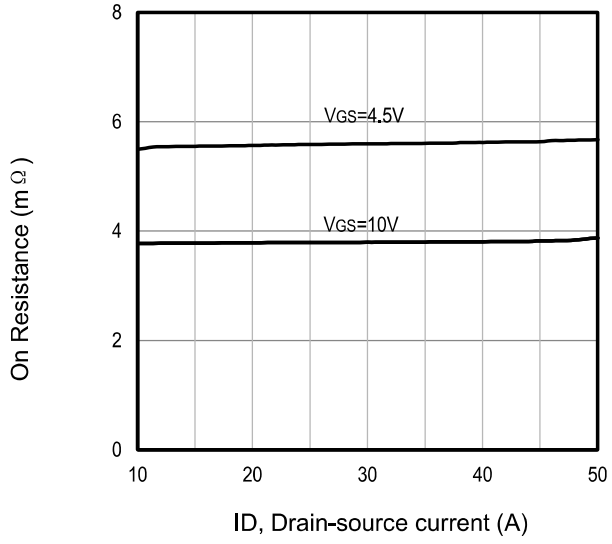


Fig6. Typical on resistance Vs drain current

Typical Characteristics

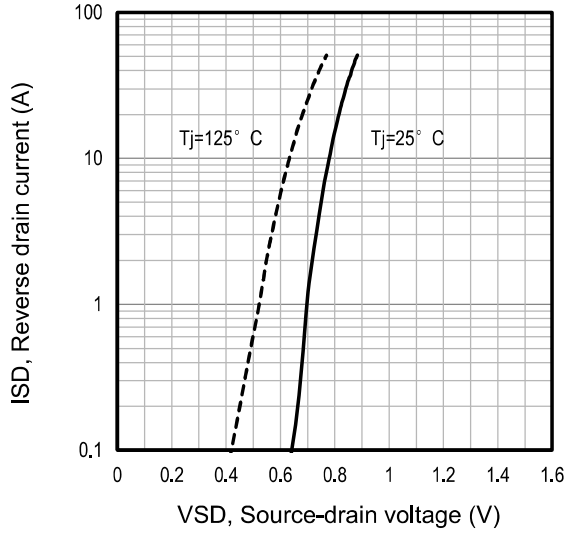


Fig7. Typical source-drain diode forward voltage

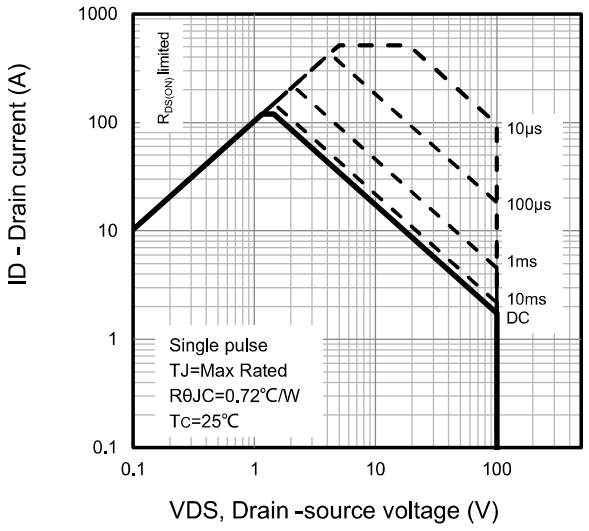


Fig8. Maximum safe operating area

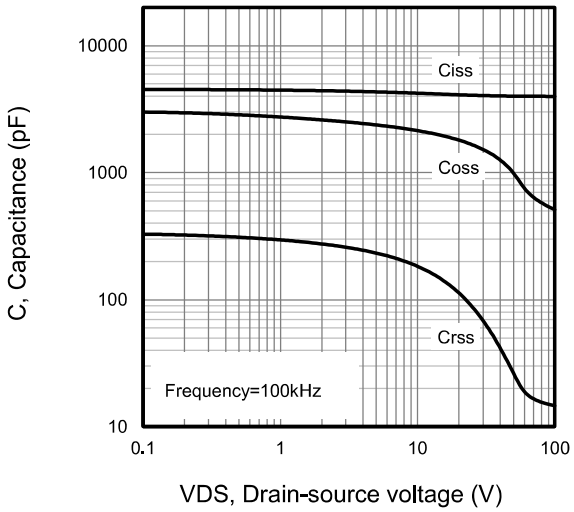


Fig9. Typical capacitance Vs. drain-source voltage

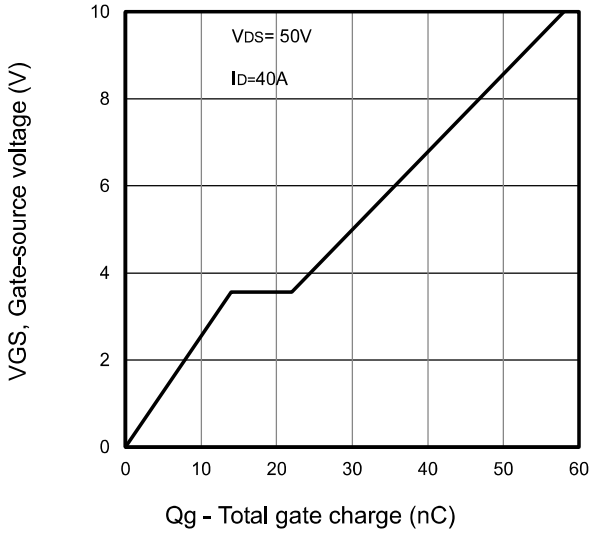


Fig10. Typical gate charge Vs. gate-source voltage

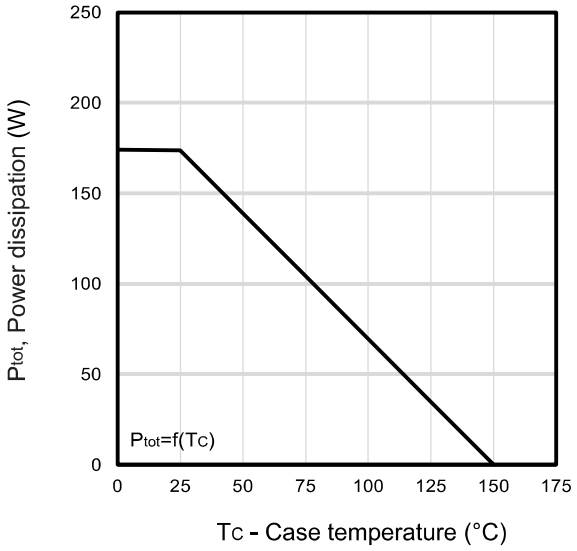


Fig11. Power dissipation Vs. case temperature

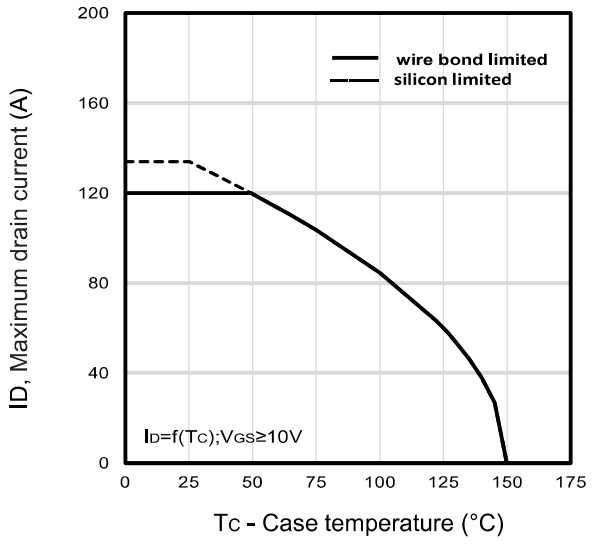


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

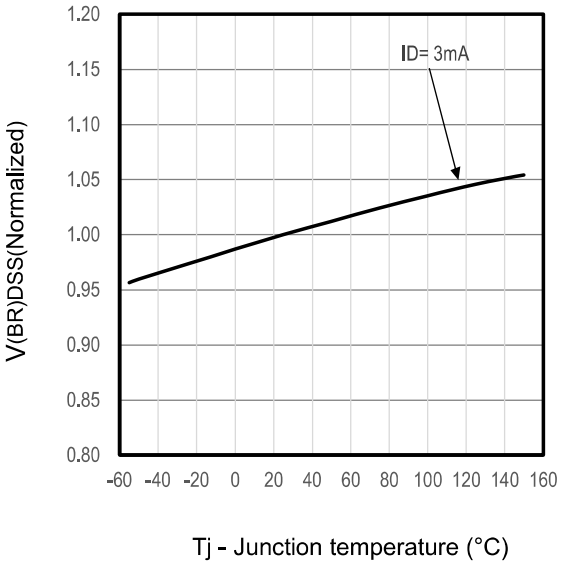


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

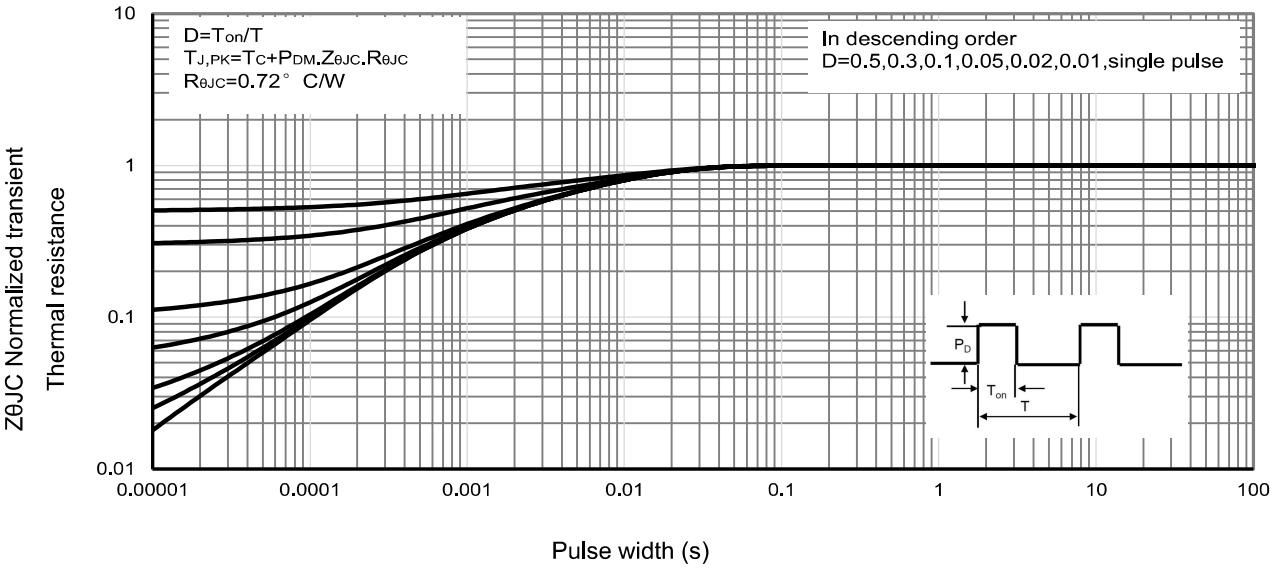


Fig14 . Normalized maximum transient thermal impedance

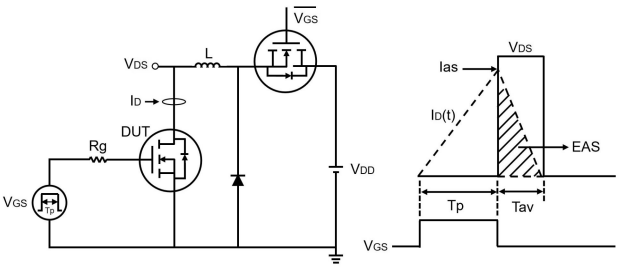


Fig15. Unclamped inductive test circuit and waveforms

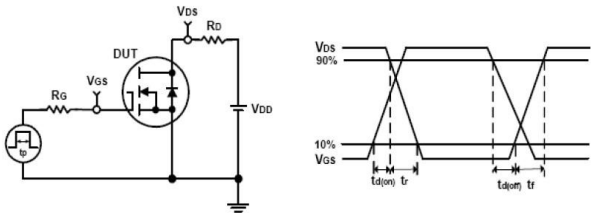
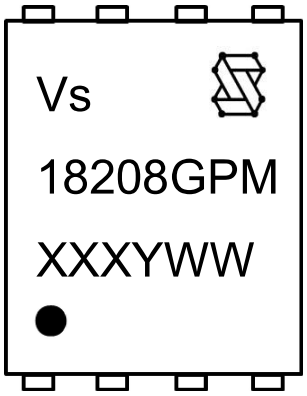


Fig16. Switching time test circuit and waveforms

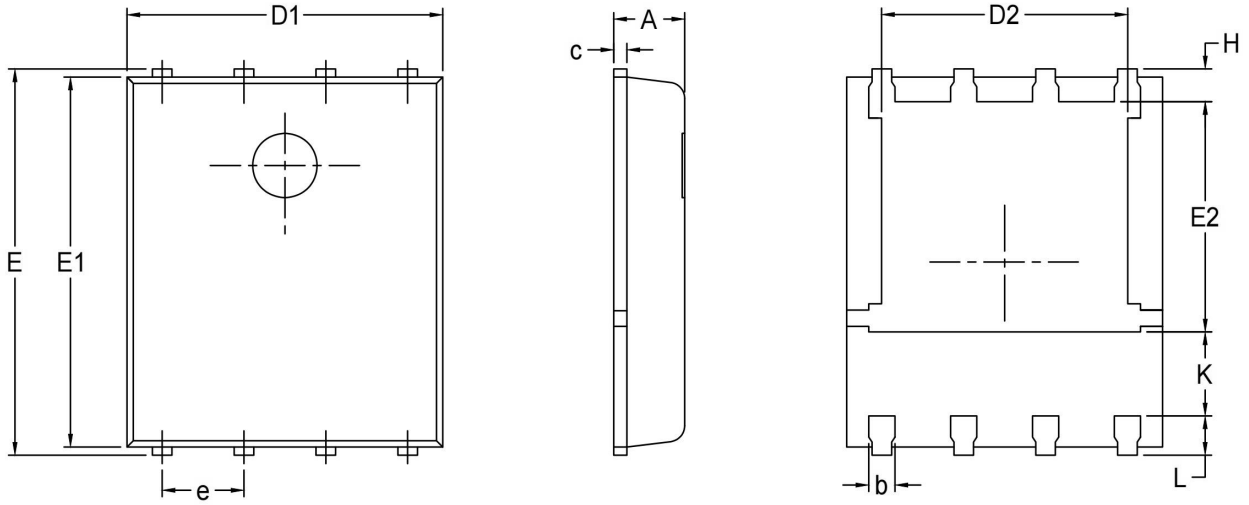
Marking Information



1st line: Vergiga code（Vs）， Vergiga logo
2nd line: Part Number（18208GPM）
3rd line: Date code （XXXYWW）
XXX: Wafer lot number code, code changed with lot number
Y: Year code，refer to table below
WW: Week code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71

Notes:

1.Refer to JEDEC MO-240 variation AA.

2.Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.

3.Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.