



Product Specification

- **MPE3008EH7AQ** -

(eMMC 5.1)

-Support HS400-

Document Number: E21003 (Version 1.5)

Revision History

[illegible]

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Product Overview

- Support JEDEC eMMC 5.1 compliant
- Compliant with eMMC Specification Ver. 4.3, 4.4, 4.41, 4.5, 4.51, 5.0, 5.1
- Bus mode
 - Clock frequency :0-200MHz
 - 12 wire bus (clock, command, 8-bit data bus, data strobe and hardware reset)
- Support three different data bus widths : 1-bit, 4-bit, 8-bit
 - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52MHz)
 - Single data rate : up to 200Mbyte/s @200MHz
 - Dual data rate : up to 400Mbyte/s @200MHz
- Operating voltage range:
 - $V_{CCQ} = 1.8V/3.3V$
 - $V_{CC} = 3.3V$
- Error free memory access
 - Internal error correction code (ECC) to protect data communication
- Security
 - Support secure erase/trim commands
- Support Replay Protected Memory Block (RPMB)
- Support Field Firmware Update(FFU)
- Support Lock/Unlock
- Support Data Protection for Power Failure
- Support Power Saving Sleep Mode
- Support Power Off Notification for Sleep
- Support High Priority Interrupt(HPI)
- Support Packed Commands
- Support Sampling Tuning Sequence
- Support Enhanced Strobe Mode
- Support Production State Awareness
- Temperature range (T_a)
 - Operation:
 - $-40^{\circ}C \sim 85^{\circ}C$
 - Storage:
 - $-40^{\circ}C \sim 85^{\circ}C$

Note1: the operation temperature is tentative

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1. Introduction

Metorage eMMC products follow the JEDEC eMMC 5.1 standard. It is an ideal universal storage solution for many electronic devices, including smartphones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. eMMC encloses the NAND and eMMC controller inside as one JEDEC standard package, providing a standard interface to the host. The eMMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

Table 1-1 Product Part Number

Product Part Number	NAND Density	Package	Operating voltage
MPE3008EH7AQ	8GB	BGA153	$V_{CC}=3.3V$ $V_{CCQ}=1.8V/3.3V$

2. Specification

2.1 System Performance

Table 2-1 Read/Write Performance

Products	Read Sequential (MB/s)	Write Sequential (MB/s)
MPE3008EH7AQ	Up to 246	Up to 145
Note 1: Values given for an 8-bit bus width, running HS400 mode from tool, $V_{CC}=3.3V$, $V_{CCQ}=1.8V$. Note 2: Performance numbers might be subject to changes without notice.		

2.2 Power Consumption

Table 2-2 Device Power Consumption

Products	Read(mA)		Write(mA)		Standby(uA)	
	$V_{CCQ}(1.8V)$	$V_{CC}(3.3V)$	$V_{CCQ}(1.8V)$	$V_{CC}(3.3V)$	V_{CCQ}	V_{CC}
MPE3008EH7AQ	127	63	69	64	85	19
Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, $V_{CC}=3.3V\pm5\%$, $V_{CCQ}=1.8V\pm5\%$ Note 2: The test data is tentative, current numbers might be subject to changes without notice						

2.3 Capacity according to partition

Table 2-3 Capacity according to partition

Capacity	Boot size	RPMB
8GB	4096 KB	4096 KB

2.4 User Density

Total user density depends on device type.

Table 2-4 User density

Device	User Density
8GB	7864320 KBytes

3. eMMC Device and System

3.1. eMMC System Overview

The eMMC specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

Metorage NAND Device consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

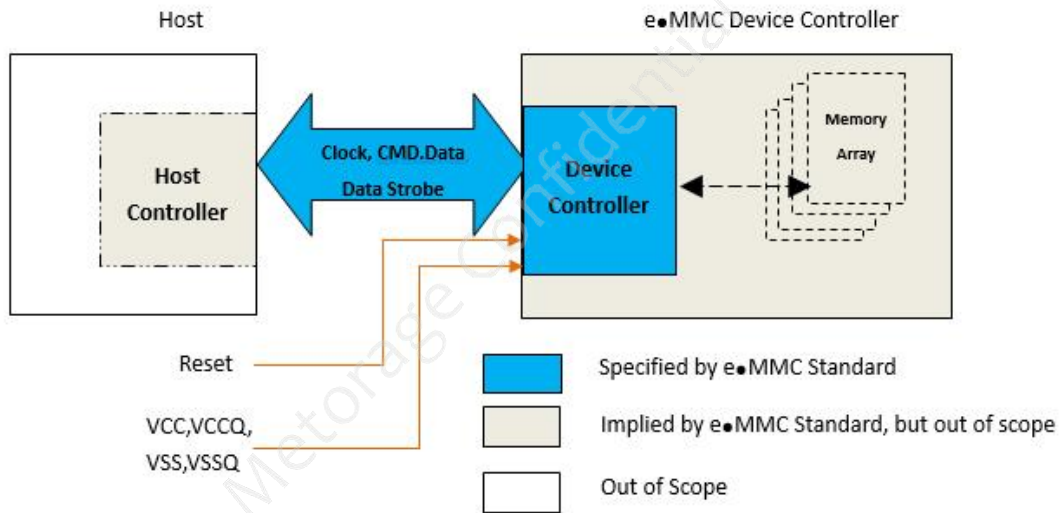


Figure 3-1 eMMC System Overview

3.2. Memory Addressing

Previous implementations of the eMMC specification are following byte addressing with 32 bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB.

To support larger densities the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode, use the host should read bit [30:29] in the OCR register.

3.3. eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

3.3.1 Clock(CLK)

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

3.3.2 Data Strobe(DS)

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

3.3.3 Command(CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

3.3.4 Input/Outputs(DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0- DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1- DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull-ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1-DAT7.

Table 3-1 Communication Interface

Name	Type ¹	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data strobe

Note1: I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

Table 3-2 eMMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.
- A reset signal
- By sending a special command

3.4. Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based eMMC bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B51.

3.5. Bus Speed Modes

eMMC defines several bus speed modes as shown in Table 3-3.

Table 3-3 Bus Speed Mode

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s
HS400	Dual	1.8V	8	0-200MHz	400MB/s

3.5.1 HS200 Bus Speed Mode

The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 4 or 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

3.5.2 HS200 System Block Diagram

Figure 3-2 shows a typical HS200 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of Host and Device. For reads, the Host needs to have an adjustable sampling point to reliably receive the incoming data.

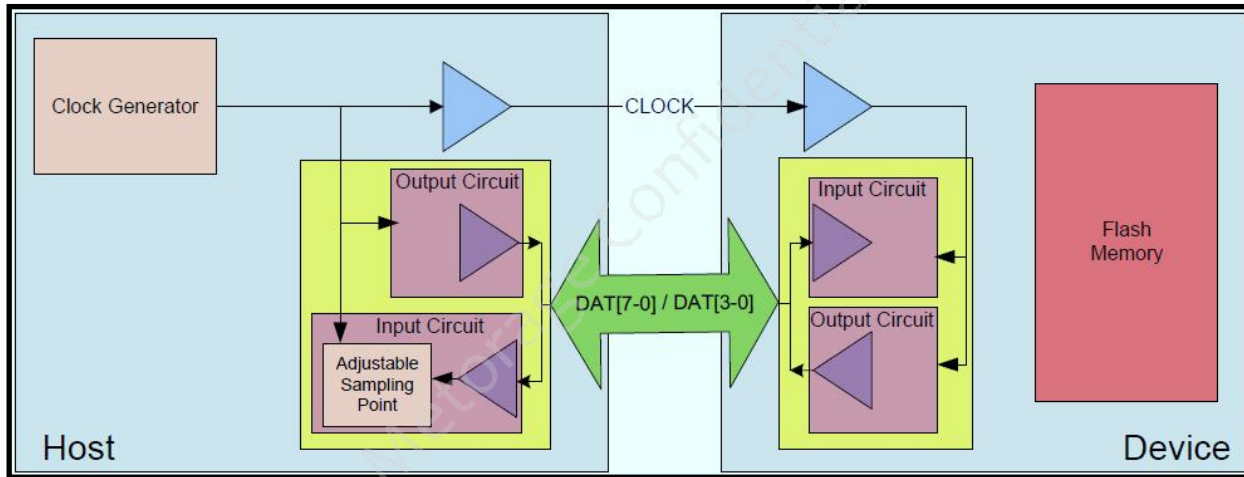


Figure 3-2 System Block Diagram

3.5.3 HS400 Bus Speed mode

The HS400 mode has the following features:

- DDR Data sampling method
- CLK frequency up to 200MHz, Data rate is – up to 400MB/s
- Only 8-bit bus width supported
- Signaling levels of 1.8V
- Support up to 5 selective Drive Strength
- Data strobe signal is toggled only for Data out and CRC response

3.5.4 HS400 System Block Diagram

Figure 3-3 shows a typical HS400 Host and Device system. The host has a clock generator, which supplies CLK to the Device. For read operations, Data Strobe is generated by device output circuit. Host receives the data which is aligned to the edge of Data Strobe.

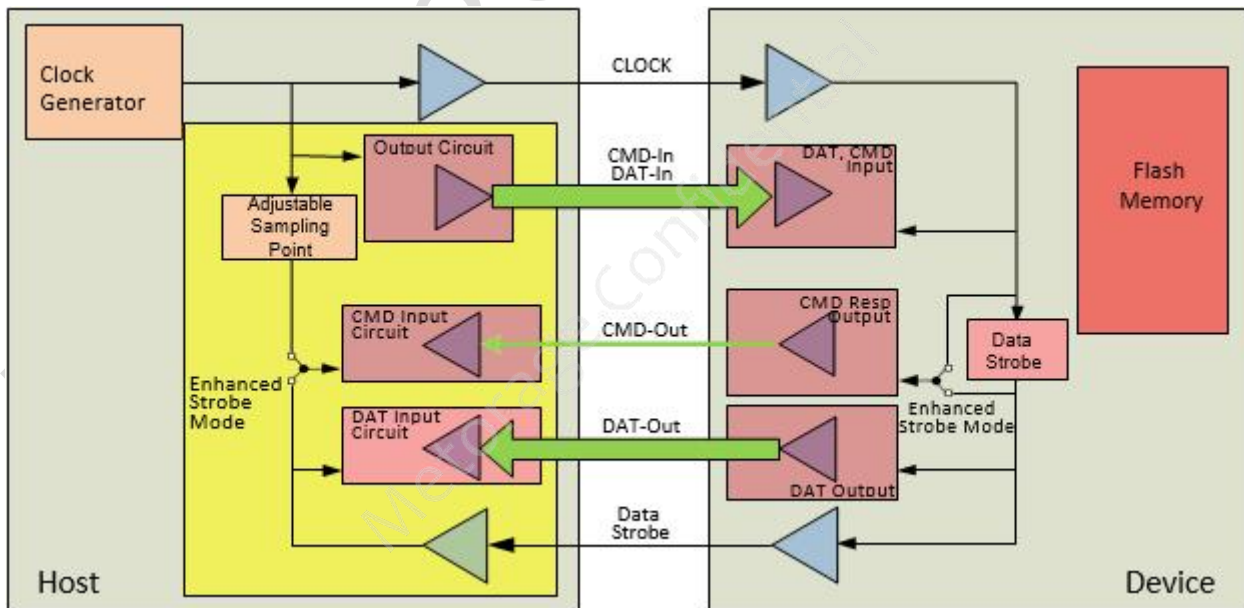


Figure 3-3 HS400 Host and Device block diagram

4. eMMC Functional Description

4.1. eMMC Overview

All communication between host and device are controlled by the host (main chip). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

Five operation modes are defined for the eMMC system:

- Boot operation mode
- Device identification mode
- Interrupt mode
- Data transfer mode
- Inactive mode

4.2. Boot Operation Mode

In boot operation mode, the master (eMMC host) can read boot data from the slave (eMMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFF, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B51.

4.3. Device Identification Mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative Device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B51.

4.4. Interrupt Mode

The interrupt mode on the eMMC system enables the master (eMMC host) to grant the transmission allowance to the slaves (Device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a Device request for service. Supporting eMMC interrupt mode is an option, both for the host and the Device. For more details, refer to section 6.5 of the JEDEC Standard Specification No.JESD84-B51.

4.5. Data Transfer Mode

When the Device is in *Stand-by State*, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B51.

4.6. Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to *Pre-idle* state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B51.

4.7. H/W Reset Operation

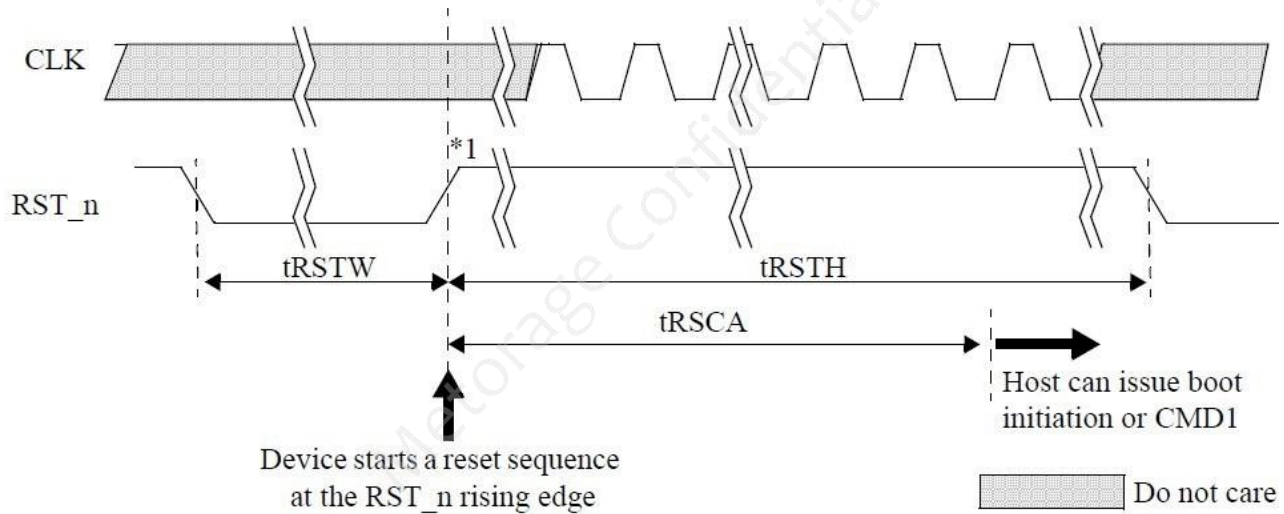


Figure 4-1 H/W Reset Waveform

Note1: Device will detect the rising edge of RST_n signal to trigger internal reset sequence

Table 4-1 H/W Reset Timing Parameters

Symbol	Comment	Min	Max	Unit
tRSTW	RST_n pulse width	1	-	[us]
tRSCA	RST_n to Command time	200 ¹	-	[us]
tRSTH	RST_n high period (interval time)	1	-	[us]

Note1: 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFA.

4.8. Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity

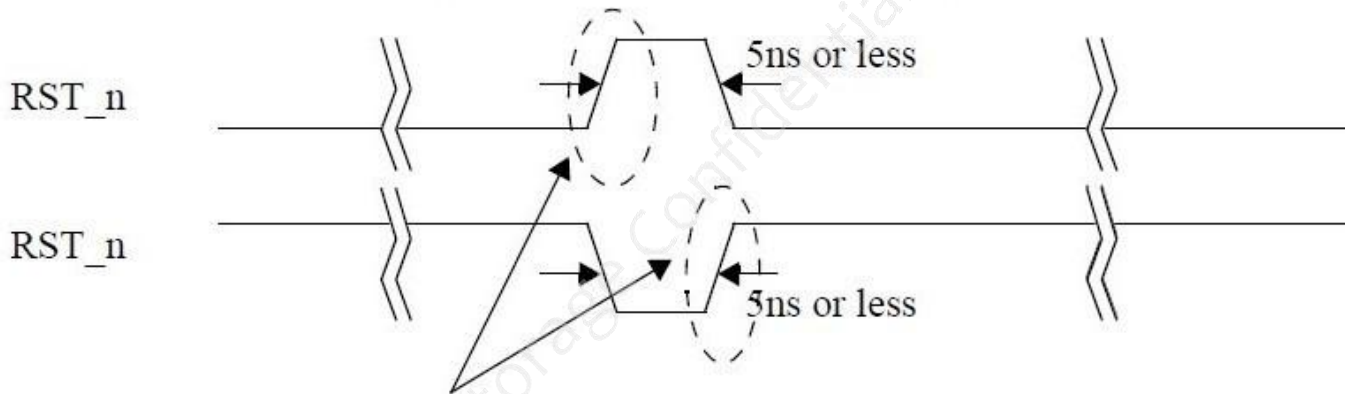


Figure 4-2 Noise Filtering Timing for H/W Reset

Device must not detect these rising edge.

Device must not detect 5ns or less of positive or negative RST_n pulse.

Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

4.9. Pseudo SLC Technology(for pSLC product only)

Pseudo SLC can be considered as an extended version of TLC. While TLC does Full Sequence Programming into 8 Vth distribution, pSLC only does Lower page programming into 2 Vth distribution. Accordingly, because only Lower pages are programmed, pSLC provides better performance and endurance than TLC. Moreover, pSLC performs similarly with SLC, yet pSLC is more cost-effective.

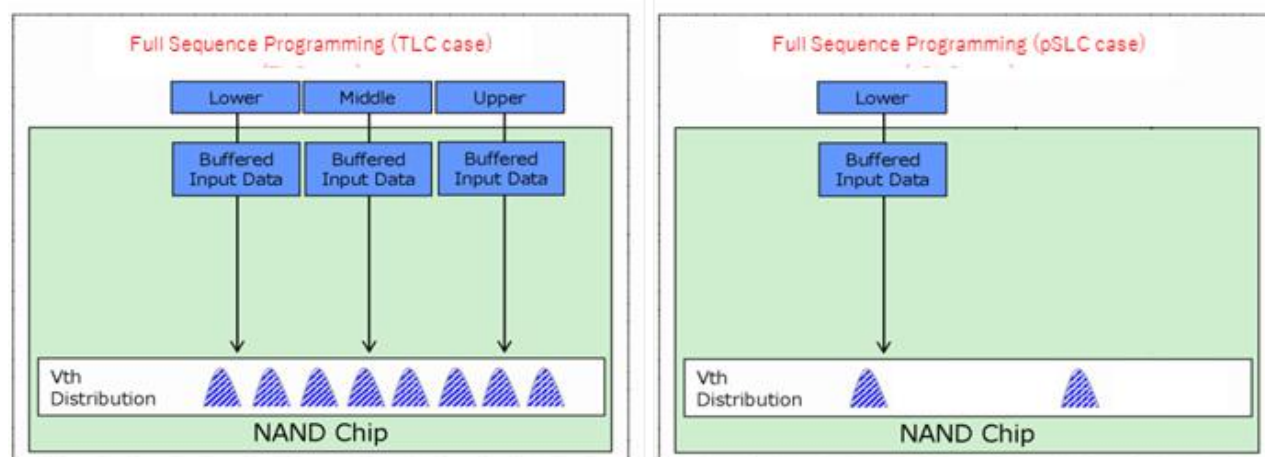


Figure 4- 3 Cell Content of TLC (Left) and Pseudo SLC (Right)

4.10. Field Firmware Update(FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the eMMC device and, following a successful download, instructs the eMMC device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the eMMC device supports FFU capabilities by reading SUPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the eMMC device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required). Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionality of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When host switched back to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

In case MODE_OPERATION_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW_Reset/Power cycle to install the new firmware. In such case the device doesn't need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED.

In both cases occurrence of a CMD0/HW_Reset/Power occurred before the host successfully downloaded the new firmware bundle to the device may cause the firmware download process to be aborted.

4.11. Power off Notification for sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER_OFF_LONG, POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power supplies or it may use to a power off notification (SLEEP_NOTIFICATION) if it intends to turn-off VCC after moving the device to Sleep state.

To indicate to the device that power off notification is supported by the host, a supporting host shall first set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To execute a power off, before powering the device down the host will change the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). Host should wait for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, host may safely power off the device.

The host may issue SLEEP_AWAKE (CMD5) to enter or to exit from Sleep state if POWER_OFF_NOTIFICATION byte is set to POWERED_ON. Before moving to Standby state and then to Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DATo line de-assertion. While in Sleep (slp) state VCC (Memory supply) may be turned off as defined in 4.1.6. Removing power supplies other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of Sleep (slp) state back to Transfer state using CMD5 and CMD7 and then execute a power off notification setting POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If host continues to send commands to the device after switching to the power off setting (POWER_OFF_LONG, POWER_OFF_SHORT or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON.

If host tries to change POWER_OFF_NOTIFICATION to 0x00 after writing another value there, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgent the host wants to turn power off. The device should respond to POWER_OFF_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used and the device shall respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to host shall:

- Keep the device power supplies alive (both V_{CC} and V_{CCQ}) and in their active mode
- Not power off the device intentionally before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT
- Not power off V_{CC} intentionally before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before moving the device to Sleep state

Before moving to Sleep state hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. Host should wait for the busy line to be de-asserted. Busy line may be asserted up the period defined in SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04 host may set the device into Sleep mode (CMD7+CMD5). After getting out from Sleep the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case POWER_OFF_NOTIFICATION byte will restore to POWERED_ON.

5. Register Settings

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

5.1. OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table 5-1 OCR Register fields

OCR Register Definitions OCR bit	VCCQ voltage window	Value
[31]	(Device power up status bit(busy) (Note1)	
[30:29]	Access Mode	00b(byte mode) 10b(sector mode)
[28:24]	Reserved	-
[23:15]	2.7-3.6V	11111111b
[14:8]	2.0-2.6V	0000000b
[7]	1.7-1.95V	1b
[6:0]	Reserved	-

Note 1: This bit is set to LOW if the Device has not finished the power up routine.

5.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol). For details, refer to JEDEC Standard Specification No.JESD84-B51

Table 5-2 CID Register fields

CID Fields Name	Field	Width	CID slice	Value
Manufacturer ID	MID	8	[127:120]	C4h
Reserved	-	6	[119:114]	-
Device/BGA	CBX	2	[113:112]	1h
OEM/Application ID	OID	8	[111:104]	FFh
Product name	PNM	48	[103:56]	4D45544F5241h
Product revision	PRV	8	[55:48]	-
Product serial number	PSN	32	[47:16]	Random by Production
Manufacturing data	MDT	8	[15:8]	month, year
CRC7 checksum	CRC	7	[7:1]	-
Not used, always "1"	-	1	[0]	1h

5.3. CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format... etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84- B51.

Table 5-3 CSD Register fields

Name	Field	Width	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	[127:126]	3h
System specification version	SPEC_VERS	4	[125:122]	4h
Reserved	-	2	[121:120]	-
Data read access-time 1	TAAC	8	[119:112]	2Fh
Data read access-time2 in CLK cycle(NSAC*100)	NSAC	8	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	[103:96]	2Ah
Device command classes	CCC	12	[95:84]	DF5h

Max. read data block length	READ_BL_LEN	4	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	[79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	[78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	[77]	0h
DSR implemented	DSR_IMP	1	[76]	0h
Reserved	-	2	[75:74]	-
Device size	C_SIZE	12	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	[61:59]	6h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	[58:56]	6h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	[55:53]	6h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	[52:50]	6h
Device size multiplier	C_SIZE_MULT	3	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	[36:32]	1Fh
Write protect group enable	WP_GRP_ENABLE	1	[31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0h
Write speed factor	R2W_FACTOR	3	[28:26]	1h
Max. write data block length	WRITE_BL_LEN	4	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21]	0h
Reserved	-	4	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	[16]	0h
File format group	FILE_FORMAT_GRP	1	[15]	0h
Copy flag (OTP)	COPY	1	[14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	[13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	[12]	0h
File format	FILE_FORMAT	2	[11:10]	0h
ECC code	ECC	2	[9:8]	0h
CRC	CRC	7	[7:1]	-
Not used, always '1'	-	1	[0:0]	1h

5.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No. JESD84-B51.

Table 5-4 Extended CSD Register fields

Name	Field	Size (Bytes)	CSD-slice	Value
Properties Segment				
Reserved	-	6	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	01h
HPI features	HPI_FEATURES	1	[503]	03h
Background operations support	BKOPS_SUPPORT	1	[502]	01h
Max packed read commands	MAX_PACKED_READS	1	[501]	3Fh
Max packed write Commands	MAX_PACKED_WRITES	1	[500]	3Fh

Data Tag Support	DATA_TAG_SUPPORT	1	[499]	01h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	01h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context management Capabilities	CONTEXT_CAPABILITIES	1	[496]	05h
Large Unit size	LARGE_UNIT_SIZE_M1	1	[495]	0h
Extended partitions attribute support	EXT_SUPPORT	1	[494]	03h
Supported modes	SUPPORTED_MODES	1	[493]	01h
FFU features	FFU_FEATURES	1	[492]	01h
Operation codes timeout	OPERATION_CODE_TIME_OUT	1	[491]	17h
FFU Argument	FFU_ARG	4	[490:487]	0h
Barrier support	BARRIER_SUPPORT	1	[486]	0h
Reserved	–	177	[485:309]	-
CMDQ support	CMDQ_SUPPORT	1	[308]	0h
CMDQ depth	CMDQ_DEPTH	1	[307]	0h
Reserved	–	1	[306]	–
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	[305:302]	0h
Vendor proprietary health Report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	[301:270]	0h
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	01h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	01h
Pre EOL information	PRE_EOL_INFO	1	[267]	01h
Optimal read size	OPTIMAL_READ_SIZE	1	[266]	08h
Optimal write size	OPTIMAL_WRITE_SIZE	1	[265]	08h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	[264]	08h
Device version	DEVICE_VERSION	2	[263:262]	0h
Firmware version	FIRMWARE_VERSION	8	[261:254]	-
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	[253]	0h
Cache size	CACHE_SIZE	4	[252:249]	100h
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	[248]	32h
Power off notification(long) Timeout	POWER_OFF_LONG_TIME	1	[247]	3Ch
Background operations Status	BKOPS_STATUS	1	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	[245:242]	0h
1st initialization time after Partitioning	INI_TIMEOUT_AP	1	[241]	1Eh
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	[240]	0h

Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	[239]	0h
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	[238]	0h
Power class for 200MHz at 3.6V	PWR_CL_200_195	1	[237]	0h
Power class for 200MHz at 1.95V	PWR_CL_200_130	1	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	[234]	0h
Reserved	–	1	[233]	–
TRIM Multiplier	TRIM_MULT	1	[232]	02h
Secure Feature support	SEC_FEATURE_SUPPORT	1	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	[230]	1Bh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	[229]	11h
Boot information	BOOT_INFO	1	[228]	07h
Reserved	–	1	[227]	–
Boot partition size	BOOT_SIZE_MULT	1	[226]	20h
Access size	ACC_SIZE	1	[225]	06h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	[224]	01h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	[223]	01h
Reliable write sector count	REL_WR_SEC_C	1	[222]	01h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	[221]	20h
Sleep current (VCC)	S_C_VCC	1	[220]	07h
Sleep current (VCCQ)	S_C_VCCQ	1	[219]	07h
Production state awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	[218]	17h
Sleep/awake timeout	S_A_TIMEOUT	1	[217]	17h
Sleep Notification timeout	SLEEP_NOTIFICATION_TIME	1	[216]	11h
Sector Count	SEC_COUNT	4	[215:212]	F00000h
Sector Write Protection Mode	SECURE_WP_INFO	1	[211]	0h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	[210]	0h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	[209]	0h

Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	[208]	0h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	[207]	0h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	[206]	0h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	[205]	0h
Reserved	–	1	[204]	–
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	[203]	0h
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	[202]	0h
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	[201]	0h
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	[199]	05h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	[198]	19h
I/O Driver Strength	DRIVER_STRENGTH	1	[197]	0Fh
Device type	DEVICE_TYPE	1	[196]	57h
Reserved	–	1	[195]	–
CSD structure version	CSD_STRUCTURE	1	[194]	02h
Reserved	–	1	[193]	–
Extended CSD revision	EXT_CSD_REV	1	[192]	08h
Modes Segment				
Command set	CMD_SET	1	[191]	0h
Reserved	–	1	[190]	–
Command set revision	CMD_SET_REV	1	[189]	0h
Reserved	–	1	[188]	–
Power class	POWER_CLASS	1	[187]	0h
Reserved	–	1	[186]	–
High-speed interface timing	HS_TIMING	1	[185]	0h
Strobe support	STROBE_SUPPORT	1	[184]	01h
Bus width mode	BUS_WIDTH	1	[183]	0h
Reserved	–	1	[182]	–
Erased memory content	ERASED_MEM_CONT	1	[181]	0h
Reserved	–	1	[180]	–
Partition configuration	PARTITION_CONFIG	1	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	[178]	0h

Boot bus Conditions	BOOT_BUS_CONDITIONS	1	[177]	0h
Reserved	–	1	[176]	–
High-density erase group Definition	ERASE_GROUP_DEF	1	[175]	0h
Boot write protection status Registers	BOOT_WP_STATUS	1	[174]	0h
Boot area write protection Register	BOOT_WP	1	[173]	0h
Reserved	–	1	[172]	–
User area write protection Register	USER_WP	1	[171]	0h
Reserved	–	1	[170]	–
FW configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	[168]	20h
Write reliability setting Register	WR_REL_SET	1	[167]	0h
Write reliability parameter Register	WR_REL_PARAM	1	[166]	14h
Start Sanitize operation	SANITIZE_START	1	[165]	0h
Manually start background Operations	BKOPS_START	1	[164]	0h
Enable background operations handshake	BKOPS_EN	1	[163]	0h
H/W reset function	RST_n_FUNCTION	1	[162]	0h
HPI management	HPI_MGMT	1	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	[160]	07h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	[159:157]	1E0h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	[156]	0h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT 4	3	[154:152]	0h
General Purpose Partition Size	GP_SIZE_MULT3	3	[151:149]	0h
General Purpose Partition Size	GP_SIZE_MULT2	3	[148:146]	0h
General Purpose Partition Size	GP_SIZE_MULT1	3	[145:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	[139:136]	0h
Reserved	–	1	[135]	–
Bad Block Management Mode	SEC_BAD_BLK_MGMNT	1	[134]	0h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT	1	[132]	0h

Periodic Wake-up	PERIODIC_WAKEUP	1	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	[130]	01h
Reserved	–	2	[129:128]	–
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	[127:64]	0h
Native sector size	NATIVE_SECTOR_SIZE	1	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTRL	2	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATU	2	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	[53:52]	0h
Context configuration	CONTEXT_CONF	15	[51:37]	-
Packed command status	PACKED_COMMAND_STATUS	1	[36]	0h
Packed command failure	PACKED_FAILURE_INDEX	1	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	[32]	0h
Reserved	–	1	[31]	–
Mode config	MODE_CONFIG	1	[30:30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	[29:29]	0h
Reserved	–	2	[28:27]	–
FFU status	FFU_STATUS	1	[26:26]	0h
Per loading data size	PRE_LOADING_DATA_SIZE	4	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	[21:18]	F00000h
Product state awareness Enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	[17:17]	03h
Secure removal type	SECURE_REMOVAL_TYPE	1	[16:16]	09h
Command Queue Mode Enable	CMDQ_MODE_EN	1	[15:15]	0h
Reserved	–	15	[14:0]	–

5.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the Stand-by State with CMD7.

5.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 7.6 of the JEDEC Standard Specification No. JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage.

6. The eMMC bus

The eMMC bus has ten communication lines and three supply lines:

- **CMD:** Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- **DAT0-7:** Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- **CLK:** Clock is a host to Device signal. CLK operates in push-pull mode
- **Data Strobe:** Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

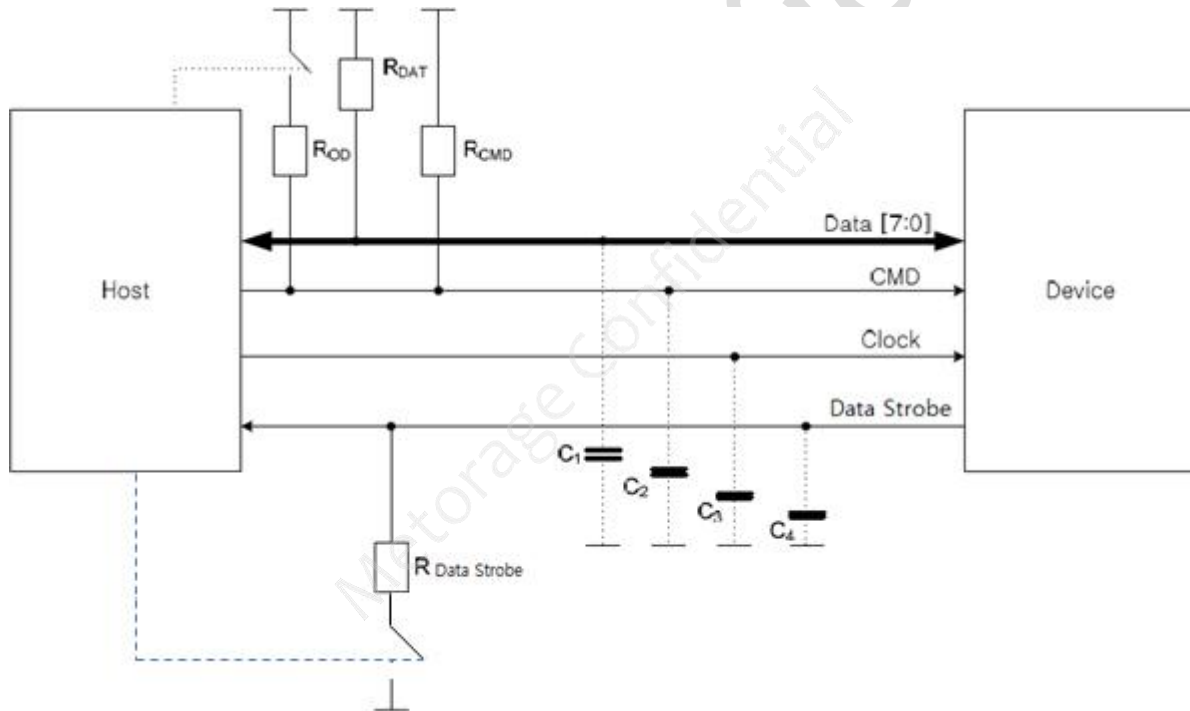


Figure 6-1 Bus Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD} . R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used). Consequently the maximum operating frequency in the open drain mode has to be reduced if the used R_{CMD} value is higher than the minimal one given in.

$R_{DataStrobe}$ is pull-down resistor used in HS400 device.

6.1 Power-up

6.1.1 eMMC power-up

An eMMC bus power-up is handled locally in each device and in the bus master. Figure 7 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No. JESD84-B51 for specific instructions regarding the power-up sequence.

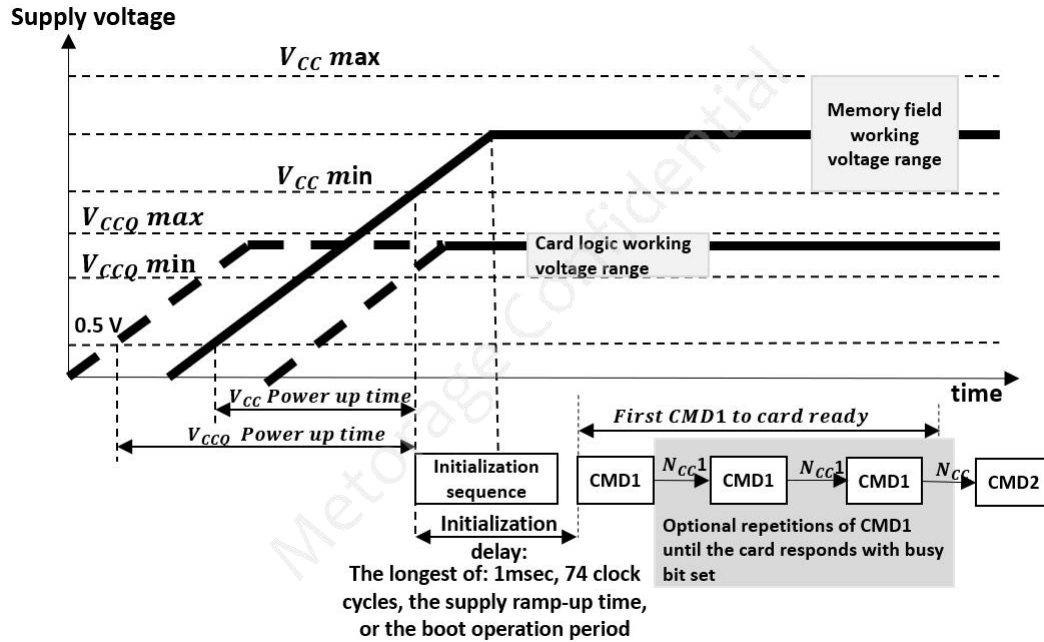


Figure 6-2 eMMC Power-up Diagram

6.1.2 eMMC Power Cycling

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No. JESD84-B51.

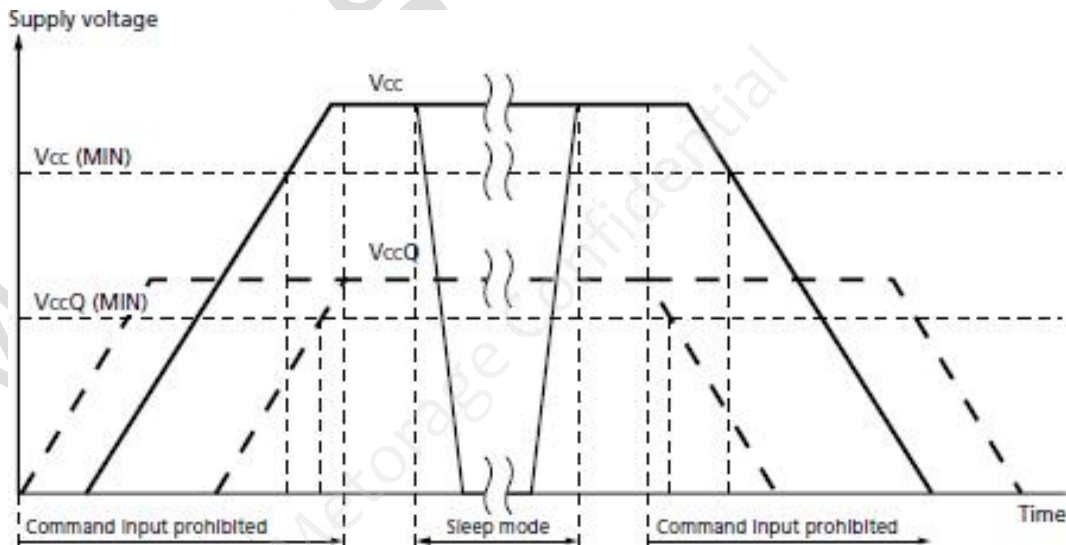


Figure 6-3 The eMMC Power Cycle

6.2 Bus Operating Condition

Table 6-1 General Operating Conditions

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines	-	-0.5	$V_{CCQ} + 0.5$	V	-
All Inputs					
Input Leakage Current (before initialization sequence ¹ and/or the internal pull up resistors connected)	-	-100	100	μA	-
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)	-	-2	2	μA	-
All Outputs					
Output Leakage Current (before initialization sequence)	-	-100	100	μA	-
Output Leakage Current (after initialization sequence) ²	-	-2	2	μA	-
Note1: Initialization sequence is defined in section 10.1 of the JEDEC Standard Specification No. JESD84-B51.					
Note2: DS (Data strobe) pin is excluded.					

6.2.1 Power supply: eMMC

In the eMMC, V_{CC} is used for the NAND flash device and its interface voltage; V_{CCQ} is for the controller and the MMC interface voltage as shown in Figure 9. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ} . A C_{Reg} capacitor must be connected to the V_{DDi} terminal to stabilize regulator output on the system.

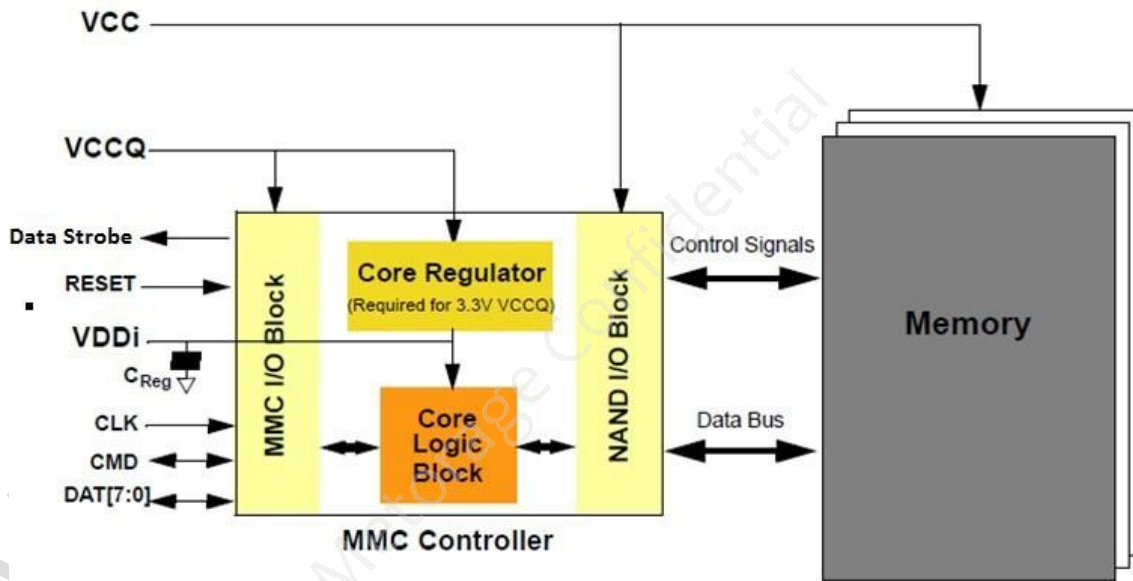


Figure 6-4 eMMC Internal Power Diagram

6.2.2 eMMC Power Supply Voltage

The eMMC supports one or more combinations of V_{CC} and V_{CCQ} as shown in Table 9. The V_{CCQ} must be defined at equal to or less than V_{CC} .

Table 6-2 eMMC Operating Voltage

Parameter	Symbol	Min	Max	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.6	V
Supply voltage (I/O)	V_{CCQ}	1.7	1.95	V
		2.7	3.6	V
Supply power-up for 3.3V	t_{PRUH}	-	35	ms
Supply power-up for 1.8V	t_{PRUL}	-	25	ms

The eMMC must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table).

Table 6-3 eMMC Voltage Combinations

		V_{CCQ}	
		1.7V–1.95V	2.7V–3.6V ¹
V_{CC}	2.7V–3.6V	Valid	Valid

Note1: V_{CCQ} (I/O) 3.3 volt range is not supported in HS200 /HS400 devices.

6.2.3 Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST} , the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances must be under 20pF.

Table 6-4 Signal Line Load

Parameter	Symbol	Min	Max	Typ	Unit
Pull-up resistance for CMD	R_{CMD}	4.7	50	10	Kohm
Pull-up resistance for DAT0~7	R_{DAT}	10	50	10	Kohm
Pull-up resistance for RST_n	R_{RST_n-n}	4.7	50	10	Kohm
Bus signal line capacitance	C_L	-	30	30	pF
Single Device capacitance	C_{BGA}	-	6	6	pF
Maximum signal line inductance	-	-	16	16	nH
Impedance on CLK / CMD / DAT0 ~ 7	-	45	55	50	ohm
Serial's resistance on CLK line	SR_{CLK}	0	47	0	ohm
Serial's resistance on CMD / DAT0 ~ 7 line	SR_{CMD} $SR_{DAT0\sim7}$	0	47	0	ohm
V_{CCQ} decoupling capacitor	-	2.2+0.1	10+0.22	2.2+0.1	μF
	CH1	1	2.2	1	
V_{CC} capacitor value	-	2.2+0.1	10+0.22	4.7+0.1	μF
V_{DDI} capacitor value	-	1+0.1	2.2+0.1	1+0.1	μF

6.2.4 HS400 reference load

The circuit in Figure 10 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.

The reference load is made up by the transmission line and the $C_{\text{REFERENCE}}$ capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.

Delay time (t_d) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

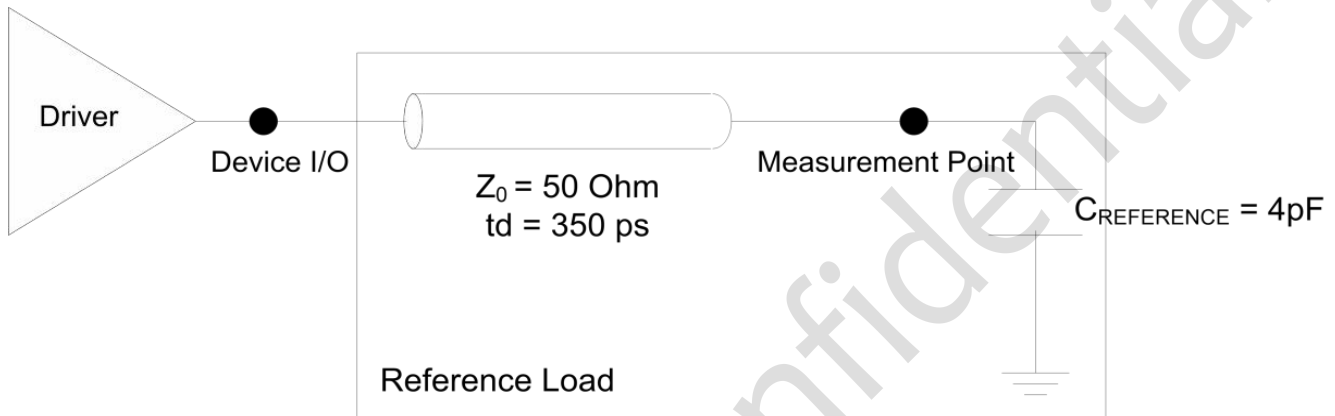


Figure 6-5 HS400 reference load

6.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

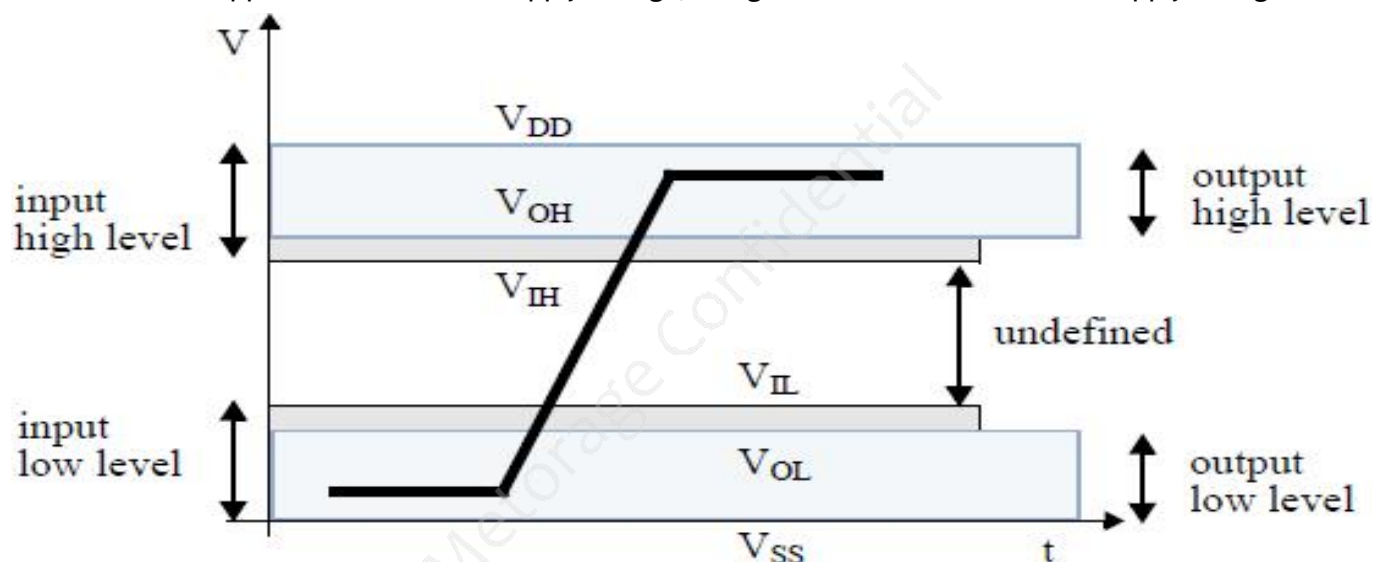


Figure 6-6 Bus Signal Levels

6.3.1 Open-drain Mode Bus Signal Level

Table 6-5 Open-drain Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	VOH	$V_{DD} - 0.2$	-	V	$I_{OH} = -100 \mu A$
Output LOW voltage	VOL	-	0.3	V	$I_{OL} = 2 \text{ mA}$

The input levels are identical with the push-pull mode bus signal levels.

6.3.2 Push-pull mode bus signal level — eMMC

The device input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range

For 1.70V – 1.95V V_{CCQ} range (Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.)

Table 6-6 Push-pull Signal Level—1.70 -1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	VOH	$V_{CCQ} - 0.45V$	-	V	$I_{OH} = -2mA$
Output LOW voltage	VOL	-	0.45V	V	$I_{OL} = 2mA$
Input HIGH voltage	VIH	$0.65 \cdot V_{CCQ}$	$V_{CCQ} + 0.3$	V	-
Input LOW voltage	VIL	$V_{SS} - 0.3$	$0.35 \cdot V_{DD}$	V	-

Note1: $0.7 \cdot V_{DD}$ for MMC™4.3 and older revisions.

Note2: $0.3 \cdot V_{DD}$ for MMC™4.3 and older revisions.

For 2.7V-3.6V V_{CCQ} range (compatible with JESD8C.01)

Table 6-7 Push-pull Signal Level—High-voltage eMMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	VOH	$0.75 * V_{CCQ}$	-	V	$I_{OH} = -100 \mu A @ V_{CCQ} \text{ min}$
Output LOW voltage	VOL	-	$0.125 * V_{CCQ}$	V	$I_{OL} = 100 \mu A @ V_{CCQ} \text{ min}$
Input HIGH voltage	VIH	$0.625 * V_{CCQ}$	$V_{CCQ} + 0.3$	V	-
Input LOW voltage	VIL	$V_{SS} - 0.3$	$0.25 * V_{CCQ}$	V	-

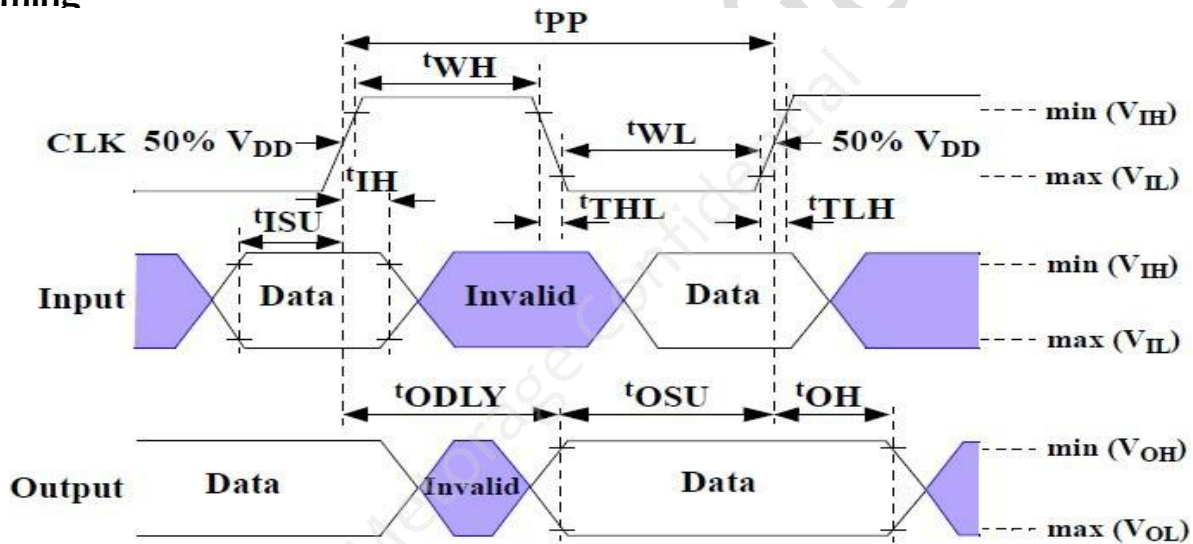
6.3.3 Bus Operating Conditions for HS200 & HS400

The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84- B51 through 10.5.2 of JESD84-B51.

6.3.4 Device Output Driver Requirements for HS200 & HS400

Refer to section 10.5.4 of the JEDEC Standard Specification No.JESD84-B51.

6.4 Bus Timing



Data must always be sampled on the rising edge of the clock.

Figure 6-7 Timing Diagram

6.4.1 Device Interface Timings

Table 6-8 High-speed Device Interface Timing

Parameter	Symbol	Min	Max	Unit
Clock CLK ¹				
Clock frequency Data Transfer Mode(PP) ²	fPP	0	52 ³	MHz
Clock frequency Identification Mode(OD)	fOD	0	400	kHz
Clock high time	tWH	6.5	-	ns
Clock low time	tWL	6.5	-	ns
Clock rise time ⁴	tTLH	-	3	ns
Clock fall time	tTHL	-	3	ns

Inputs CMD, DAT (referenced to CLK)				
Input set-up time	tISU	3	-	ns
Input hold time	tIH	3	-	ns
Outputs CMD, DAT (referenced to CLK)				
Output delay time during data transfer	tODLY	-	13.7	ns
Output hold time	tOH	2.5	-	ns
Signal rise time ⁵	tRISE	-	3	ns

Note1: CLK timing is measured at 50% of VDD.
 Note2: eMMC shall support the full frequency range from 0-26Mhz or 0-52MHz.
 Note3: Device can operate as high-speed Device interface timing at 26 MHz clock frequency. Note4: CLK rise and fall times are measured by min (VIH) and max (VIL).
 Note5: Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 6-9 Backward-compatible Device Interface Timing

Parameter	Symbol	Min	Max	Unit
Clock CLK ²				
Clock frequency Data Transfer Mode (PP) ³	fPP	0	26	MHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz
Clock high time	tWH	10	-	-
Clock low time	tWL	10	-	ns
Clock rise time ⁴	tTLH	-	10	ns
Clock fall time	tTHL	-	10	ns
Inputs CMD, DAT (referenced to CLK)				
Input set-up time	tISU	3	-	ns
Input hold time	tIH	3	-	ns
Outputs CMD, DAT (referenced to CLK)				
Output set-up time ⁵	tOSU	11.7	-	ns
Output hold time ⁵	tOH	8.3	-	ns

Note1: The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
 Note2: CLK timing is measured at 50% of VDD.
 Note3: For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
 Note4: CLK rise and fall times are measured by min (VIH) and max (VIL).
 Note5: tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

6.5 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.5 of the JEDEC Standard Specification No. JESD84-B51, therefore there is no timing change for the CMD signal.

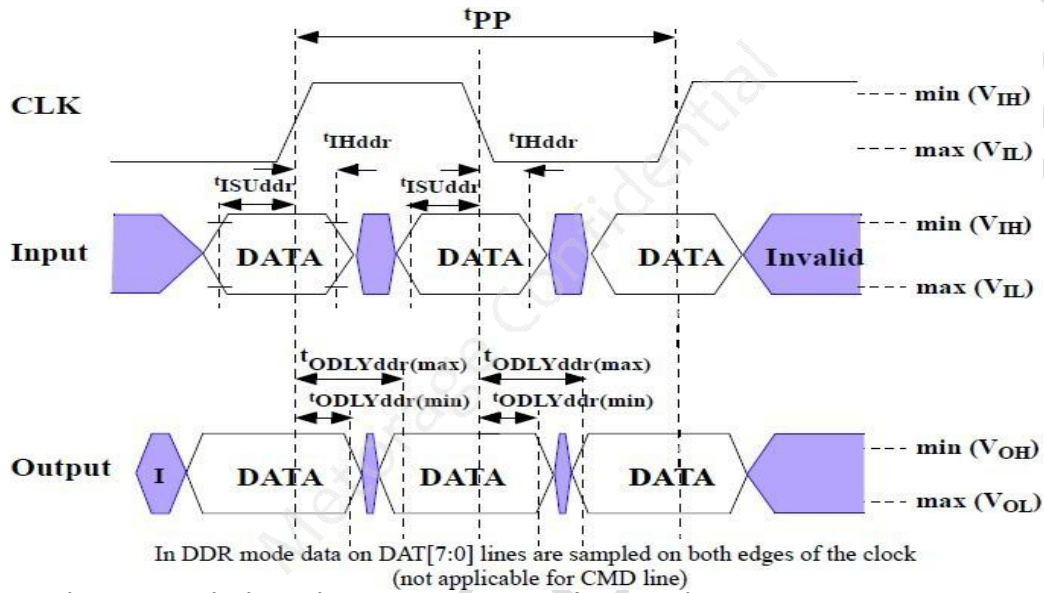


Figure 6-8 Timing Diagram: Data Input/Output in Dual Data Rate Mode

6.5.1 Dual Data Rate Interface Timings

Table 6-10 High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max	Unit
Input CLK ¹				
Clock duty cycle	-	45	55	%
Input DAT (referenced to CLK-DDR mode)				
Input set-up time	tISUddr	2.5	-	ns
Input hold time	tIHddr	2.5	-	ns
Output DAT (referenced to CLK-DDR mode)				
Output delay time during data transfer	tODLYd dr	1.5	7	ns
Signal rise time (all signals) ²	tRISE	-	2	ns
Signal fall time (all signals)	tFALL	-	2	ns
Note1: CLK timing is measured at 50% of VDD.				
Note2: Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).				

6.6 Bus Timing Specification in HS200 Mode

6.6.1 HS200 Clock Timing

Host CLK Timing in HS200 mode shall conform to the timing specified in Figure and Table 18. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device.

The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

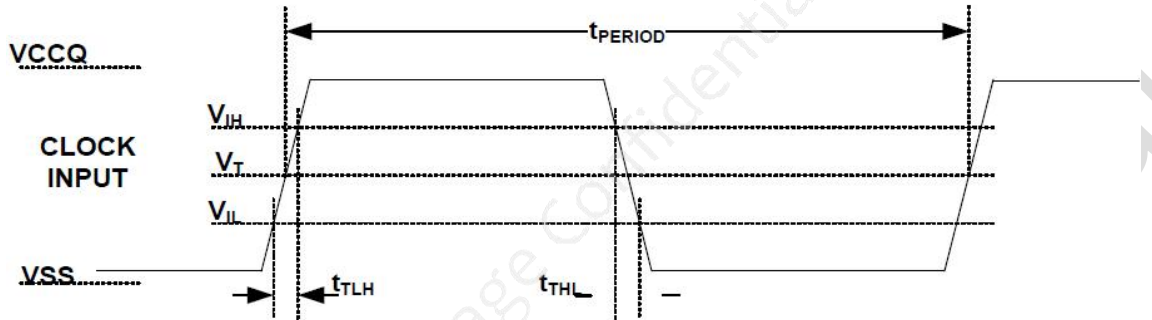


Figure 6-9 HS200 Clock Signal Timing

Note1: V_{IH} denote $V_{IH(min.)}$ and V_{IL} denotes $V_{IL(max.)}$.
Note2: $V_T = 50\%$ of V_{CCQ} , indicates clock reference point for timing measurements.

Table 6-11 HS200 Clock Signal Timing

Symbol	Min	Max	Unit
t_{PERIOD}	5	-	ns
t_{TLH}, t_{THL}	-	$0.2 * t_{PERIOD}$	ns
Duty Cycle	30	70	%

6.6.2 HS200 Device Input Timing

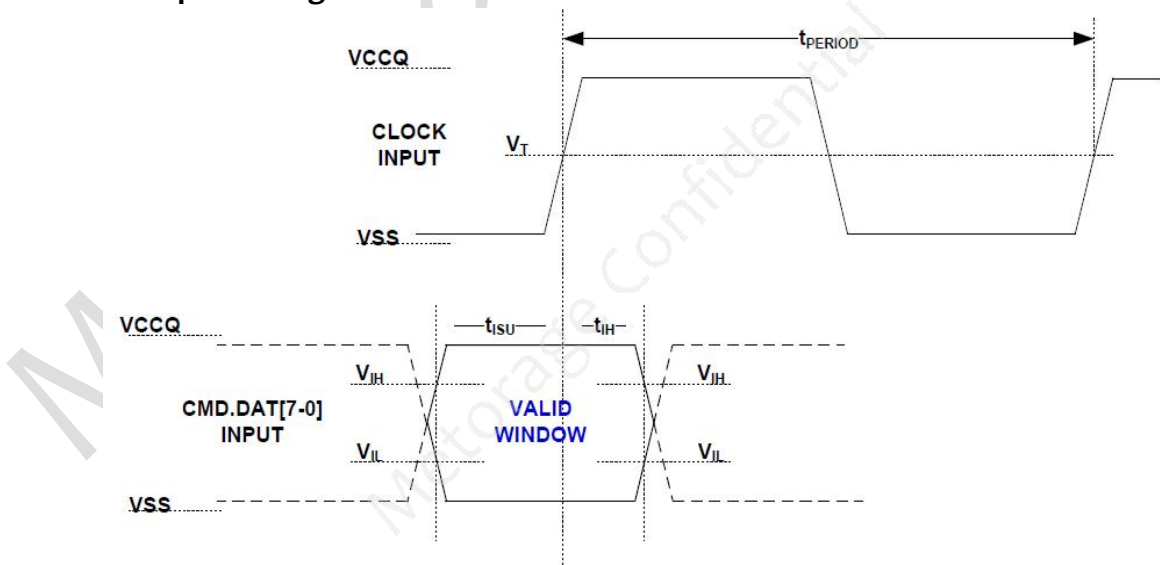


Figure 6-10 HS200 Device Input Timing

Note1: t_{ISU} and t_{IH} are measured at $V_{IL(max.)}$ and $V_{IH(min.)}$.
Note2: V_{IH} denote $V_{IH(min.)}$ and V_{IL} denotes $V_{IL(max.)}$.

Table 6-12 HS200 Device Input Timing

Symbol	Min	Max	Unit
t_{ISU}	1.4	-	ns
t_{IH}	0.8	-	ns

6.6.3 HS200 Device Output Timing

t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD} . After initialization, the t_{PH} may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

Figure 16 and Table 20 define Device output timing.

While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔT_{PH} . Output valid data window (t_{VW}) is available regardless of the drift (ΔT_{PH}) but position of data window varies by the drift, as described in Figure 17.

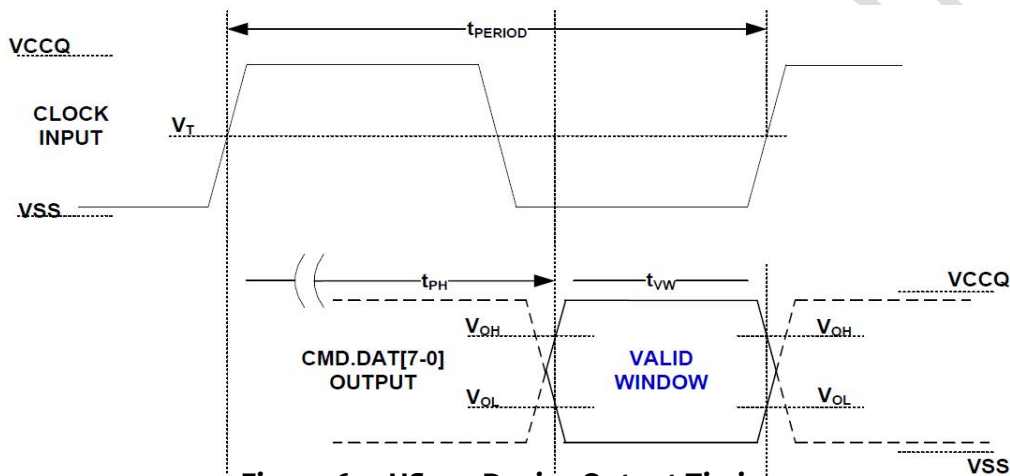


Figure 6-11 HS200 Device Output Timing

Note: V_{OH} denotes $V_{OH}(\min.)$ and V_{OL} denotes $V_{OL}(\max.)$.

Table 6-13 Output Timing

Symbol	Min	Max	Unit
t_{PH}	0	2	UI
ΔT_{PH}	-350 ($\Delta T = -20^{\circ}C$)	+1550 ($\Delta T = 90^{\circ}C$)	ps
T_{VW}	0.575	-	UI

Note : Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

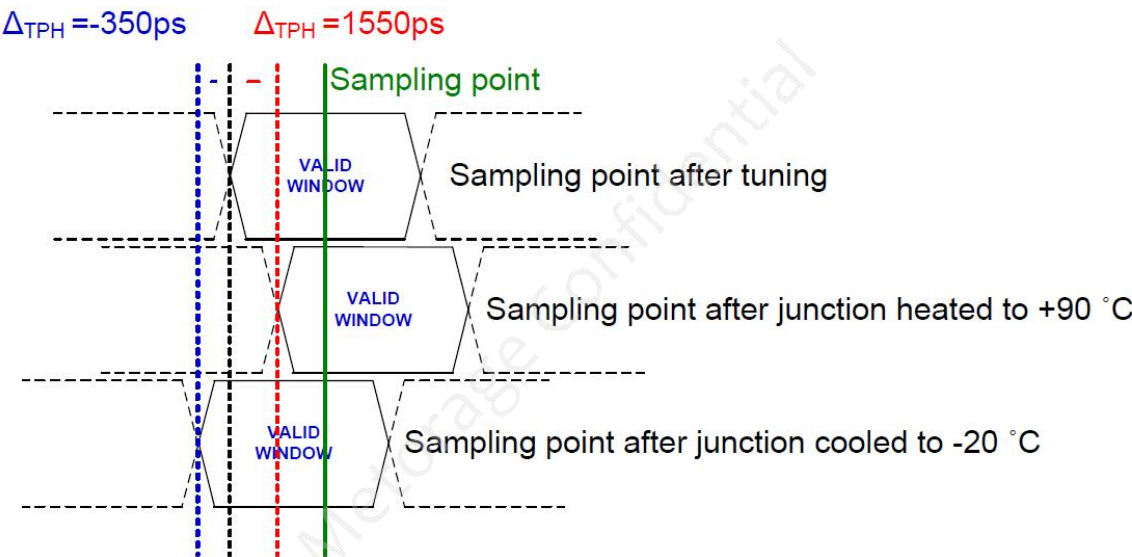


Figure 6-12 ΔT_{PH} consideration

Implementation Guide: Host should design to avoid sampling errors that may be caused by the ΔT_{PH} drift. It is recommended to perform tuning procedure while Device wakes up, after sleep. One simple way to overcome the ΔT_{PH} drift is by reduction of operating frequency.

6.7 Bus Timing Specification in HS400 mode

6.7.1 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode. Figure 18 and Table 21 show Device input timing.

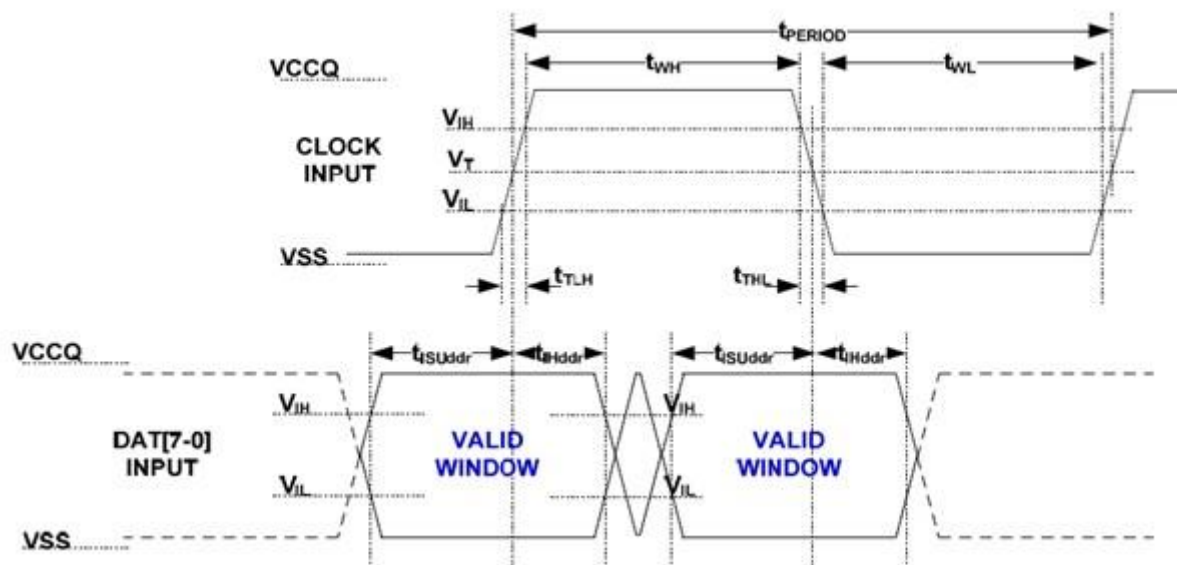


Figure 6-13 HS400 Device Data input timing

Note1: t_{SU} and t_{IH} are measured at $V_{IL}(\max.)$ and $V_{IH}(\min.)$.

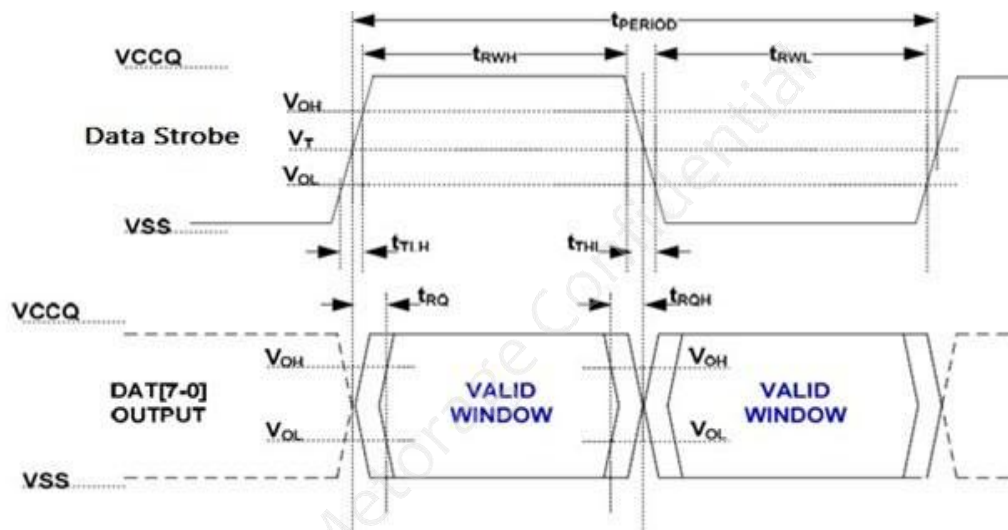
Note2: V_{IH} denote $V_{IH}(\min.)$ and V_{IL} denotes $V_{IL}(\max.)$.

Table 6-14 HS400 Device input timing

Parameter	Symbol	Min	Max	Unit
Input CLK				
Cycle time data transfer mode	t_{PERIOD}	5	-	-
Slew rate	SR	1.125	-	V/ns
Duty cycle distortion	t_{CKDCD}	0	0.3	ns
Minimum pulse width	t_{CKMPW}	2.2	-	ns
Input DAT (referenced to CLK)				
Input set-up time	t_{ISUddr}	0.4	-	ns
Input hold time	t_{IHddr}	0.4	-	ns
Slew rate	SR	1.125	-	V/ns

6.7.2 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



Note: V_{OH} denotes $V_{OH}(\min.)$ and V_{OL} denotes $V_{OL}(\max.)$.

Figure 6-14 HS400 Device output timing

Note: $V_T = 50\%$ of V_{CCQ} , indicates clock reference point for timing measurements.

Table 6-15 HS400 Device Output timing

Parameter	Symbol	Min	Max	Unit
Data Strobe				
Cycle time data transfer mode	t_{PERIOD}	5	-	-
Slew rate	SR	1.125	-	V/ns
Duty cycle distortion	t_{DSDCD}	0	0.2	ns
Minimum pulse width	t_{DSMPW}	2	-	ns
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}
Read post- amble	t_{RPST}	0.4	-	t_{PERIOD}
Output DAT (referenced to Data Strobe)				
Slew rate	SR	1.125	-	V/ns

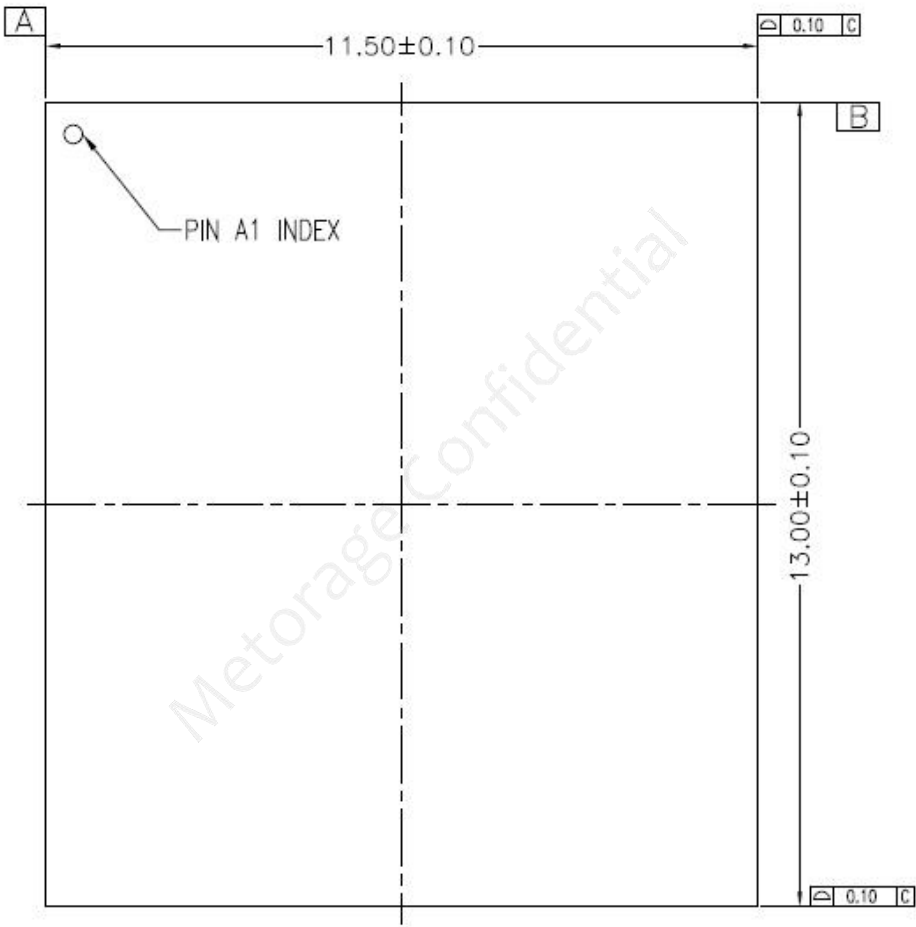
NOTE : Measured with HS400 reference load(6.2.4)

Table 6-16 HS400 Capacitance

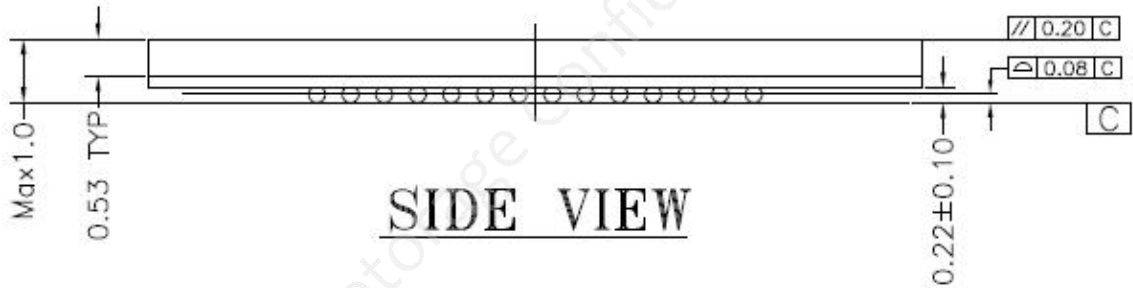
Parameter	Symbol	Min	Type	Max	Unit
Pull-up resistance for CMD	RCMD	4.7	-	50	Kohm
Pull-up resistance for DAT0-7	RDAT	10	-	50	Kohm
Pull-down resistance for Data Strobe	RDS	10	-	50	Kohm
Internal pull up resistance DAT1-DAT7	Rint	10	-	150	Kohm
Single Device capacitance	CDevice	-	-	6	pF

7. Package connections

Package Mechanical (11.5 x 13.0 x 1.0mm)



TOP VIEW



SIDE VIEW



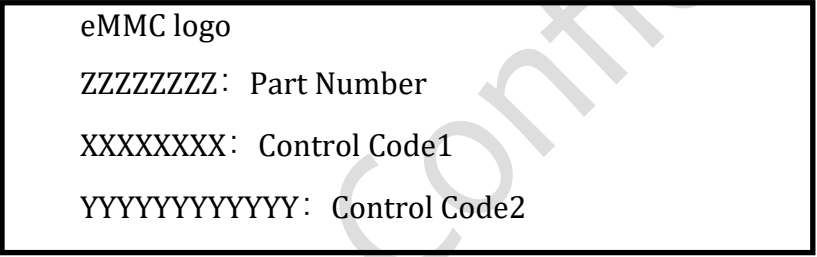
: The size data is tentative

8. Ball Assignment(153 ball)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	14
13	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	13
12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	12
11	NC	NC	NC									NC	NC	NC	11
10	NC	NC	NC		NC	NC	NC	VSS	VCC	NC		NC	NC	NC	10
9	NC	NC	NC		NC					VCC		NC	NC	NC	9
8	NC	NC	NC		NC					VSS		NC	NC	NC	8
7	NC	NC	NC		VSS					NC		NC	NC	NC	7
6	VSS	DAT7	VCCQ		VCC					NC		CLK	NC	VSSQ	6
5	DAT2	DAT6	NC		NC	Vcc	Vss	DS	Vss	RST_n		CMD	VSSQ	VCCQ	5
4	DAT1	DAT5	VSSQ	NC								VCCQ	VCCQ	VSSQ	4
3	DAT0	DAT4	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VCCQ	3
2	NC	DAT3	VDDi	NC	NC	NC	NC	NC	NC	NC	NC	NC	VssQ	NC	2
1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 8-1 153 ball assignment (Top View, Ball Side Down)

9. Marking



10. Appendix

10.1 Endurance characteristic

30,000 cycles/block