MPQ18913

30V, 0.3A, High-Frequency Transformer Driver for Automotive Applications, AEC-Q100

DESCRIPTION

The MPQ18913 is a high-frequency half-bridge transformer driver. It is ideal for use as the primary-side MOSFET in isolated power supplies for biasing silicon carbide (SiC) field-effect transistors (FETs), silicon FETs, and insulated gate bipolar transistors (IGBTs). The MPQ18913 simplifies an isolated biased supply's design by integrating the control, switching power stage, and protection circuitry in one device. This typology supports designs with a high isolation voltage and small interwinding capacitance.

The MPQ18913 features soft switching and an optional frequency spread spectrum (FSS) to optimize EMI performance. It supports a wide 5V to 30V input voltage (V_{IN}) range, and can survive surges of up to 50V. It also integrates two switching MOSFETs that are rated for 300mA of average input current (I_{IN}).

The device has a wide 400kHz to 5MHz configurable switching frequency (f_{SW}) range, which reduces the solution size and optimizes efficiency in resonant topologies (e.g. LLC converters).

Full safety and protection features include input over-voltage protection (OVP), over-current protection (OCP), and fault indication. The device's built-in soft start (SS) controls the inrush current during start-up.

The MPQ18913 is available in QFN-10 (2mmx2.5mm) package with wettable flanks.

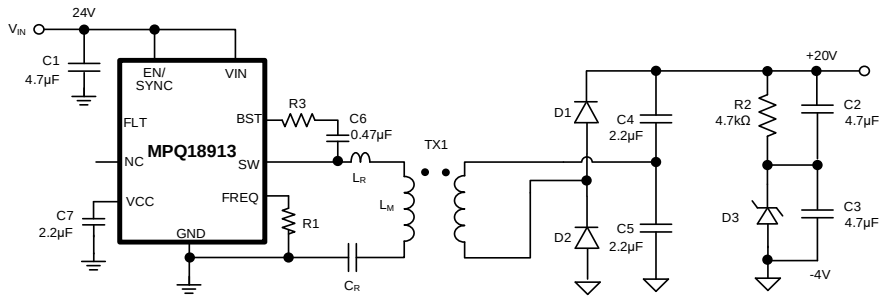
FEATURES

- Advanced Protection Features:
  - Over-Current Protection (OCP)
  - Short-Circuit Protection (SCP)
  - Over-Voltage Protection (OVP)
  - Over-Temperature Protection (OTP)
  - Fault Reporting
  - Under-Voltage Lockout (UVLO)
  - Supports Up to 5kV Isolation Voltage
- Low EMI:
  - Soft Switching
  - Flip-Chip Package
  - Frequency Spread Spectrum (FSS) Option
  - Low Interwinding Capacitance
- Small Solution Size:
  - 400kHz to 5MHz Configurable Switching Frequency (f_{SW})
  - Available in a Tiny QFN-10 (2mmx2.5mm) Package with Wettable Flanks

APPLICATIONS

- Silicon Carbide (SiC) Transformer Driver Biased Supplies
- Automotive Traction Inverters and Onboard Charging (OBC)
- DC Fast-Charging Stations
- Uninterrupted Power Supplies (UPSs) and Solar Inverters
- Isolated Power Supplies

TYPICAL APPLICATION



SELECTION GUIDE

Part Number	Soft-Start Time	Hiccup Time
MPQ18913GRPE-AEC1-Z	2ms	12ms
MPQ18913GRPE-A-AEC1-Z	20ms	120ms

ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ18913GRPE-AEC1*	QFN-10 (2mmx2.5mm)	*See Below*	1
MPQ18913GRPE-A-AEC1**			

* For Tape & Reel, add suffix -Z (e.g. MPQ18913GRPE-AEC1-Z).

** For Tape & Reel, add suffix -Z (e.g. MPQ18913GRPE-A-AEC1-Z).

TOP MARKING (MPQ18913GRPE-AEC1)

$\overline{\text{MLY}}$

LLL

ML: Product code of MPQ18913GRPE-AEC1
Y: Year code
LLL: Lot number

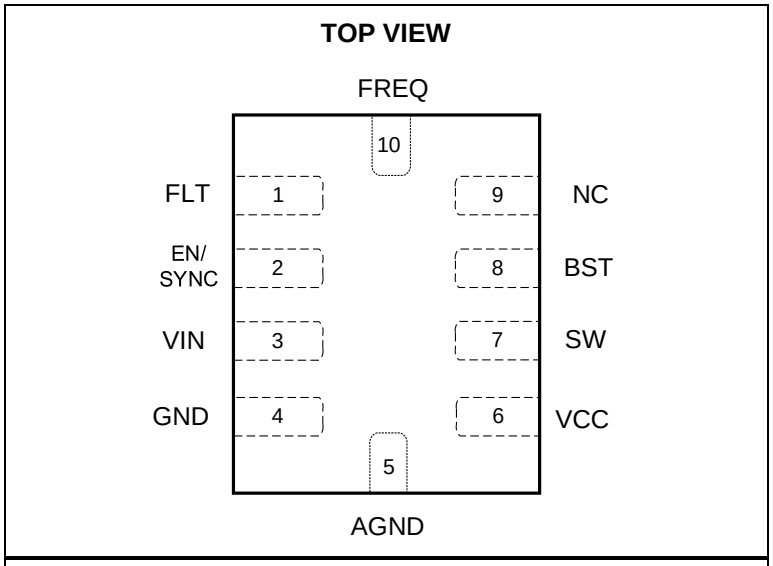
TOP MARKING (MPQ18913GRPE-A-AEC1)

$\overline{\text{MMY}}$

LLL

MM: Product code of MPQ18913GRPE-A-AEC1-Z
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-10 (2mmx2.5mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Description
1	FLT	**Fault indicator.** The FLT pin is an open-drain output.
2	EN/SYNC	**Enable and external clock.** Pull the EN/SYNC pin high to turn the device on; pull EN/SYNC low to turn it off. Apply an external clock to synchronous switching frequency (f_{SW}).
3	VIN	**Input voltage.** Bypass the VIN pin to GND using a 1µF ceramic capacitor, placed as close to the IC as possible.
4	GND	**Ground.**
5	AGND	**Analog ground.** Connect AGND to power ground using a single-point connection.
6	VCC	**Biased supply.** Decouple the VCC pins using a ⩾1µF ceramic capacitor referred to GND. Place this capacitor as close to VCC as possible.
7	SW	**Switching node.**
8	BST	**HS-FET driver voltage.** Connect a ceramic capacitor between the BST and SW pins.
9	NC	**Not connected.** For internal test use only. Leave the NC pin floating.
10	FREQ	**Switching frequency setting.** Connect a resistor between the FREQ and GND pins to set f_{SW}. Place this resistor as close to FREQ as possible.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{EN} ..... -0.3V to +35V
V_{SW} ..... -0.3V to (V_{IN} + 0.3V)
BST to SW..... -0.3V to +6.5V
V_{CC}, V_{DET}, V_{FLT}, V_{FREQ} ..... -0.3V to +6.5V
V_{IN}, V_{EN} (surge) ..... -0.3V to +50V
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-10 (2mmx2.5mm) 2.5W

ESD Ratings

Human body model (HBM) .....±2000V
Charged device model (CDM).....±2000V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 5V to 30V
External VCC bias ..... 4.86V to 5.5V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

EVQ-18913-D-00A (4)	45.3	7 °C/W
QFN-10 (2mmx2.5mm) (5)	70	2.3 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVQ18913-D-00A, 6-layer PCB.
5) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Transformer Driver						
VCC regulator voltage	V_{CC}	I_{CC} = 0mA to 20mA, V_{EN} = 1.5V	4.55	4.7	4.85	V
V_{CC} under-voltage lockout rising (UVLO) threshold	$V_{CC\_UVLO\_RISING}$	V_{CC} rising	4.1	4.25	4.4	V
V_{CC} UVLO falling threshold	$V_{CC\_UVLO\_FALLING}$	V_{CC} falling	3.95	4.1	4.25	V
V_{CC} UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			150		mV
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$	V_{IN} rising	4.35	4.65	4.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	V_{IN} falling	4	4.25	4.5	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			400		mV
Shutdown current	I_{SD}	V_{EN} = 0V		4	12	µA
Quiescent current	I_Q	V_{EN} =1.5V, f_{SW} = 1MHz (set by the FREQ resistor, R_{FREQ}), SW is floating		9.5		mA
Input over-voltage protection (OVP) rising threshold	V_{OVP_RISING}	Rising	31	33	35	V
Input OVP falling threshold	$V_{OVP\_FALLING}$	Falling	28.5	30.5	32.5	V
Input OVP hysteresis	V_{OVP_HYS}			2.5		V
EN start-up threshold	V_{EN_ON}	V_{EN} rising	1	1.1	1.2	V
EN shutdown threshold	V_{EN_OFF}	V_{EN} falling	0.8	0.9	1	V
EN hysteresis	V_{EN_HYS}			0.2		V
EN pull-down resistance	R_{EN}			2		MΩ
EN shutdown blanking time (6)	$t_{EN\_SD\_BLK}$	EN off to stop switching		6		µs
Synchronous (SYNC) input rising threshold	V_{SYNC_RISING}	Rising		1.7		V
SYNC input falling threshold	$V_{SYNC\_FALLING}$	Falling		0.9		V
SYNC input hysteresis	V_{SYNC_HYS}			0.8		V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{DS} = 0.1A		180		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{DS} =0.1A		180		mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 24V, T_J = 25°C			1	µA
		V_{EN} = 0V, V_{SW} = 24V, T_J = -40°C to 150°C			6	µA
Average SW capacitance	C_{SW}	V_{EN} = 0V, SW ramps up from 0V to 24V	100	125	150	pF
FLT output low voltage	V_{OL}			0.2	0.3	V
Switching frequency	f_{SW}	R_{FREQ} = 33kΩ	-3%	3	+3%	MHz
		R_{FREQ} = 100kΩ	-3%	1	+3%	MHz

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

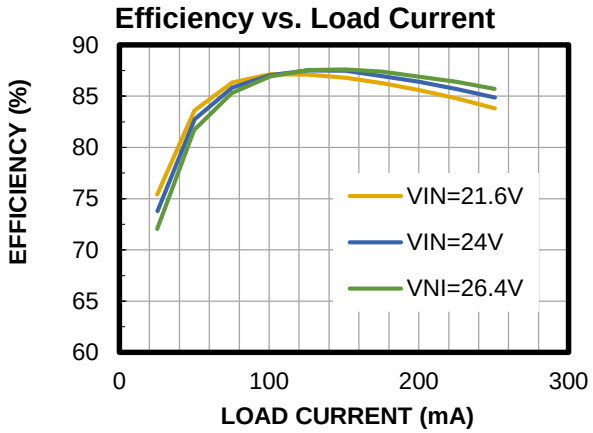
Parameter	Symbol	Condition	Min	Typ	Max	Units
FREQ resistor	R_{FREQ}		20		250	kΩ
SYNC frequency	f_{SYNC}		0.4		5	MHz
Over-current protection (OCP) threshold	I_{OCP}		-15%	1.2	+15%	A
Over-current protection (OCP) blanking time (6)	t_{OCP}	MPQ18913, R_{FREQ} = 100kΩ	-20%	1	+20%	ms
		MPQ18913-A, R_{FREQ} =100kΩ	-20%	20	+20%	ms
Short circuit protection (SCP) threshold	I_{SC}	Fast off limit		6		A
Hiccup time (6)	t_{HICCUP}	MPQ18913	-20%	12	+20%	ms
		MPQ18913-A	-20%	120	+20%	
Dead time (DT) (6)			-20%	25	+20%	ns
Soft-start time (6)	t_{SS}	MPQ18913, R_{FREQ} = 100kΩ		2		ms
		MPQ18913-A, R_{FREQ} = 100kΩ		20		ms
Thermal shutdown	T_{SD}			170		°C
Thermal shutdown hysteresis	ΔT_{SD}			20		°C

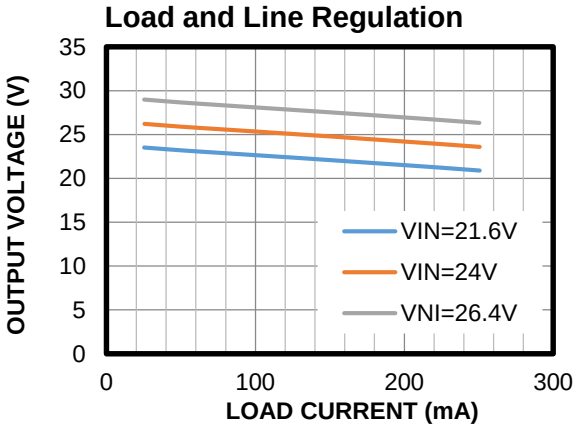
Note:

6) Derived from bench characterization. Not tested in production.

TYPICAL CHARACTERISTICS

Performance curves and waveforms are tested on the evaluation board, V_{IN} = 24V, V_{OUT} = 24V, T_A = 25°C, unless otherwise noted.



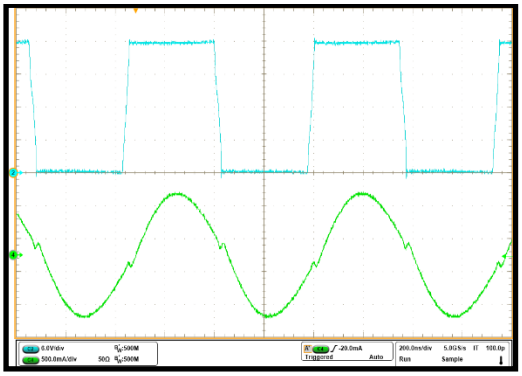


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, I_{OUT} = 0.25A, T_A = 25°C, unless otherwise noted.

Steady State

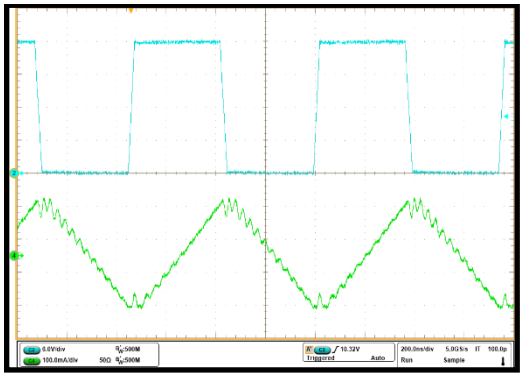
I_{OUT} = 0.25A



200ns/div.

Steady State

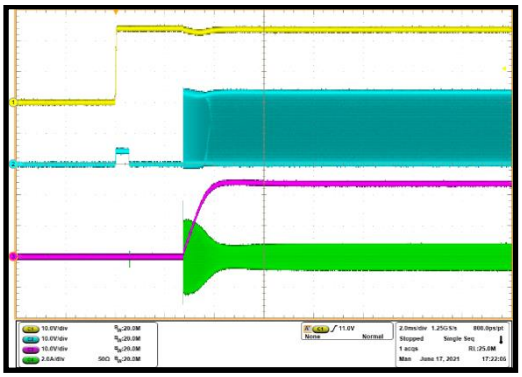
I_{OUT} = 0A



200ns/div.

Start-Up through VIN

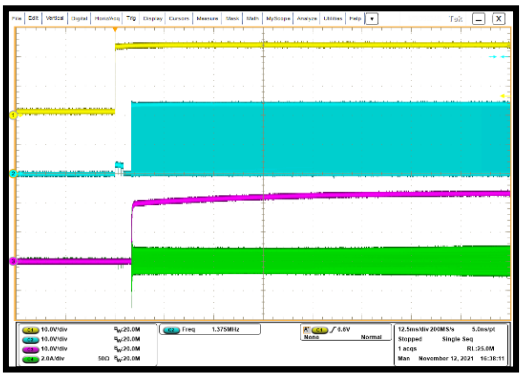
MPQ18913



2ms/div.

Start-Up through VIN

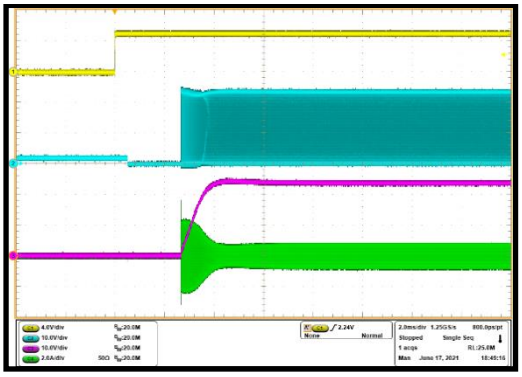
MPQ18913A



12.5ms/div.

Start-Up through EN

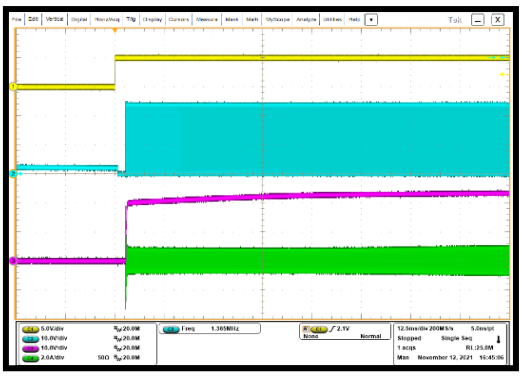
MPQ18913



2ms/div.

Start-Up through EN

MPQ18913A



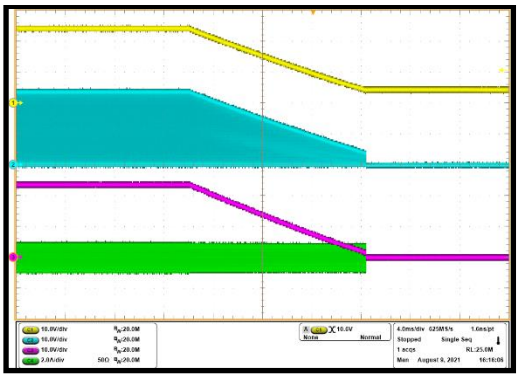
12.5ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, I_{OUT} = 0.25A, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

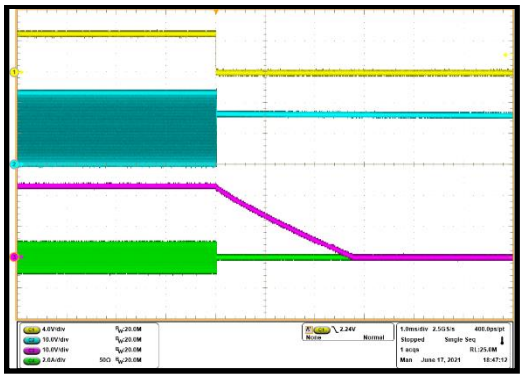
CH1: V_{IN} 10V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 2A/div



5ms/div.

EN Turn Off

CH1: EN 5V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 2A/div.

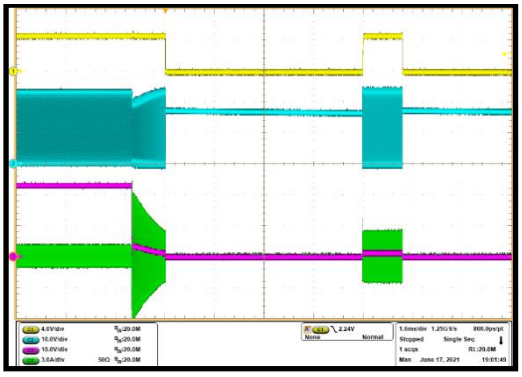


1ms/div.

Output Short

MPQ18913

CH1:FLT 4V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 3A/div.

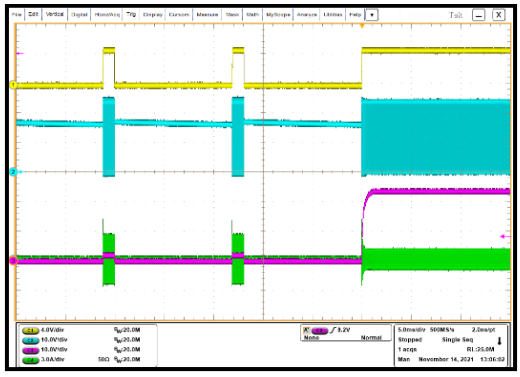


1.5ms/div.

Output Short Recovery

MPQ18913

CH1:FLT 4V/div.
CH2: SW 10V/div.
CH3: V_{OUT} 10V/div.
CH4: I_{PRI} 3A/div.



5ms/div.

FUNCTIONAL BLOCK DIAGRAM

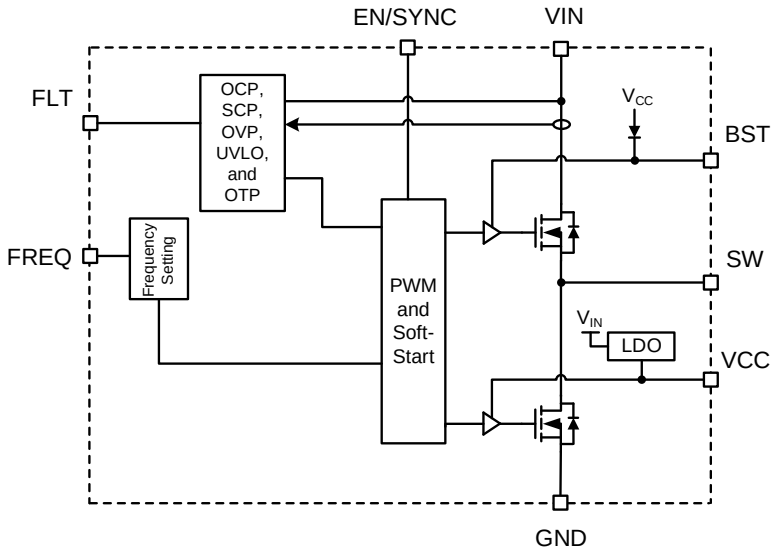


Figure 1: Functional Block Diagram

OPERATION

Enable Control (EN/SYNC)

The EN pin enables and disables the MPQ18913 power converter. Pull the EN voltage (V_{EN}) above the start-up threshold to enable the MPQ18913. The device starts switching after a delay time. The device is disabled when V_{EN} falls below the shutdown threshold. The EN/SYNC pin can support up to 30V. For automatic start-up, connect EN/SYNC directly to the VIN pin.

Then EN/SYNC pin can also be used for external clock synchronization. Connect a clock with a 400kHz to 1.67MHz frequency to the EN/SYNC pin. The internal clock frequency scales to be 1x or 3x the external clock frequency while continuing to operate at a 50% duty cycle. The scale factor is set by the FREQ resistor (R_{FREQ}).

Scale Factor	f_{SW} (MHz)	R_{FREQ} (kΩ)
1	0.4 to 1.5	100
3	1.5 to 5	33.2

Under-Voltage Lockout (UVLO)

The MPQ18913 implements separate under-voltage lockout (UVLO) protection for the input VIN and VCC pins. The maximum input voltage (V_{IN}) UVLO rising threshold can be as low as 4.9V to allow for start-up across the entire V_{IN} range. The FLT pin is always low during V_{IN} or V_{CC} UVLO.

Power Converter Soft Start (SS)

During start-up, the switching frequency (f_{SW}) is 2x the set frequency to limit the inrush current, and then gradually decreases to the set value.

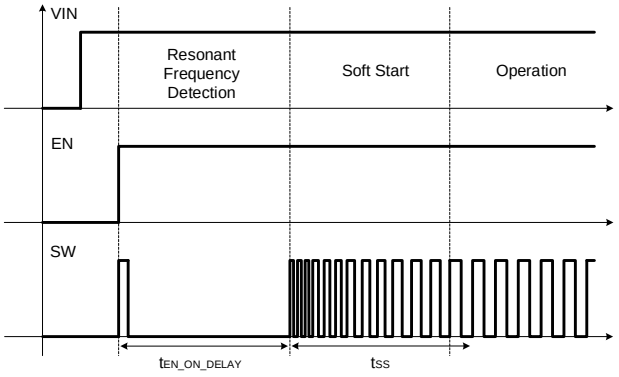


Figure 2: Timing Diagram during Start-Up

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

Over-Current protection (OCP) is implemented by measuring the instantaneous current ($I_{INSTANTANEOUS}$) on the low-side MOSFET (LS-FET). When the current exceeds the OCP threshold, f_{SW} increases to limit the input current (I_{IN}). If the over-current (OC) fault persists for longer than 1ms, the device stops switching, and automatically attempts to resume switching after a hiccup period (t_{HICCUP}). The FLT pin is also pulled low. The FLT pin is released once the part attempts to start switching again.

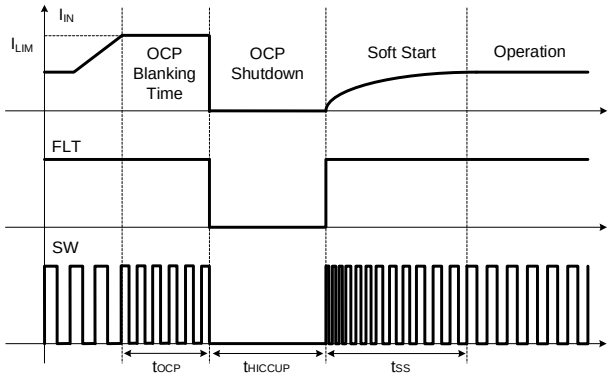


Figure 3: Timing Diagram during an OC Fault

Short-circuit protection (SCP) is implemented by sensing $I_{INSTANTANEOUS}$ on high-side MOSFET (HS-FET). SCP protects the device from dead shorts between SW and GND.

Over-Voltage Protection (OVP)

When V_{IN} exceeds the over-voltage protection (OVP) rising threshold, the converter immediately stops switching, and FLT pulls low. Once V_{IN} falls below the OVP falling threshold with hysteresis, the part starts switching and FLT releases.

Over-Temperature Protection (OTP)

The MPQ18913 consistently monitors the die temperature to implement over-temperature protection (OTP). When the die temperature exceeds the thermal shutdown threshold, the part stops switching and pulls FLT low. Once the temperature falls below thermal shutdown threshold with hysteresis, the part starts up again and FLT releases.

Fault Reporting (FLT)

The FLT pin is an open-drain output that is pulled low if one of the following occur: V_{IN} UVLO, V_{CC} UVLO, OCP (in hiccup or latch-off mode), SCP (in hiccup or latch-off mode), OVP, and OTP.

Table 1: Fault Reporting Functions (7)

EN	V_{IN}	V_{CC}	FLT
-	Powered	Powered	High
-	Not powered, UVLO	Not powered, UVLO	Low
Low	Powered	Not powered	Low
Low	Not powered, UVLO	Powered (8)	Low
High	Powered	Not powered, UVLO (8)	Low
High	Not powered, UVLO	Powered (8)	Low

Note:

7) "Powered" means that the device is no longer in V_{IN} or V_{CC} UVLO, and an internal or external supply is applied. "Not powered" means the pin is in UVLO.
8) This operation can only occur when an external V_{CC} bias is applied. It is not recommended to power V_{CC} while V_{IN} is not powered, or to pull EN high while V_{IN} is powered and V_{CC} is not powered.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Rectification Diodes

It is recommended to use Schottky diodes, due to their low forward voltage drop and fast recovery, to minimize power loss and achieve zero voltage switching (ZVS).

The diodes' peak current (I_{PEAK}) can be calculated with Equation (1):

$$I_{PEAK} \approx \Pi \times I_{LOAD} \quad (1)$$

Selecting the Output Capacitor (C_{OUT})

The output voltage ripple (ΔV_{OUT}) is determined by the powered device's capacitance and gate charge (e.g. SiC FET or IGBT). To maintain an acceptable ΔV_{OUT}, choose a proper output capacitance (C_{OUT}). C_{OUT} for the two V_{OUT} rails can be estimated with Equation (2):

$$C_{OUT\_POS\_RAIL} = C_{OUT\_NEG\_RAIL} \geq (QG / \Delta V_{OUT}) \quad (2)$$

If each rail's capacitance should exceed 22µF, then the MPQ18913A should be selected due to its longer soft-start time (t_{SS}).

Selecting the Switching Frequency (f_{SW})

A higher f_{SW} reduces the size of transformer, requires a larger transformer winding AC resistance, which limits the output power (P_{OUT}). Table 2 shows the recommended f_{SW}.

Table 2: Recommended f_{SW}

P_{OUT} (W)	f_{SW} (MHz)
≤6	0.4 to 0.75
≤3	0.75 to 2
≤2	1.5 to 5

The resistor between FREQ and GND (R_{FREQ}) sets f_{SW} (see Figure 4).

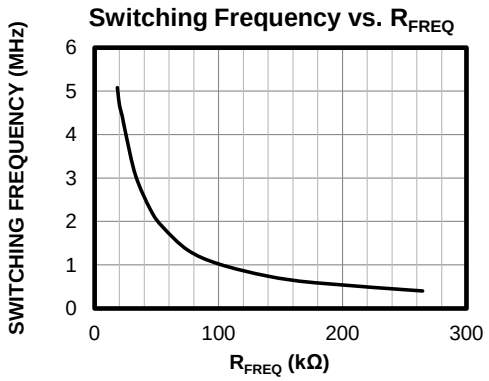


Figure 4: Switching Frequency vs. R_{FREQ}

Selecting the Transformer's Magnetizing Inductance

The magnetizing inductance (L_M) target design value is based on achieving ZVS. L_M can be calculated with Equation (3).

$$L_M = \frac{DT}{8 \times C_{SW} \times f_{SW}} = \frac{25ns}{8 \times 0.15nF \times f_{SW}} \quad (3)$$

If L_M exceeds the target value, then there is not enough magnetizing current to achieve full ZVS. With a low input voltage and small parasitic capacitance on the converter, partial ZVS may not cause excessive thermal or electrical stress. If L_M is below the design target value, there is more magnetizing current than required, which caused additional conduction loss in the FET and copper loss in the transformer. Given the small on resistance of the integrated FET and reasonable AC resistance of the transformer, the additional loss can be manageable.

L_M should exceed 10x the leakage inductance to reduce V_{OUT}'s sensitivity to the inductance and resonant capacitance variation.

Selecting the Resonant Capacitor (C_R)

The resonant capacitance (C_R) can be calculated with Equation (4):

$$C_R = \frac{1}{4 \times \pi^2 \times L_R \times f_{SW}^2} \quad (4)$$

Where L_R is the transformer leakage inductance, reflected to the primary side.

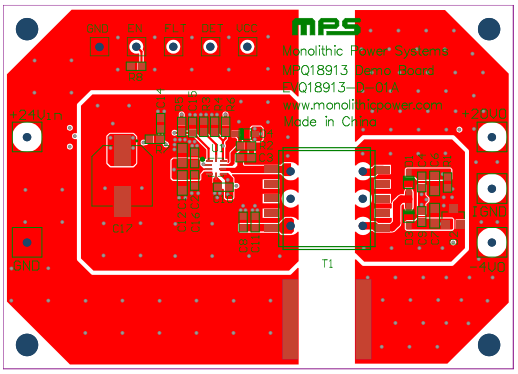
PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

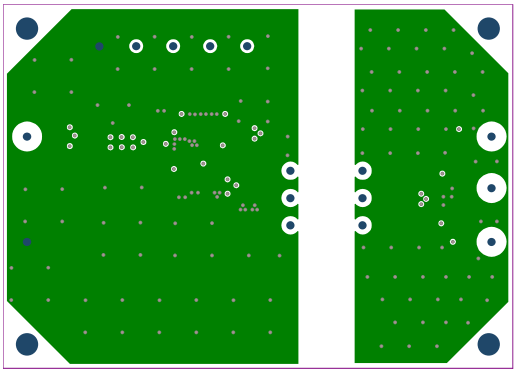
1. Place the input capacitor, VCC capacitor, and BST capacitor as close to the corresponding pins as possible.
2. Place the R_{FREQ} as close to the FREQ pin as possible.
3. Connect R_{FREQ} using short and direct traces. The other R_{FREQ} terminal should be connected to AGND.
4. Connect AGND to power ground through a single-point connection.
5. Minimize the switching node areas on both the primary and secondary sides to reduce EMI.
6. Place the input filter on the bottom layer to reduce EMI.

Note:

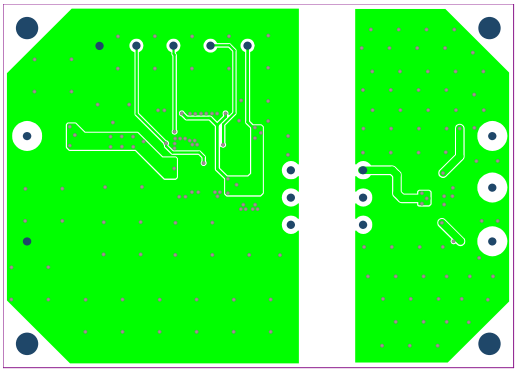
9) The recommended layout is based on Figure 6 on page 14.



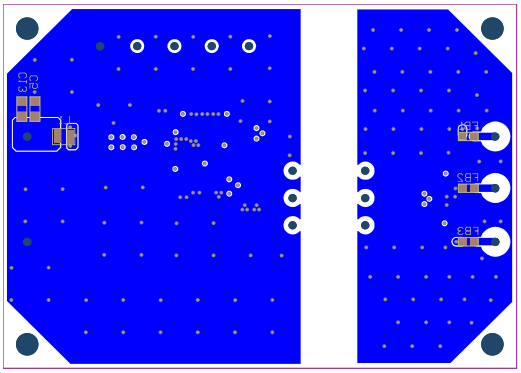
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

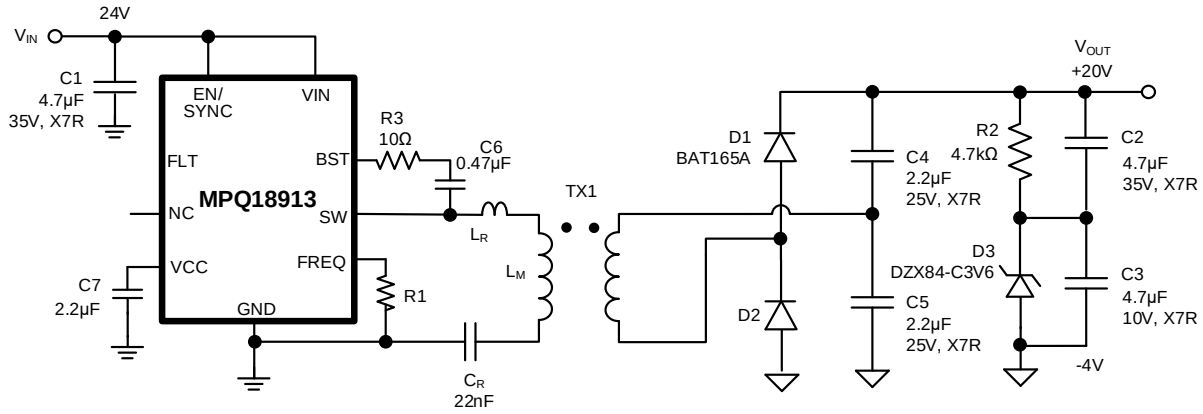
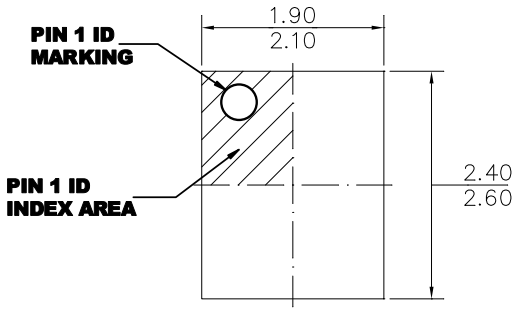


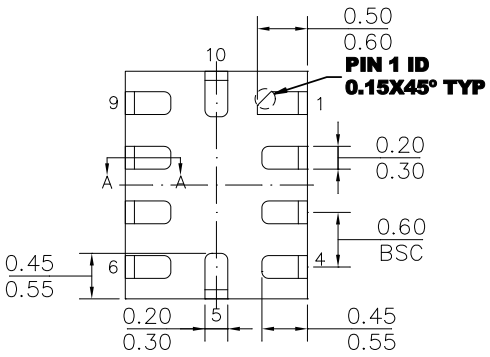
Figure 6: Typical Application Circuit (V_{IN} = 24V, V_{OUT} = +20V/-4V, 6W LLC, Start Up through VIN)

PACKAGE INFORMATION

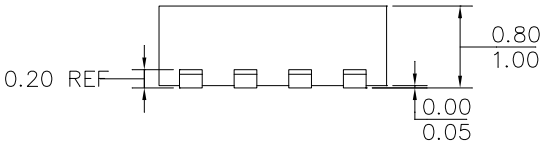
QFN-10 (2mmx2.5mm)



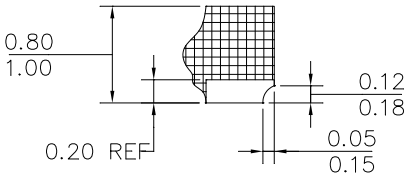
TOP VIEW



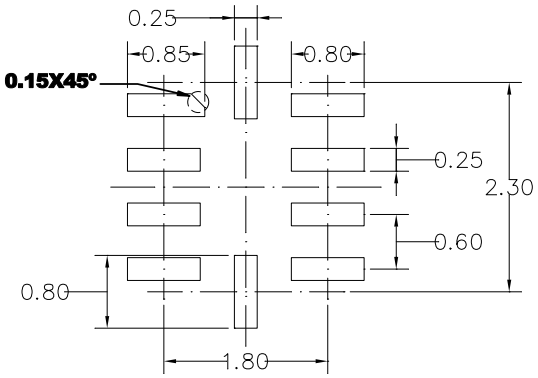
BOTTOM VIEW



SIDE VIEW



SECTION A-A

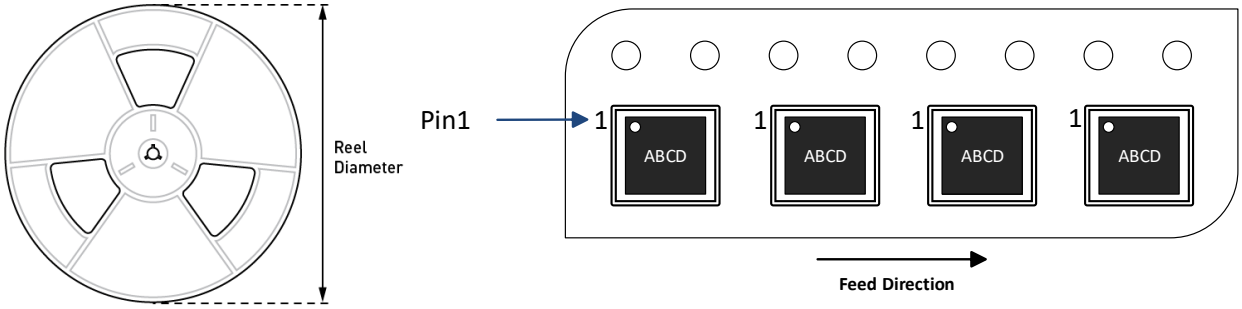


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ18913GRPE-AEC1-Z	QFN-10 (2mmx2.5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ18913GRPE-A-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/24/2023	Initial Release	-
1.01	7/18/2024	Updated R3 and C6 to be in series in Typical Application circuit diagram	1, 14
		• Updated formatting for Equation (1) • Updated “28” to “8” and “0.17nF” to “0.15nF” in Equation (3) • Fixed formatting in Table 2, Figure 4, and Selecting the Transformer’s Magnetizing Inductance section	12