Trion® T120 BGA324 Development Kit User Guide

T120F324-DK-UG-v2.7
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www.elitestek.com

Contents

Introduction

Thank you for choosing the Trion® T120 BGA324 Development Kit (part number: T120F324-DK), which allows you to explore the features of the T120 FPGA with a MIPI CSI-2 interface and DDR controller. The kit includes 3 daughter cards that let you connect MIPI cameras, a Raspberry Pi V2 camera module, and extend the GPIO, plus a Raspberry Pi camera module and accessories.

Warning: The board can be damaged without proper anti-static handling.

What's in the Box?

The Trion® T120 BGA324 Development Kit includes:

- Trion® T120 BGA324 Development Board preloaded with a demonstration design
- MIPI and LVDS Expansion Daughter Card
- 2 Raspberry Pi Camera Connector Daughter Cards
- Raspberry Pi V2 camera module with 15-pin FFC/FPC cable
- 10 standoffs, 10 screws, and 6 nuts for development board and daughter cards
- 3 foot USB cable (type A to micro type B)
- Universal AC to DC power adapter

Important: This kit includes a power cable with a type A plug (U.S. style). You need an adapter to use this cable with other socket types.

Register Your Kit

When you purchase an 易灵思 development kit, you also receive a license for the Efinity® software plus one year of software upgrades and patches. The Efinity® software is available for download from the Support Center on the 易灵思 web site.

To get access to our Support Center to download your software, register your development kit at **https://www.elitestek.com/register**.

Download the Efinity® Software

To develop your own designs for the T120 device on the board, you must install the Efinity® software. You can obtain the software from the 易灵思 Support Center under Efinity Software (**www.elitestek.com/support/**).

The Efinity® software includes tools to program the device on the board. Refer to the Efinity® Software User Guide for information about how to program the device.

Learn more: Efinity® documentation is installed with the software (see **Help** > **Documentation**) and is also available in the Support Center under Documentation (**www.elitestek.com/support/**).

Installing the Linux USB Driver

The following instructions explain how to install a USB driver for Linux operating systems.

1. Disconnect your board from your computer.
2. In a terminal, use these commands:

```
> sudo <installation directory>/bin/install_usb_driver.sh
> sudo udevadm control --reload-rules
```

Note: If your board was connected to your computer before you executed these commands, you need to disconnect and re-connect it.

Installing the Windows USB Drivers

On Windows, you use software from Zadig to install drivers. Download the Zadig software (version 2.7 or later) from **zadig.akeo.ie**. (You do not need to install it; simply run the downloaded executable.)

To install the driver:

1. Connect the board to your computer with the appropriate cable and power it up.
2. Run the Zadig software.

   Note: To ensure that the USB driver is persistent across user sessions, run the Zadig software as administrator.

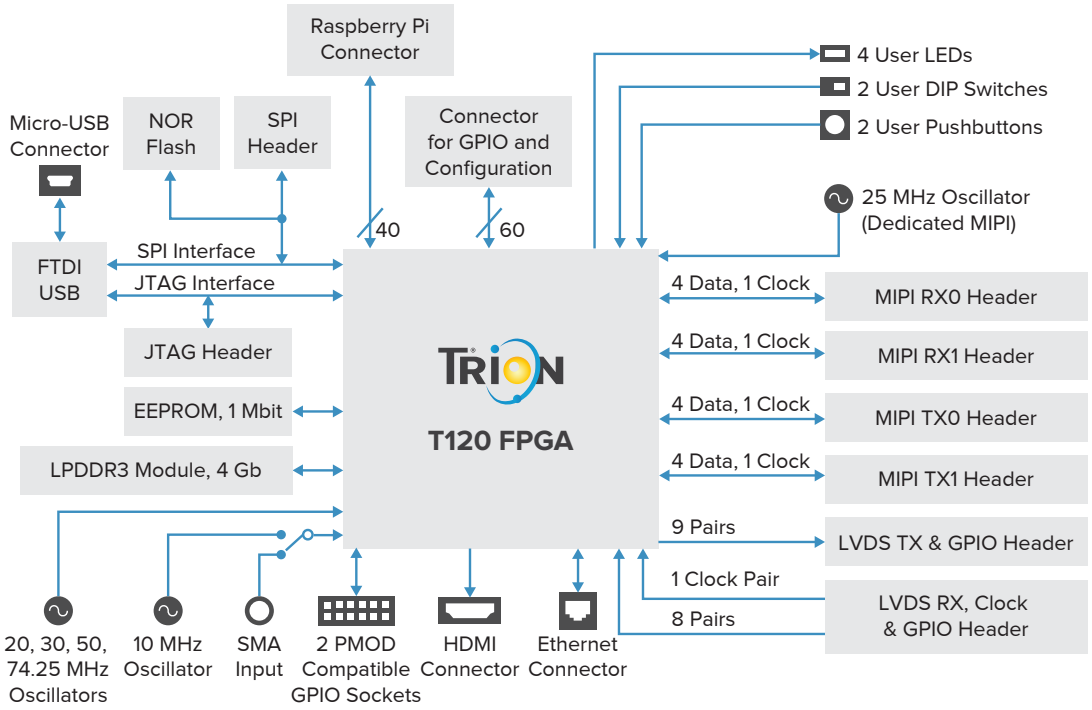
3. Choose **Options** > **List All Devices**.
4. Repeat the following steps for each interface. The interface names end with *(Interface N)*, where *N* is the channel number.
   - Select **libusb-win32** in the **Driver** drop-down list.
   - Click **Replace Driver**.
5. Close the Zadig software.

Note: This section describes how to install the libusb-win32 driver for each interface separately. If you have previously installed a composite driver or installed using libusbK drivers, you do not need to update or reinstall the driver. They should continue to work correctly.

Board Functional Description

The Trion® T120 BGA324 Development Board contains a variety of components to help you build designs for the Trion® T120 device.

Figure 1: Trion® T120 BGA324 Development Board Block Diagram



Features

- 易灵思® T120F324I4 device in an 324-ball FineLine BGA package with MIPI CSI-2 interface and DDR DRAM controller
- LPDDR3 256 Mbits x 16 bits memory supporting up to 4 Gb
- HDMI 1080p transmitter for video output
- Triple-speed Ethernet PHY
- 1 Mbit EEPROM
- 128 Mbit SPI NOR flash memory
- FTDI FT2232H dual-channel chipset with USB controller
- Micro-USB type B receptacle
- Designed to accommodate multiple daughter cards:
  - Four MIPI high-speed connectors to attach 易灵思 camera connector daughter cards
  - Two LVDS high-speed headers to attach the 易灵思 GPIO daughter card
- 60-pin high-speed connector for user I/O
- 40-pin socket compatible with Raspberry Pi computer
- Two 12-pin PMOD-compatible GPIO sockets
- User LEDs and switches:
  - 4 LEDs on T120F324I4 bank 2F
  - 2 pushbutton switches (connected to bank 2F I/O pins)
  - 2 DIP switches (connected to bank 2F I/O pins)
- 10, 20, 25, 30, 50, and 74.25 MHz oscillators for T120F324I4 PLL input

- Optional 3.3 V external clock source available through SMA input to drive the T120F324I4 PLL input or clock input pin
- Power:
  - Power source: 12 V, 5 A power supply
  - On-board regulator sources: 1.2 V (5 A), 1.25 V (0.5 A), 3.3 V (5 A), 5 V (0.5 A), 1.8 (2 A), 2.5V (2 A), and 2.8 V (0.5 A)
  - On-board regulator for LPDDR3 memory
  - Fixed 3.3 V VCCIO for T120F324I4 I/O banks 1A, 1D, 1E, 1F, 1G, 2D, 2E, 3D, 4E, and 4F
  - User selectable voltages from 1.8 V, 2.5 V, and 3.3 V for bank 1B, 1C, and 2F
  - Optional header for camera power supply with power on sequence
  - Optional header for daughter card power supply
- Power good and T120F324I4 configuration done LEDs

Overview

The board features the 易灵思® T120 programmable device in a 324-ball FBGA package, which is fabricated using 易灵思® Quantum™ technology. The Quantum™-accelerated programmable logic and routing fabric is wrapped with an I/O interface in a small footprint package. T120 devices also include embedded memory blocks and multiplier blocks (or DSP blocks). You create designs for the T120 device in the Efinity® software, and then download the resulting configuration bitstream to the board using the USB connection.

Learn more: For more information on T120 FPGAs, refer to the T120 Data Sheet.

Figure 2: Trion® T120 BGA324 Development Board Components (Top)

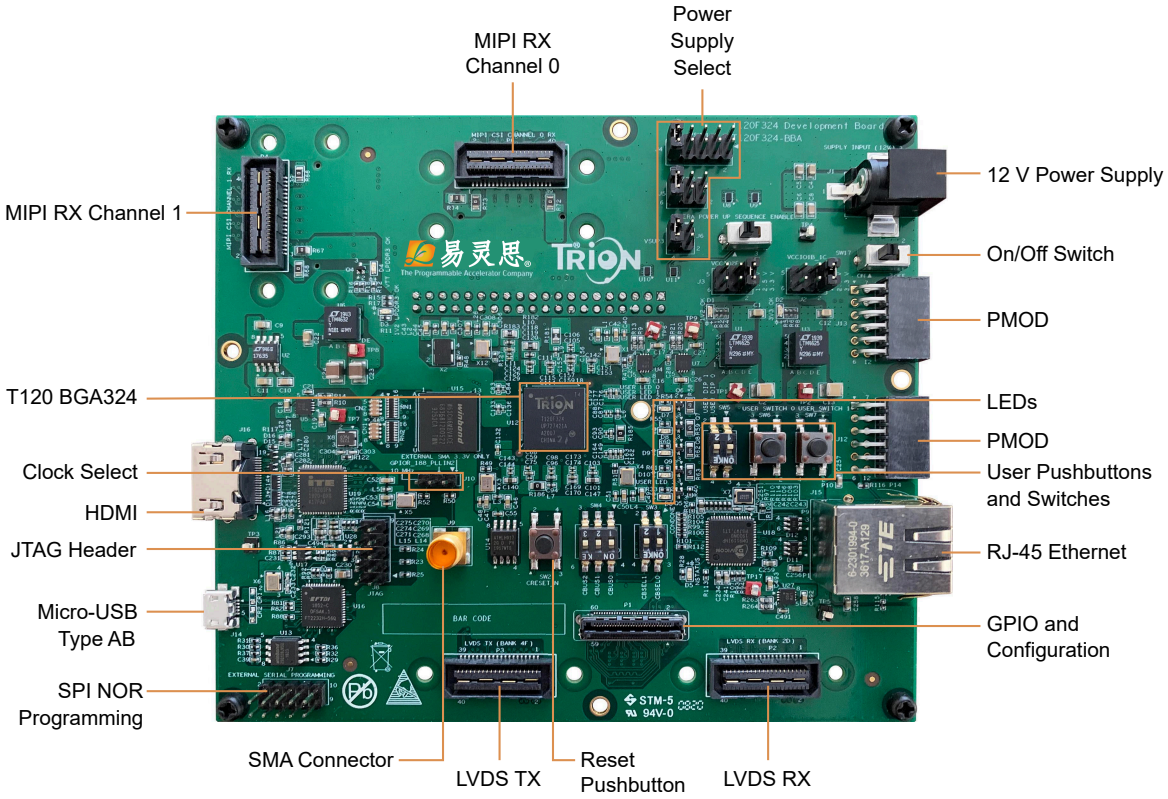
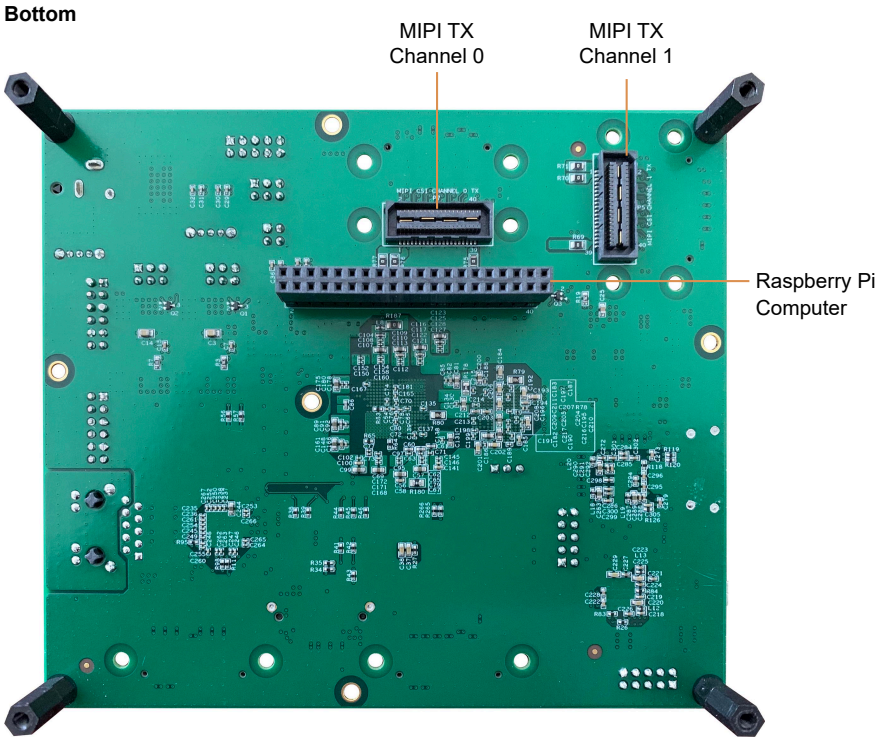


Figure 3: Trion® T120 BGA324 Development Board Components (Bottom)



The Trion® T120 BGA324 Development Board provides four 0.8 mm high-speed ground plane sockets for the MIPI CSI-2 interface and two 0.8 mm high-speed ground plane sockets for the LVDS transmitters and receivers. It has two sockets to connect PMOD-compatible peripherals. Additionally, it has a 0.5 mm high-speed connector for additional I/O pins and one 40-pin header for connecting to a Raspberry Pi computer.

The FTDI FT2232H module has two channels to support SPI (FTDI interface 0) and JTAG (FTDI interface 1) configuration. It receives the T120 configuration bitstream from a USB host and writes to the on-board SPI NOR flash memory. After a reset in SPI passive mode, the FTDI controller can also write the configuration bitstream directly to the FPGA. Additionally, it supports direct JTAG programming mode in which it writes the configuration bitstream directly to the FPGA through the JTAG interface.

Learn more: Refer to AN 006 Configuring Trion FPGAs for more information.

The SPI NOR flash memory stores the configuration bitstream it receives from the FTDI FT2232H module. The T120 device accesses this configuration bitstream when it is in active configuration mode (default).

The board's main power supply is the 12 V DC input. Use the included power supply to provide the board with power through the 12 V input jack. The recommended power input is a 12 V (5 A minimum) DC power source.

Note: Although the Trion® T120 BGA324 Development Board has a different power-up sequence, you should follow the power-up sequence in the T20 Data Sheet when designing your own board. For improved reliability, 易灵思® recommends that you use supervisor IC at `CRESET_N` explained in AN 006 Configuring Trion FPGAs.

The board regulates down the 12 V DC input using on-board switching regulators to provide the necessary voltages for the T120 device, LPDDR3, Ethernet PHY, HDMI transmitter, PMOD module, SPI flash memory, SDRAM and on-board oscillator.

Learn more: Refer to the Trion® T120 BGA324 Development Board Schematics and BOM for more information about the components used in the Trion® T120 BGA324 Development Board.

Power On

To turn on the development board, turn on switch SW17. Upon power-up, the 12 V DC power is input to the on-board regulators through 12 V input jack (CON1) to generate the required 3.3 V, 2.8 V, 2.5 V, 1.8 V, 1.25 V, and 1.2 V for components on the board. When these voltages are up and stable, on-board LEDs (D1, D2, D3, and D4) illuminate, giving you a visual confirmation that the power supplies on the board are up and stable.

Note: The micro-USB cable cannot power the board. You must use the provided 12 V DC power adapter cable.

Reset

The T120F324I4 device is typically brought out of reset with the CRESET signal. Upon power up, the T120F324I4 device is held in reset until CRESET toggles high-low-high.

Note: You can manually assert the high-low-high transition with pushbutton switch SW2.

CRESET has a pull-up resistor. When you press SW2, the board drives CRESET low; when you release SW2, the board drives CRESET high. Thus, a single press of SW2 provides the required high-low-high transition.

After toggling CRESET, the T120F324I4 device goes into configuration mode and reads the device configuration bitstream from the flash memory. When configuration completes successfully, the device drives the CDONE signal high. CDONE is connected to a green LED (D6), which turns on when the T120F324I4 device enters user mode.

Clock Sources

Six on-board oscillators (10, 20, 25, 30, 50, and 74.25 MHz), are available to drive the T120F324I4 PLL input pin and clock input. Alternatively, you can disable the 10 MHz oscillator and use an external clock source through the SMA input (J9). Set jumper J10 to use the 10 MHz or SMA input as the clock source.

Table 1: Oscillator and Clock Generator Sources

Clock Source	PLL Input Pin	PLL
10 MHz oscillator or 3.3 V SMA input	GPIOR_188_PLLIN2	PLL_BR2
20 MHz oscillator	GPIOR_167_PLLIN1	PLL_TR1
25 MHz oscillator	GPIOR_169_MREFCLK	Dedicated MIPI clock source
30 MHz oscillator	GPIOL_15_PLLIN0	PLL_BL0
50 MHz oscillator	GPIOR_186_PLLIN0	PLL_BR0
74.25 MHz oscillator	GPIOR_166_PLLIN0	PLL_TR0

Configuration

The Trion® T120 BGA324 Development Board has two DIP switches to set the configuration mode for the T120 FPGA.

Learn more: For more details on configuration, refer to AN 006 Configuring Trion FPGAs.

Table 2: Configuration Pins

Reference	Configuration Pin	Notes
SW3	CBSEL	Choose which image to load from the SPI flash device.
SW4	CBUS	Select configuration bus width for SPI active or passive configuration.

EEPROM

The Trion® T120 BGA324 Development Board has a 1 Mbit (131,072 x 8) EEPROM to store user data (part number AT24CM01-SHD-T). You can program the EEPROM through the I^2C bus at the preset address 0x50.

Table 3: EEPROM Pins

Signal Name	FPGA Pin
EEPROM_SCL	GPIOL_04
EEPROM_SDA	GPIOL_05

Camera Power-Up Circuit

The Trion® T120 BGA324 Development Board includes a basic power up sequence circuit for MIPI CSI-2 cameras. You control the circuit using SW1. When SW1 is on, the power up goes from VSUP1 to VSUP2 to VSUP3 in sequence.

Note: To apply power in sequence, set the jumpers for J4, J5 and J6 as described in **Header J4, J5, and J6 (Power Select)** on page 17.

Headers

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

Table 4: Trion® T120 BGA324 Development Board Headers

Reference Designator	Description
P1	60-pin high-speed connector for GPIO and configuration
P2	40-pin high-speed connector for LVDS receiver (RX) and GPIO
P3	40-pin high-speed connector for LVDS transmitter (TX) and GPIO
P4	40-pin connector for MIPI CSI-2 channel 1 receiver, 1.8, 2.5, 3.3 V GPIO, and power supply
P5	40-pin connector for MIPI CSI-2 channel 1 transmitter, 1.8, 2.5, 3.3 V GPIO, and power supply
P6	40-pin connector for MIPI CSI-2 channel 0 receiver, 1.8, 2.5, 3.3 V GPIO, and power supply
P7	40-pin connector for MIPI CSI-2 channel 0 transmitter, 1.8, 2.5, 3.3 V GPIO, and power supply
J1	12 V DC power supply input jack
J2	User selectable VCCIO for banks 1B and 1C
J3	User selectable VCCIO for bank 2F
J4	User selectable supply with or without power up sequence for MIPI CSI-2 camera (5.0 V, 3.3 V, and 2.8 V)
J5	User selectable supply with or without power up sequence for MIPI CSI-2 camera (3.3 V and 1.8 V)
J6	User selectable supply with or without power up sequence for MIPI CSI-2 camera (1.2 V)
J7	External SPI NOR flash programming header
J8	JTAG header
J9	SMA connector for external 3.3 V clock source input
J10	3-pin header to select whether to use the on-board 10 MHz oscillator or SMA input from external clock source
J11	40-pin connector compatible with Raspberry Pi computer
J12, J13	12-pin PMOD socket
J14	Micro-USB Type-AB receptacle
J15	RJ-45 triple-speed Ethernet connector
J16	HDMI output connector

Header P1 (GPIO and Configuration)

P1 is a high-speed connector (part number is LSHM-130-02.5-L-DV-A-S-TR) that you can connect to an external board. Through it, the external board can configure the T120 FPGA and control the GPIO. P1 connects to GPIO pins in banks 1B, 1C, 1G, 3D, and TR. These pins are fixed to 3.3 V.

P1 also provides 12 V DC power directly from the DC adapter. To connect to P1, use part number: LSHM-130-02.5-L-DV-A-S-TR.

Table 5: P1 Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name
1	12V	2	12V
3	GPIOL_01_CCK	4	GPIOL_11_CBUS0
5	GPIOL_00_SS_N	6	GPIOL_12_CBUS1
7	GPIOL_08_CDI0	8	GPIOL_13_CBUS2
9	GPIOL_09_CDI1	10	CDONE
11	GPIOL_14_CDI2	12	GPIOL_150_NSTATUS
13	GPIOL_16_CDI3	14	CRESET_N
15	GPIOL_18_CDI4	16	NC
17	GPIOL_20_CDI5	18	NC
19	GPIOL_22_CDI6	20	NC
21	GPIOL_24_CDI7	22	NC
23	GND	24	NC
25	GPIOL_66_CLK0	26	GND
27	GPIOT_RXP15	28	NC
29	GPIOT_RXN15	30	NC
31	GPIOT_RXP16	32	NC
33	GPIOT_RXN16	34	NC
35	GPIOT_RXP17	36	NC
37	GPIOT_RXN17	38	NC
39	GPIOT_RXP18_EXTFB1	40	NC
41	GPIOT_RXN18_EXTFB1	42	NC
43	GND	44	GND
45	GPIOR_168_PLLIN2	46	NC
47	GPIOR_187_PLLIN1	48	NC
49	GPIOT_RXN14	50	NC
51, 53, 55, 57, 59	NC	52, 54, 56, 58, 60	NC
61	GND	62	GND

Headers P2 and P3 (LVDS)

P2 and P3 contain the LVDS signals. Each header has 9 dedicated LVDS channels. You can also use LVDS pins as GPIO.

Learn more: Refer to the Trion Interfaces User Guide for instructions on using the LVDS pins as GPIO.

Table 6: P2 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	GPIOT_RXP09_CLKP0	Dedicated LVDS RX clock	2	GPIOT_RXP07	Dedicated LVDS RX Channel 07
3	GPIOT_RXN09_CLKN0		4	GPIOT_RXN07	
5	GND	Ground	6	GND	Ground
7	GPIOT_RXP01	Dedicated LVDS RX Channel 01	8	GPIOT_RXP08	Dedicated LVDS RX Channel 08
9	GPIOT_RXN01		10	GPIOT_RXN08	
11	GND	Ground	12	GND	Ground
13	GPIOT_RXP02	Dedicated LVDS RX Channel 02	14	NC	No Connect
15	GPIOT_RXN02		16	NC	
17	GND	Ground	18	GND	Ground
19	GPIOT_RXP03	Dedicated LVDS RX Channel 03	20	NC	No Connect
21	GPIOT_RXN03		22	NC	
23	GND	Ground	24	GND	Ground
25	GPIOT_RXP04	Dedicated LVDS RX Channel 04	26	NC	No Connect
27	GPIOT_RXN04		28	NC	
29	GND	Ground	30	GND	Ground
31	GPIOT_RXP05	Dedicated LVDS RX Channel 05	32	NC	No Connect
33	GPIOT_RXN05		34	NC	
35	GND	Ground	36	GND	Ground
37	GPIOT_RXP06	Dedicated LVDS RX Channel 06	38	NC	No Connect
39	GPIOT_RXN06		40	NC	

Table 7: P3 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	GPIOB_TXP00	Dedicated LVDS TX Channel 00	2	GPIOB_TXP07	Dedicated LVDS TX Channel 07
3	GPIOB_TXN00		4	GPIOB_TXN07	
5	GND	Ground	6	GND	Ground
7	GPIOB_TXP01	Dedicated LVDS TX Channel 01	8	GPIOB_TXP08	Dedicated LVDS TX Channel 08
9	GPIOB_TXN01		10	GPIOB_TXN08	
11	GND	Ground	12	GND	Ground
13	GPIOB_TXP02	Dedicated LVDS TX Channel 02	14	NC	No Connect
15	GPIOB_TXN02		16	NC	
17	GND	Ground	18	GND	Ground
19	GPIOB_TXP03	Dedicated LVDS TX Channel 03	20	NC	No Connect
21	GPIOB_TXN03		22	NC	
23	GND	Ground	24	GND	Ground
25	GPIOB_TXP04	Dedicated LVDS TX Channel 04	26	NC	No Connect
27	GPIOB_TXN04		28	NC	
29	GND	Ground	30	GND	Ground
31	GPIOB_TXP05	Dedicated LVDS TX Channel 05	32	NC	No Connect
33	GPIOB_TXN05		34	NC	
35	GND	Ground	36	GND	Ground
37	GPIOB_TXP06	Dedicated LVDS TX Channel 06	38	NC	No Connect
39	GPIOB_TXN06		40	NC	

Headers P4 and P6 (MIPI Receiver)

P4 and P6 are dedicated MIPI CSI-2 receiver high-speed interface connectors that support 1 clock lane and 4 data lanes. These headers also include optional supply pins VSUP1, VSUP2, VSUP3, as well as five 1.8 V or 3.3 V GPIO pins (user selectable). You can use these connectors to attach a camera connector daughter card.

Table 8: MIPI Receiver Channel 0 (P6) and Channel 1 (P4)

where x is 1 or 0

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	Voltage supply 1	2	MIPI*x*_RXD_P0	Differential MIPI Receiver Channel Lane 0
3	VSUP2	Voltage supply 2	4	MIPI*x*_RXD_N0	
5	GND	Ground	6	GND	Ground
7	NC	No Connect	8	MIPI*x*_RXD_P1	Differential MIPI Receiver Channel Lane 1
9	NC		10	MIPI*x*_RXD_N1	
11	GND	Ground	12	GND	Ground
13	NC	No Connect	14	MIPI*x*_RXD_P2	Differential MIPI Receiver Channel Lane 2
15	NC		16	MIPI*x*_RXD_N2	
17	GND	Ground	18	GND	Ground
19	NC	No Connect	20	MIPI*x*_RXD_P3	Differential MIPI Receiver Channel Lane 3
21	NC		22	MIPI*x*_RXD_N3	
23	GND	Ground	24	GND	Ground
25	NC	No Connect	26	MIPI*x*_RXD_P4	Differential MIPI Receiver Channel 0 Lane 4
27	NC		28	MIPI*x*_RXD_N4	
29	GND	Ground	30	GND	Ground
31	NC	No Connect	32	USER_SWITCH0 (P4) PMOD_A_IO0 (P6)	1.8 or 3.3 V GPIO
33	NC		34	USER_SWITCH1 (P4) PMOD_A_IO1 (P6)	1.8 or 3.3 V GPIO
35	GND	Ground	36	GND	Ground
37	VSUP3	Voltage supply 3	38	USER_DIP0 (P4) PMOD_A_IO2 (P6)	1.8 or 3.3 V GPIO
39	GPIOT_RXP16 (P4) GPIOT_RXP15 (P6)	1.8 or 3.3 V GPIO	40	USER_DIP1 (P4) PMOD_A_IO3 (P6)	1.8 or 3.3 V GPIO

Headers P5 and P7 (MIPI Transmitters)

P5 and P7 are dedicated MIPI CSI-2 transmitter high-speed interface connectors that support 1 clock lane and 4 data lanes. These headers also include optional supply pins VSUP1, VSUP2, VSUP3, as well as five 1.8 V or 3.3 V GPIO pin (user selectable). You can use these connectors to attach a camera connector daughter card.

Note: P5 and P7 are located on the bottom of the board.

Table 9: MIPI Transmitter Channel 0 (P7) and Channel 1 (P5)

where x is 1 or 0

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	Voltage supply 1	2	MIPI*x*_TXD_P0	Differential MIPI Transmitter Channel Lane 0
3	VSUP2	Voltage supply 2	4	MIPI*x*_TXD_N0	
5	GND	Ground	6	GND	Ground
7	NC	No Connect	8	MIPI*x*_TXD_P1	Differential MIPI Transmitter Channel Lane 1
9	NC		10	MIPI*x*_TXD_N1	
11	GND	Ground	12	GND	Ground
13	NC	No Connect	14	MIPI*x*_TXD_P2	Differential MIPI Transmitter Channel Lane 2
15	NC		16	MIPI*x*_TXD_N2	
17	GND	Ground	18	GND	Ground
19	NC	No Connect	20	MIPI*x*_TXD_P3	Differential MIPI Transmitter Channel Lane 3
21	NC		22	MIPI*x*_TXD_N3	
23	GND	Ground	24	GND	Ground
25	NC	No Connect	26	MIPI*x*_TXD_P4	Differential MIPI Transmitter Channel Lane 4
27	NC		28	MIPI*x*_TXD_N4	
29	GND	Ground	30	GND	Ground
31	NC	No Connect	32	USER_LED0 (P5) PMOD_A_IO4 (P7)	1.8 or 3.3 V GPIO
33	NC		34	USER_LED1 (P5) PMOD_A_IO5 (P7)	1.8 or 3.3 V GPIO
35	GND	Ground	36	GND	Ground
37	VSUP3	Voltage supply 3	38	USER_LED2 (P5) PMOD_A_IO6 (P7)	1.8 or 3.3 V GPIO
39	GPIOT_RXN16 (P5) GPIOT_RXN15 (P7)	1.8 or 3.3 V GPIO	40	USER_LED3 (P5) PMOD_A_IO7 (P7)	1.8 or 3.3 V GPIO

Header J1 (12 V Power)

J1 is a 12 V DC power supply input jack. J1 supplies power to regulators on the board that power the T120F324I4 FPGA. The maximum current supply to this input jack is 10 A.

Header J2 and J3

J2 and J3 are a 6-pin headers used to select the voltage supply for banks 1B and 1C (J2) and bank 2F (J3). By default, the jumpers connect pin 1 and 2, which is 3.3 V. Connect the jumpers as shown in the following table to change the voltages..

Jumper	VCCIO1B_1C (J2)	VCCIO2F (J3)
Connect pins 1 and 2	3.3 V (default)	3.3 V (default)
Connect pins 3 and 4	2.5 V	2.5 V
Connect pins 5 and 6	1.8 V	1.8 V

Warning: For J2 and J3, only select one voltage at a time; otherwise you may damage the board.

Header J4, J5, and J6 (Power Select)

J4, J5, and J6 are headers you use to select the voltage and/or power up sequence option. Use a jumper across 2 pins to make your selection.

- J4 controls the voltage (5.0, 3.3, and 2.8) for the 4 MIPI headers and 2 LVDS headers
- J5 controls the voltage (3.3 and 1.8) for the 4 MIPI headers and 2 LVDS headers
- J6 controls the voltage (1.2) for the four MIPI headers

Table 10: Voltage Selection for J4, J5, and J6

Jumper	VSUP1 (J4)	VSUP2 (J5)	VSUP3 (J6)
Connect pins 1 and 2	5.0 V	3.3 V	1.2 V
Connect pins 3 and 4	3.3 V	1.8 V	1.2 V with power up sequence (default)
Connect pins 5 and 6	3.3 V with power up sequence	1.8 V with power up sequence (default)	–
Connect pins 7 and 8	2.8 V	–	–
Connect pins 9 and 10	2.8 V with power up sequence (default)	–	–

Warning: For each header, only select one voltage at a time; otherwise you may damage the board.

Header J7 (SPI)

J7 is a SPI interface that you can use to configure the on-board NOR flash or T120F324I4 FPGA.

Table 11: J7 Pin Assignments

Pin Number	Signal Name	Description	T120F324I4 Pin Name
1	CCK	SPI configuration clock	GPIOL_01_CCK
2	CRESET_N	Configuration reset pin (active low)	CRESET_N
3	CDI0	SPI serial data output	GPIOL_08_CDI0
4	CONDONE	Configuration done status pin	CDONE
5	CDI1	SPI serial data input	GPIOL_09_CDI1
6	HOLD	SPI hold pin (active low)	–
7	SS	SPI slave select pin (active low)	GPIOL_00_SS
8	3V3	3.3 V power supply	–
9	FTDI_RST	Reset pin for on board FTDI FT2232 chipset (active low)	–
10	GND	Ground	–

Header J8 (JTAG)

Headers J8 is the JTAG interfaces for configuration or boundary scan testing.

Table 12: J8 Pin Assignments

Pin Number	Signal Name	Description
1	TDO	JTAG data output signal
2	3.3V	3.3 V power supply
3	TCK	JTAG data clock
4	TDI	JTAG data input
5	TMS	JTAG TMS mode select
6	FTDI_RST	Reset pin for on-board FTDI FT2232 module (active low)
7	SS	Slave select signal
8	CRESET_N	Configuration reset pin (active low)
9	GND	Ground
10	GND	Ground

Header J10 (Clock and PLL Input Select)

J10 is a 3-pin header used to select the source for the T120F324I4 clock input and PLL input. Drive a 3.3 V clock source input into the SMA connector, J9, if you are using the external clock source option.

Table 13: Clock Selection Pin Assignments

Pin Number	Signal	Notes
1	External clock source from SMA input J9	Connect pins 1 and 2 to select the SMA input
2	GPIOR_188_PLLIN2	
3	10 MHz on-board oscillator	Connect pins 2 and 3 to select the oscillator (default)

Header J11 (Raspberry Pi)

J11 is a 40-pin connector that is compatible with Raspberry Pi computers. It connects to GPIO pins in banks 1C, 1D, and 3D.

Note: J11 is located on the bottom of the board.

Table 14: J11 Pin Assignments

Pin Number	Signal Name	T120F324I4 Pin Name	Pin Number	Signal Name	T120F324I4 Pin Name
1	3.3 V	3.3 V supply	2	5.0 V	5.0 V supply
3	GPIOT_RXP18	GPIOT_RXP18	4	5.0 V	5.0 V supply
5	GPIOT_RXN18	GPIOT_RXN18	6	GND	Ground
7	GPIOR_168	GPIOR_168	8	GPIOT_RXP17	GPIOT_RXP17
9	GND	Ground	10	GPIOT_RXN17	GPIOT_RXN17
11	GPIOT_RXN14	GPIOT_RXN14	12	NC	No connect
13, 15	NC	No connect	14	GND	Ground
17	3.3 V	3.3 V Supply	16, 18	NC	No connect
19	GPIOT_RXP16	GPIOT_RXP16	20	GND	Ground
21	GPIOT_RXN16	GPIOT_RXN16	22	NC	No connect
23	GPIOR_187	GPIOR_187	24	GPIOT_RXP15	GPIOT_RXP15
25	GND	Ground	26	GPIOT_RXN15	GPIOT_RXN15
27, 29, 31, 33, 35, 37	NC	No connect	30, 34	GND	Ground
39	GND	Ground	28, 32, 36, 38, 40	NC	No connect

Headers J12 and J13 (PMOD)

J12 and J13 are 12-pin sockets for connecting to peripheral modules (PMODs) such as ADC, DAC, audio, WiFi, Bluetooth, etc. These interfaces support PMOD type 1, 2, 2A, 3, 4, 4A, 5 and 6. You can choose between 1.8 V, 2.5 V, and 3.3 V for these sockets.

Table 15: J12 Pin Assignments

Pin Number	Signal Name	T120F324I4 Pin Name	Pin Number	Signal Name	T120F324I4 Pin Name
1	PMOD_A_IO0	GPIOT_RXP20	7	PMOD_A_IO1	GPIOT_RXN20
2	PMOD_A_IO2	GPIOT_RXP21	8	PMOD_A_IO3	GPIOT_RXN21
3	PMOD_A_IO4	GPIOT_RXP22	9	PMOD_A_IO5	GPIOT_RXN22
4	PMOD_A_IO6	GPIOT_RXP23	10	PMOD_A_IO7	GPIOT_RXN23
5	Ground	GND	11	Ground	GND
6	VCC	3.3 V	12	VCC	3.3 V

Table 16: J13 Pin Assignments

Pin Number	Signal Name	T120F324I4 Pin Name	Pin Number	Signal Name	T120F324I4 Pin Name
1	USER_LED0	GPIOT_RXP24	7	USER_DIP0	GPIOT_RXP28
2	USER_LED1	GPIOT_RXN24	8	USER_DIP1	GPIOT_RXN28
3	USER_LED2	GPIOT_RXP27	9	USER_SWITCH0	GPIOT_RXP29
4	USER_LED3	GPIOT_RXN27	10	USER_SWITCH1	GPIOT_RXN29
5	Ground	GND	11	Ground	GND
6	VCC	3.3 V	12	VCC	3.3 V

Header J14 (USB Connector)

J14, a micro-USB type B socket, is the interface between the board and your computer for communication. Connect the micro-USB cable for configuring T120F324I4 FPGA and NOR flash. The board supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode.

Note: The USB cable cannot power the board.

Header J15 (RJ-45 Ethernet)

The board has a Gigabit Ethernet transceivers from Davicom (part number: DM9119INP, which is compliant with IEEE Std. 802.33 MAC and IEEE STD. 802.3I 1000BASE-TX/100BASE-TX/10BASE-T. The chip supports:

- Reduced Gigabit Media Independent Interface (RGMII) to the MAC controller
- Standard unshielded twisted pair (UTP) CAT6, CAT5e, CAT5, CAT3 cable (10 Mbps only)
- Auto-negotiation with auto MDI/MDI crossover correction, auto polarity correction, and power down mode
- Advanced DSP for baseline wander correction, equalization, echo, and crosstalk cancellation

The Ethernet transceiver U18 is set to address 0x03H.

Table 17: J15 (Ethernet) Pin Assignments

Signal Name	Pin Name	T120F324I4 Pin Name	Description
ETH_GTXCLK	GTXCLK	GPIOL_72	GMII transmit clock
ETH_TXEN	TXEN	GPIOT_RXP11	GMII/MII transmit enable
ETH_TXD3	TXD[3]	GPIOR_178	GMII and MII transmit data
ETH_TXD2	TXD[2]	GPIOR_183	GMII and MII transmit data
ETH_TXD1	TXD[1]	GPIOR_174	GMII and MII transmit data
ETH_TXD0	TXD[0]	GPIOR_173	GMII and MII transmit data
ETH_RXC	RXC	GPIOL_73	GMII and MII receive clock
ETH_RXDV	RXDV/AD[2]	GPIOT_RXP12	GMII and MII receive data valid
ETH_RXD3	RXD[3]/AN[1]	GPIOL_75	GMII and MII receive data
ETH_RXD2	RXD[2]/AN[0]	GPIOL_17	GMII and MII receive data
ETH_RXD1	RXD[1]/TXDLY	GPIOL_63	GMII and MII receive data
ETH_RXD0	RXD[0]/AD[3]	GPIOL_62	GMII and MII receive data
ETH_RSTN	RSTN	GPIOT_RXN13	Global reset input; active-low to reset the entire chip
ETH_MDC	MDC	GPIOT_RXN12	Serial clock line
ETH_MDIO	MDIO	GPIOT_RXP13	Serial data line
ETH_IRQ	IRQ	GPIOT_RXN11	Interrupt to MAC

Header J16 (HDMI)

J16 is an HDMI connector that outputs video through the on-board LVDS HDMI transmitter from ITE Tech. Inc. (part number: IT6263N). The IT6263 is a high-performance, single-chip De-SSC LVDS to HDMI converter. It supports HDMI v1.4a standard with resolutions up to 1080p with UXGA and 10-bit deep colors. The HDMI transmitter I/O pins are connected to banks 2E, 4E and 4F. The HDMI device is set to address 0x98, and you can access it through the I^2C interface.

Table 18: J16 HDMI Pin Assignments

Signal Name	Pin Name	T120F324I4 Pin Name	Description
HDMI_RESET	SYSRSTN	GPIOT_RXP14	Hardware reset pin. Active Low
HDMI_RXPCLK	RXPCLK	GPIOB_TXP09	LVDS positive clock input
HDMI_RXNCLK	RXNCLK	GPIOB_TXN09	LVDS negative clock input
HDMI_RXPA1	RXPA1	GPIOB_TXP10	LVDS first link positive input
HDMI_RXNA1	RXNA1	GPIOB_TXN10	LVDS first link negative input
HDMI_RXPB1	RXPB1	GPIOB_TXP11	LVDS first link positive input
HDMI_RXNB1	RXNB1	GPIOB_TXN11	LVDS first link negative input
HDMI_RXPC1	RXPC1	GPIOB_TXP12	LVDS first link positive input
HDMI_RXNC1	RXNC1	GPIOB_TXN12	LVDS first link negative input
HDMI_RXPD1	RXPD1	GPIOB_TXP13	LVDS first link positive input
HDMI_RXND1	RXND1	GPIOB_TXN13	LVDS first link negative input
HDMI_RXPE1	RXPE1	GPIOB_TXP14	LVDS first link positive input
HDMI_RXNE1	RXNE1	GPIOB_TXN14	LVDS first link negative input
HDMI_RXPA2	RXPA2	GPIOB_TXP15	LVDS second link positive input
HDMI_RXNA2	RXNA2	GPIOB_TXN15	LVDS second link negative input
HDMI_RXPB2	RXPB2	GPIOB_TXP16	LVDS second link positive input
HDMI_RXNB2	RXNB2	GPIOB_TXN16	LVDS second link negative input
HDMI_RXPC2	RXPC2	GPIOB_TXP17	LVDS second link positive input
HDMI_RXNC2	RXNC2	GPIOB_TXN17	LVDS second link negative input
HDMI_RXPD2	RXPD2	GPIOB_TXP18	LVDS second link positive input
HDMI_RXND2	RXND2	GPIOB_TXN18	LVDS second link negative input
HDMI_RXPE2	RXPE2	GPIOB_TXP19	LVDS second link positive input
HDMI_RXNE2	RXNE2	GPIOB_TXN19	LVDS second link negative input
HDMI_PCSCL	PCSCL	GPIOT_RXP19	Serial programming clock for chip programming
HDMI_PCSDA	PCSDA	GPIOT_RXN19	Serial programming data for chip programming

User Outputs

The board has 4 green user LEDs that are connected to I/O pins in T120F324I4 banks 2F. By default, the T120F324I4 I/O connected to these LEDs are set as active high. To turn a given LED on, pull the corresponding I/O signal high.

Note: When adding these GPIO in the Efinity® Interface Designer, configure them as output pins.

Table 19: User Outputs

Reference Designator	Schematic Name	T120F324I4 Pin Name	Active
D7	USER_LED0	GPIOT_RXP24	High
D8	USER_LED1	GPIOT_RXN24	High
D9	USER_LED2	GPIOT_RXP27	High
D10	USER_LED3	GPIOT_RXN27	High

User Inputs

The board has 2 pushbutton switches and 2 DIP switches that you can use as inputs to the T120F324I4 device. The T120F324I4 bank 2F I/O signals connect to T120F324I4 pins to control the functionality. When building designs using this switches, turn on an internal pull up for these pins in the Interface Designer.

When you press the pushbutton switches the signal drives low, indicating user input. Turning the DIP switch to the on position drives the signal low.

Table 20: User Pushbuttons

Reference Designator	Schematic Name	T120F324I4 Pin Name	Active
SW6	USER_SWITCH0	GPIOT_RXP29	Low
SW7	USER_SWITCH1	GPIOT_RXN29	Low

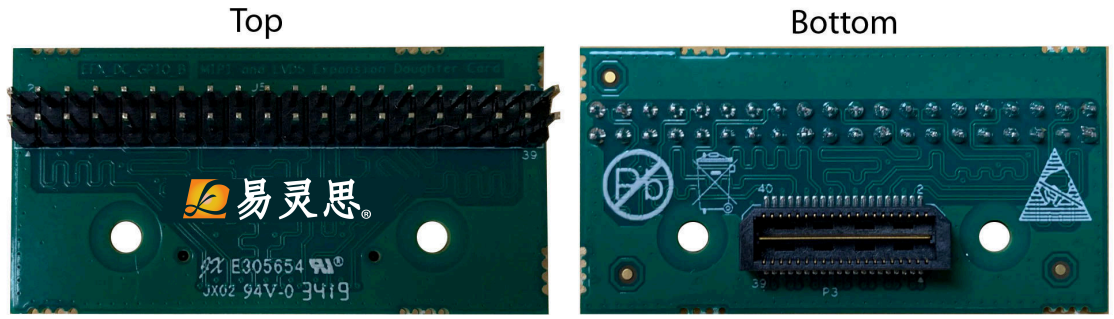
Table 21: User DIP Switches

Reference Designator	Schematic Name	T120F324I4 Pin Name	Active
SW5.1	USER_DIP0	GPIOT_RXP28	Low
SW5.2	USER_DIP1	GPIOT_RXN28	Low

MIPI and LVDS Expansion Daughter Card

The MIPI and LVDS Expansion Daughter Card (part number: EFX_DC_GPIO_B) converts the signals from the development board's QSE header.

Figure 4: MIPI and LVDS Expansion Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin MIPI or LVDS interfaces on the development board to a 40-pin male header
- Power supplied from the development board; no external power required
  - Each pin supports up to 3 A

Headers

Table 22: MIPI and LVDS Expansion Daughter Card Headers

Reference Designator	Description
P3	40-pin QTE header bringing MIPI or LVDS signals, power, and 1.8 V GPIO pins from the development board.
J5	40-pin male header.

Headers P3 (QTE Connector) and J5 (40-Pin Male Header)

P3 is a 40-pin QTE header to connect the daughter card to the QSE header on the development board. J5 is a 40-pin male header.

Table 23: QTE Connector (P3) and Expansion Prototype Connector (J5)

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO_H01	User I/O	2	GPIO_H02	User I/O
3	GPIO_H03	User I/O	4	GPIO_H04	User I/O
5	GND	Ground	6	GND	Ground
7	GPIO_H07	User I/O	8	GPIO_H08	User I/O
9	GPIO_H09	User I/O	10	GPIO_H10	User I/O
11	GND	Ground	12	GND	Ground
13	GPIO_H13	User I/O	14	GPIO_H14	User I/O
15	GPIO_H15	User I/O	16	GPIO_H16	User I/O
17	GND	Ground	18	GND	Ground
19	GPIO_H19	User I/O	20	GPIO_H20	User I/O
21	GPIO_H21	User I/O	22	GPIO_H22	User I/O
23	GND	Ground	24	GND	Ground
25	GPIO_H25	User I/O	26	GPIO_H26	User I/O
27	GPIO_H27	User I/O	28	GPIO_H28	User I/O
29	GND	Ground	30	GND	Ground
31	GPIO_H31	User I/O	32	GPIO_H32	User I/O
33	GPIO_H33	User I/O	34	GPIO_H34	User I/O
35	GND	Ground	36	GND	Ground
37	GPIO_H37	User I/O	38	GPIO_H38	User I/O
39	GPIO_H39	User I/O	40	GPIO_H40	User I/O

Signal Mapping

MIPI Signal Mapping

This table shows the pin mapping from the MIPI headers (P4, P5, P6, and P7) to the daughter card headers.

Table 24: MIPI Signal Mapping

Where x is 0 or 1 and y is TXD or RXD

Pin Number	Daughter Card Pin	MIPI Pin	Pin Number	Daughter Card Pin	MIPI Pin
1	GPIO_H01	VSUP1	2	GPIO_H02	MIPI*x_y*_P0
3	GPIO_H03	VSUP2	4	GPIO_H04	MIPI*x_y*_N0
5	GND	GND	6	GND	GND
7	NC	No Connect	8	GPIO_H08	MIPI*x_y*_P1
9	NC		10	GPIO_H10	MIPI*x_y*_N1
11	GND	GND	12	GND	GND
13	NC	No Connect	14	GPIO_H14	MIPI*x_y*_P2
15	NC		16	GPIO_H16	MIPI*x_y*_N2
17	GND	GND	18	GND	GND
19	NC	No Connect	20	GPIO_H20	MIPI*x_y*_P3
21	NC		22	GPIO_H22	MIPI*x_y*_N3
23	GND	GND	24	GND	GND
25	NC	No Connect	26	GPIO_H26	MIPI*x_y*_P4
27	NC		28	GPIO_H28	MIPI*x_y*_N4
29	GND	GND	30	GND	GND
31	NC	No Connect	32	GPIO_H32	USER_SWITCH0 (P4) USER_LED0 (P5) PMOD_A_IO0 (P6) PMOD_A_IO4 (P7)
33	NC		34	GPIO_H34	USER_SWITCH1 (P4) USER_LED1 (P5) PMOD_A_IO1 (P6) PMOD_A_IO5 (P7)
35	GND	GND	36	GND	GND
37	GPIO_H37	VSUP3	38	GPIO_H38	USER_DIP0 (P4) USER_LED2 (P5) PMOD_A_IO2 (P6) PMOD_A_IO6 (P7)
39	GPIO_H39	GPIOT_RXP16 (P4) GPIOT_RXN16 (P5) GPIOT_RXP15 (P6) GPIOT_RXN15 (P7)	40	GPIO_H40	USER_DIP1 (P4) USER_LED3 (P5) PMOD_A_IO3 (P6) PMOD_A_IO7 (P7)

LVDS Signal Mapping

This table shows the pin mapping from the LVDS headers (P2 and P3) to the daughter card headers.

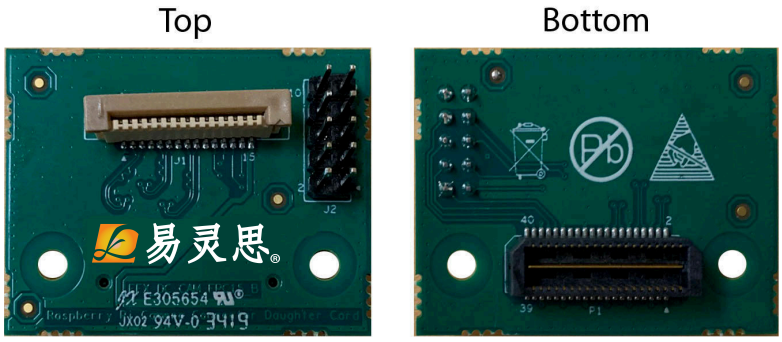
Table 25: LVDS Signal Mapping

Pin #	Daughter Card Pin	LVDS P2 Pin	LVDS P3 Pin	Pin #	Daughter Card Pin	LVDS P2 Pin	LVDS P3 Pin
1	GPIO_H01	GPIOT_RXP09 _CLKP0	GPIOB_TXP00	2	GPIO_H02	GPIOT_RXP07	GPIOB_TXP07
3	GPIO_H03	GPIOT_RXN09 _CLKN0	GPIOB_TXN00	4	GPIO_H04	GPIOT_RXN07	GPIOB_TXN07
5	GND	GND	GND	6	GND	GND	GND
7	GPIO_H07	GPIOT_RXP01	GPIOB_TXP01	8	GPIO_H08	GPIOT_RXP08	GPIOB_TXP08
9	GPIO_H09	GPIOT_RXN01	GPIOB_TXN01	10	GPIO_H10	GPIOT_RXN08	GPIOB_TXN08
11	GND	GND	GND	12	GND	GND	GND
13	GPIO_H13	GPIOT_RXP02	GPIOB_TXP02	14	GPIO_H14	NC	NC
15	GPIO_H15	GPIOT_RXN02	GPIOB_TXN02	16	GPIO_H16	NC	NC
17	GND	GND	GND	18	GND	GND	GND
19	GPIO_H19	GPIOT_RXP03	GPIOB_TXP03	20	GPIO_H20	NC	NC
21	GPIO_H21	GPIOT_RXN03	GPIOB_TXN03	22	GPIO_H22	NC	NC
23	GND	GND	GND	24	GND	GND	GND
25	GPIO_H25	GPIOT_RXP04	GPIOB_TXP04	26	GPIO_H26	NC	NC
27	GPIO_H27	GPIOT_RXN04	GPIOB_TXN04	28	GPIO_H28	NC	NC
29	GND	GND	GND	30	GND	GND	GND
31	GPIO_H31	GPIOT_RXP05	GPIOB_TXP05	32	GPIO_H32	NC	NC
33	GPIO_H33	GPIOT_RXN05	GPIOB_TXN05	34	GPIO_H34	NC	NC
35	GND	GND	GND	36	GND	GND	GND
37	GPIO_H37	GPIOT_RXP06	GPIOB_TXP06	38	GPIO_H38	NC	NC
39	GPIO_H39	GPIOT_RXN06	GPIOB_TXN06	40	GPIO_H40	NC	NC

Raspberry Pi Camera Connector Daughter Card

The kit includes the Raspberry Pi Camera Connector Daughter Card (part number: EFX_DC_CAM_FPC15_B), which bridges between the Trion® T120 BGA324 Development Board and a Raspberry Pi camera module. The daughter card connects to a Raspberry Pi computer or any Raspberry Pi camera using a 15 pin flat cable. Additionally, the board has a 10 pin header for optional camera control pins.

Figure 5: Raspberry Pi Camera Connector Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin MIPI CSI-2 interface on a Trion® T120 BGA324 Development Board to a 15-pin interface
- Pin to pin compatible with Raspberry Pi cameras
- Supports up to 1.5 Gbps on MIPI interface
- User selectable pins for optional camera functions
- Power supplied from the Trion® T120 BGA324 Development Board; no external power required; each pin supports up to 3 A

Note: For technical support using Raspberry Pi cameras, please refer to their web site at www.raspberrypi.org.

Headers

Table 26: Raspberry Pi Camera Connector Daughter Card Headers

Reference Designator	Description
P1	40-pin QTE header bringing MIPI signals, power, and 1.8 V GPIO pins from the Trion® T120 BGA324 Development Board.
J1	15-pin flexible printed cable (FPC) connector for Raspberry Pi MIPI camera modules.
J2	10-pin header for optional Raspberry Pi MIPI camera module signals.

Header P1 (Development Board Connector)

P1 is a 40-pin QTE header to connect the daughter card to the Trion® T120 BGA324 Development Board. The header provides MIPI signals and power to the camera module.

- *Raspberry Pi computer*—When using this daughter card with a Raspberry Pi computer, connect header P1 to a MIPI TX socket on the development board.
- *Raspberry Pi camera*—When using this daughter card with a Raspberry Pi camera, connect header P1 to a MIPI RX socket on the development board.

Note: See **Attaching Camera Connector Daughter Cards** on page 33 for details.

Table 27: Development Board Connector (P1)

where *n* is RXD or TXD, depending on whether you are connecting to a camera or Raspberry Pi computer.

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	3V3_15FPC	3.3V Supply	2	MIPI_P0_15FPC	Differential MIPI lane 0
3	NC	No connect	4	MIPI_N0_15FPC	
5	GND	Ground	6	GND	Ground
7	NC	No connect	8	MIPI_P1_15FPC	Differential MIPI lane 1
9	NC		10	MIPI_N1_15FPC	
11	GND	Ground	12	GND	Ground
13	NC	No connect	14	MIPI_P2_15FPC	Differential MIPI lane 2
15	NC		16	MIPI_N2_15FPC	
17	GND	Ground	18	GND	Ground
19	NC	No connect	20	NC	No connect
21	NC		22	NC	
23	GND	Ground	24	GND	Ground
25	NC	No connect	26	NC	No connect
27	NC		28	NC	
29	GND	Ground	30	GND	Ground
31	NC	No connect	32	GPIO0	1.8 V GPIO
33	NC		34	GPIO1	1.8 V GPIO
35	GND	Ground	36	GND	Ground
37	NC	No connect	38	GPIO2	1.8 V GPIO
39	NC		40	GPIO3	1.8 V GPIO

Header J1 (Raspberry Pi FPC15 Connector)

J1 is a 15-pin flexible flat cable header for connecting to a Raspberry Pi MIPI camera module.

- *Raspberry Pi computer*—When using this daughter card with a Raspberry Pi computer, these pins are TX.
- *Raspberry Pi camera*—When using this daughter card with a Raspberry Pi camera, these pins are RX.

Table 28: Raspberry Pi FPC15 Connector (J1)

where *n* is RXD or TXD, depending on whether you are connecting to a camera or Raspberry Pi computer.

Pin Number	Pin Name	Description
1	GND	Ground
2	MIPI_N0_15FPC	Differential MIPI lane 0
3	MIPI_P0_15FPC	
4	GND	Ground
5	MIPI_N1_15FPC	Differential MIPI lane 1
6	MIPI_P1_15FPC	
7	GND	Ground
8	MIPI_N2_15FPC	Differential MIPI lane 2
9	MIPI_P2_15FPC	
10	GND	Ground
11	GPIO2_15FPC	GPIO for Raspberry Pi MIPI camera module
12	GPIO3_15FPC	
13	GPIO0_15FPC	Serial clock for Raspberry Pi MIPI camera module
14	GPIO1_15FPC	Serial data for Raspberry Pi MIPI camera module
15	3V3_15FPC	3.3 V power supply

Header J2 (Optional Camera Signals)

The J2 header has optional pins (SCL and SDA) that are used for MIPI Camera Command Set (CSS) transactions. These signals are routed to the Trion® FPGA on the board. You can control these pins with an external device by removing the jumpers and connecting wires from the header to an external device.

Note: If you connect jumpers to any pins in J2, do not use the corresponding GPIO in your design. For example, if you use jumpers on pins 1-2 and 3-4, do not use `GPIO_69` or `GPIO_70`.

Table 29: Optional Camera Signals (J2)

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO0	1.8 V I/O from development board	2	GPIO0_15FPC	I^2C bus SCL signal
3	GPIO1		4	GPIO1_15FPC	I^2C bus SDA signal
5	GPIO2		6	GPIO2_15FPC	Camera GPIO
7	GPIO3		8	GPIO3_15FPC	Camera clock
9	GND	Ground	10	GND	Ground

Setting up the Board

Installing Standoffs

Before using the board, attach the standoffs with the screws provided in the kit.

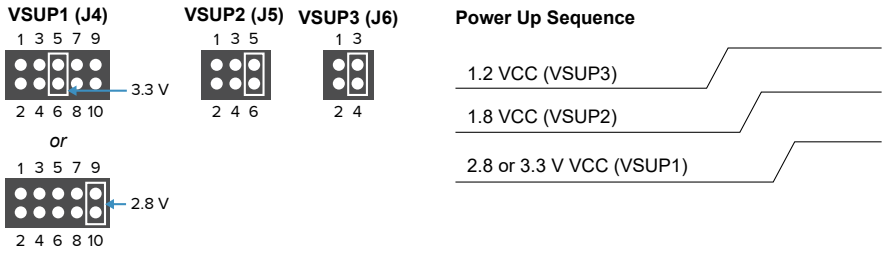
Warning: You can damage the board if you over tighten the screws. Tighten all screws to a torque between 4 ± 0.5 kgf/cm and 5 ± 0.5 kgf/cm.

Setting the Power-Up Sequence for MIPI Cameras

Trion® T120 BGA324 Development Board has a built-in power-up sequence circuit for the MIPI transmitter and receiver interfaces (P5, P6, P7, and P8) that is compatible with MIPI camera sensor power requirements. To enable the power-up sequence, you slide SW1 to position 3 and connect jumpers on the power supply headers J4, J5, and J6 for the voltages you want.

1. Remove power from the board.
2. Choose your camera voltage for VSUP1 (J4) by connecting pins 5 and 6 for 3.3 V or pins 9 and 10 for 2.8 V.
3. Connect pins 5 and 6 for VSUP2 (J5).
4. Connect pins 3 and 4 for VSUP3 (J6).
5. Slide SW1 to position 3.
6. Attach the camera connector daughter card for the camera you want to use to the board.
7. Attach the camera to the daughter card.
8. Turn on power to the board.

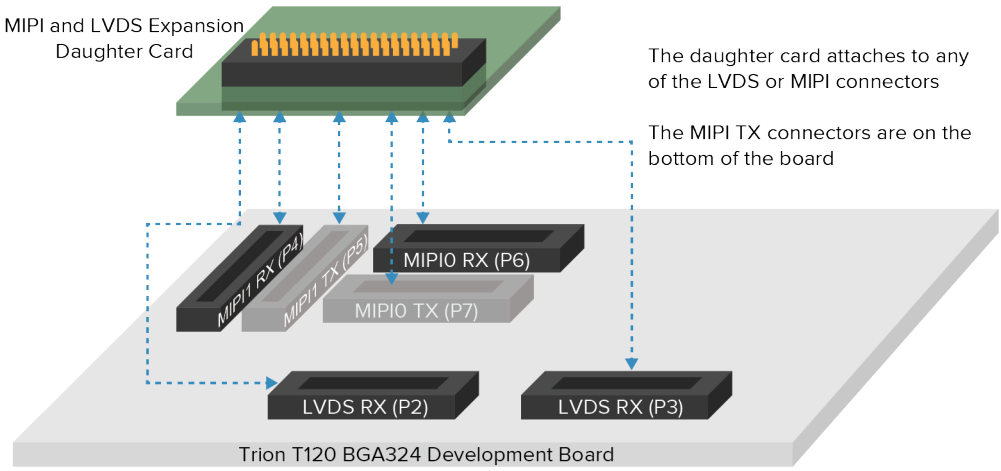
Figure 6: Setting the Power Sequence Jumpers



Attaching the MIPI and LVDS Expansion Daughter Card

The Trion® T120 BGA324 Development Board supports an expansion daughter card that fans out the GPIO.

Figure 7: Attaching MIPI and LVDS Expansion Daughter Card



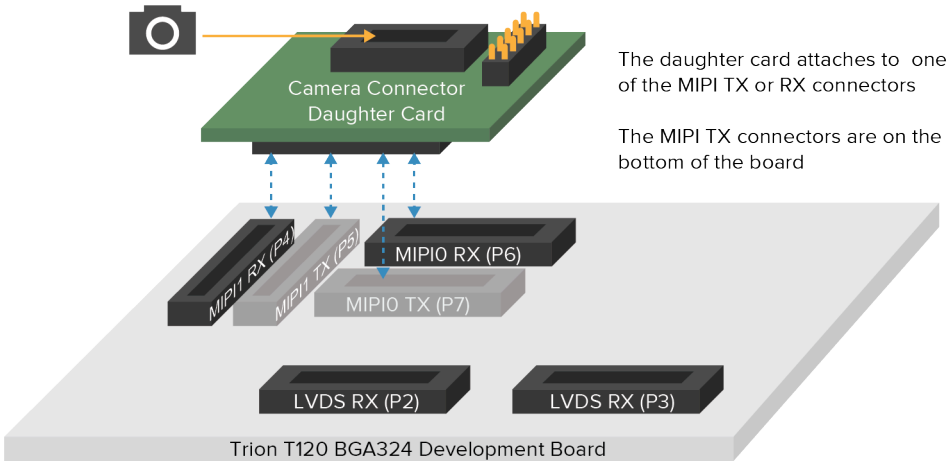
To connect the daughter card:

1. Remove power from the Trion® T120 BGA324 Development Board.
2. Attach standoffs to the MIPI and LVDS Expansion Daughter Card.
3. Attach the MIPI and LVDS Expansion Daughter Card to one of the LVDS or MIPImulti-purpose high-speed interface 40-pin headers on the Trion® T120 BGA324 Development Board.
4. Connect any cables to the GPIO as needed for your application.
5. Power up the Trion® T120 BGA324 Development Board.

Attaching Camera Connector Daughter Cards

The camera connector daughter card attaches to the high-speed MIPI TX or RX headers.

Figure 8: Attaching Camera Connector Daughter Cards (T120 BGA324 Board)



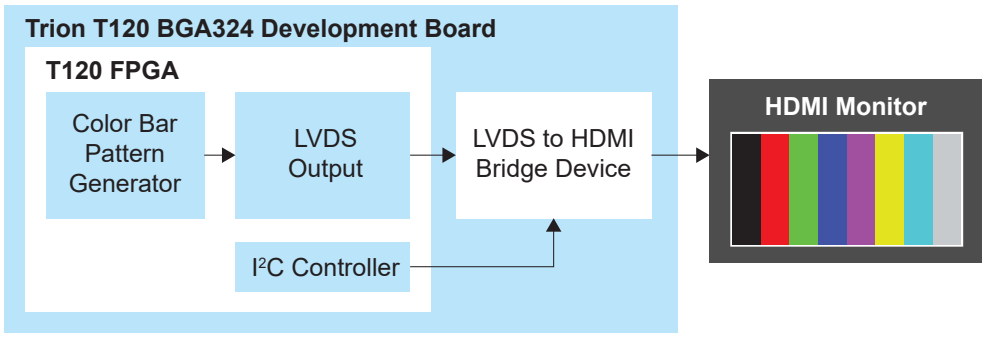
To connect a daughter card:

1. Remove power from the Trion® T120 BGA324 Development Board.
2. Attach standoffs to the daughter card.
3. Attach the daughter card to the 40-pin header on the board.
4. Connect the camera module or computer to the daughter card using a ribbon cable.
5. Power up the board.

Running the Example Design

易灵思® preloads the Trion® T120 BGA324 Development Board with a simple example design that sends color bars to an HDMI monitor at 1080p resolution. The T120 FPGA generates an 8-color bar pattern, sends it to the LVDS-to-HDMI device on the board, and then to the HDMI monitor for display.

Figure 9: HDMI Color Bar Design Block Diagram



The example design uses the following hardware:

- Trion® T120 BGA324 Development Board
- 1080p monitor with HDMI connector
- HDMI cable
- 12 V power adapter

Set Up the Hardware

1. Attach standoffs to the board.
2. Use a jumper to connect pins 2 and 3 on J10 to enable the on-board 10 MHz oscillator.
3. Connect the HDMI cable to the HDMI connector and to an HDMI-compatible monitor.
4. Connect the 12 V power cable to the board connector and to a power source.
5. Turn on the board's power switch.

Run the Example Design

After the FPGA configures, it outputs the color bars to the monitor.

The designs includes the **it6263_reg.mem** file that contains the register mapping for the 1080p resolution. To use a different resolution, modify the register map file. Each line represents the MSB or data.

- Line 1 is the the MSB of the 8 bit register.
- Line 2 is the data.
- Line 3 is the MSB of the next register, and so on

For example:

```
05
40
04
3D
04
1D
```

Lines 1 and 2 refer to register 05 and data 40.

Lines 5 and 6 refer to register 04 and data 1D.

Creating Your Own Design

The Trion® T120 BGA324 Development Board allows you to create and explore designs for the T120 device. 易灵思® provides example code and designs to help you get started:

- Our Support Center (**www.elitestek.com/support**) includes examples targeting the board.
- The Efinity software includes also example designs that you can use as a starting point for your own project, and includes a step-by-step tutorial.
- **AN 027: Using the Raspberry Pi to HDMI Example Designs (T120 BGA576)** includes example designs with additional features for Trion® T120 BGA324 Development Board.

Appendix 1: Shared Resources

Some of the resources available on the Trion® T120 BGA324 Development Board are connected to more than one I/Os. You need to ensure there are no overlapping assignments when using these resources. The following table lists the resources shared by more than one I/Os. You can refer to this table to help you plan the resources available in the Trion® T120 BGA324 Development Board

Note: Resources that are not listed are only available from one I/O (see Headers on page 11).

Table 30: Trion® T120 BGA324 Development Board Shared Resources

<header name>.<pin name/number>

Resource	Connection 1	Connection 2	Connection 3
GPIOR_168	J11.7	P1.45	–
GPIOR_187	J11.23	P1.47	–
GPIOT_RXN14	J11.11	P1.49	–
GPIOT_RXN15	J11.26	P1.29	P7.39
GPIOT_RXN16	J11.21	P1.33	P5.39
GPIOT_RXN17	J11.10	P1.37	–
GPIOT_RXN18	J11.5	P1.41	–
GPIOT_RXN20	J12.7	P6.34	–
GPIOT_RXN21	J12.8	P6.40	–
GPIOT_RXN22	J12.9	P7.34	–
GPIOT_RXN23	J12.10	P7.40	–
GPIOT_RXN24	J13.2	P5.34	LED.D8
GPIOT_RXN27	J13.4	P5.40	LED.D10
GPIOT_RXN28	J13.8	P4.40	DIPswitch.SW5.2
GPIOT_RXN29	J13.10	P4.34	Pushbutton.SW7
GPIOT_RXP15	J11.24	P1.27	P6.39
GPIOT_RXP16	J11.19	P1.31	P4.39
GPIOT_RXP17	J11.8	P1.35	–
GPIOT_RXP18	J11.3	P1.39	–
GPIOT_RXP24	J13.1	P5.32	LED.D7
GPIOT_RXP27	J13.3	P5.38	LED.D9
GPIOT_RXP28	J13.7	P4.38	DIPswitch.SW5.1
GPIOT_RXP29	J13.9	P4.32	Pushbutton.SW6

Revision History

Table 31: Revision History

Date	Version	Description
September 2022	2.7	Updated Installing Windows Driver.
June 2022	2.6	Added Appendix 1: Shared resources.
December 2021	2.5	Corrected the MIPI and LVDS Expansion Card headers.
September 2021	2.4	Added USB driver installation topics. (DOC-463)
February 2021	2.3	Added note about referring to the power-up sequence in the data sheet when designing a board and recommending supervisor IC for `CRESET_N` (DOC-388).
December 2020	2.2	Corrected pin numbers in PMOD headers. (DOC-345) Added note about power cable supplied is type A plug (U.S. style). (DOC-345) Updated Raspberry Pi camera connector daughter card header pin names. (DOC-345)
July 2020	2.1	Added step to use a jumper on J10 for the example design. Renamed TR_CORNER as TR. The bank name changed in Efinity v2020.1.
June 2020	2.0	Updated P1 header pin names Corrected Gigabit Ethernet transceivers part number to DM9119INP. Corrected configuration done pin name to CDONE. Updated oscillator and clock generator sources table. Updated CBUS configuration pin description. Updated jumper settings diagram for MIPI camera power-up. Updated clock selection pin assignment table for J10.
April 2020	1.0	Initial release.