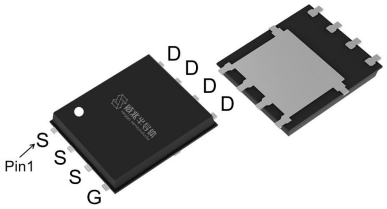
Features

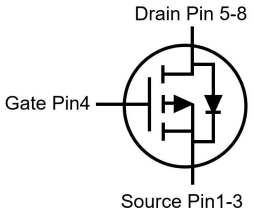
- P-Channel，-5V Logic Level Control
- Low on-resistance RDS(on) @ V_{GS}=-4.5 V
- Fast Switching
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

V_{DS}	-30	V
$R_{DS(on),TYP}$@ V_{GS}=-10 V	8.8	mΩ
$R_{DS(on),TYP}$@ V_{GS}=-4.5V	16	mΩ
I_D	-50	A

PDFN5x6



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VS3508AP	PDFN5x6	3508AP	3000pcs/reel

Maximum ratings, at T_j=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		-30	V
I_S	Diode continuous forward current	T_C=25°C	-50	A
I_D	Continuous drain current @VGS=-10V	T_C=25°C	-50	A
		T_C=100°C	-32	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	-200	A
EAS	Avalanche energy, single pulsed ②		56	mJ
P_D	Maximum power dissipation	T_C=25°C	40	W
V_{GS}	Gate-Source voltage		±20	V
T_{STG},T_J	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	30	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=-30V,V_{GS}=0V	–	–	-1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=-30V,V_{GS}=0V	–	–	-100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	–	–	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.3	-1.8	-2.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ③	V_{GS}=-10V, I_D=-20A	–	8.8	11	mΩ
$R_{DS(on)}$	Drain-Source On-State Resistance ③	V_{GS}=-4.5V, I_D=-15A	–	16	20	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=-15V,V_{GS}=0V, f=1MHz	3000	3305	3600	pF
Coss	Output Capacitance		350	395	450	pF
Crss	Reverse Transfer Capacitance		220	260	300	pF
Rg	Gate Resistance	f=1MHz	–	3.2	–	Ω
Qg	Total Gate Charge	V_{DS}=-15V,I_D=-20A, V_{GS}=-10V	–	59	–	nC
Qgs	Gate-Source Charge		–	11	–	nC
Qgd	Gate-Drain Charge		–	12	–	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=-15V, I_D=-20A, R_G=3Ω, V_{GS}=-10V	–	9.5	–	ns
Tr	Turn-on Rise Time		–	12	–	ns
Td(off)	Turn-Off Delay Time		–	51	–	ns
Tf	Turn-Off Fall Time		–	15	–	ns
Source- Drain Diode Characteristics@ T_J = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-20A,V_{GS}=0V	–	-0.9	-1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=-20A, V_{GS}=0V di/dt=-500A/μs	–	14	–	ns
Qrr	Reverse Recovery Charge		–	22	–	nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by TJmax, starting TJ = 25°C, L = 0.5mH, RG = 25Ω, IAS = -15A, VGS =-10V. Part not recommended for use above this value

③ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

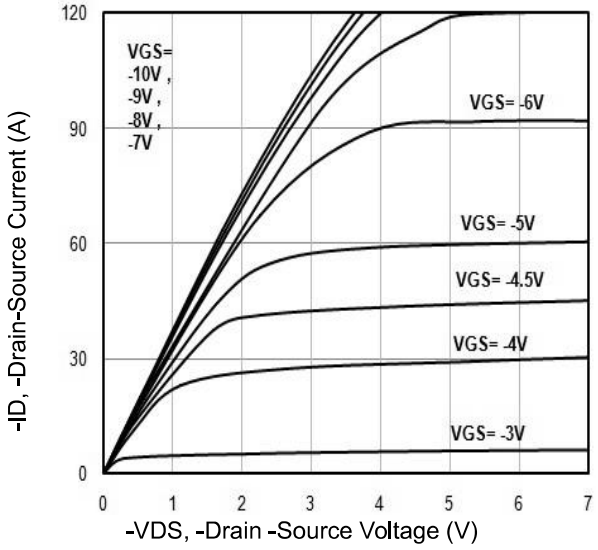


Fig1. Typical Output Characteristics

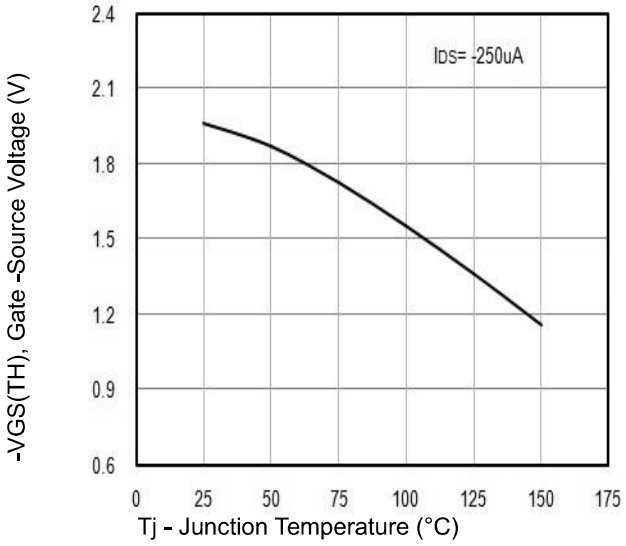


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

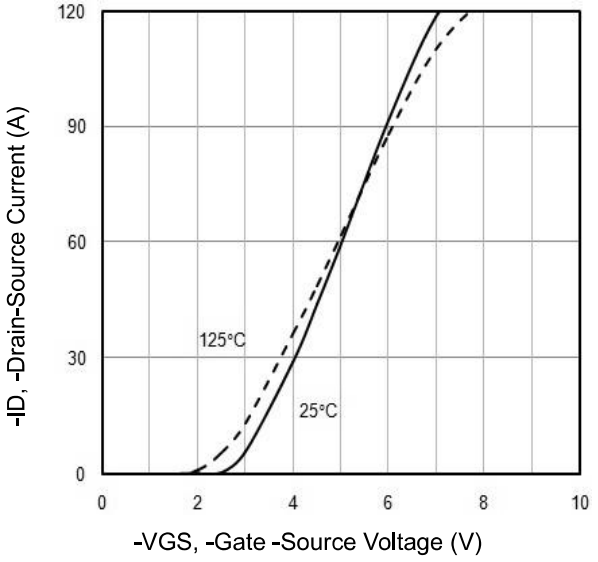


Fig3. Typical Transfer Characteristics

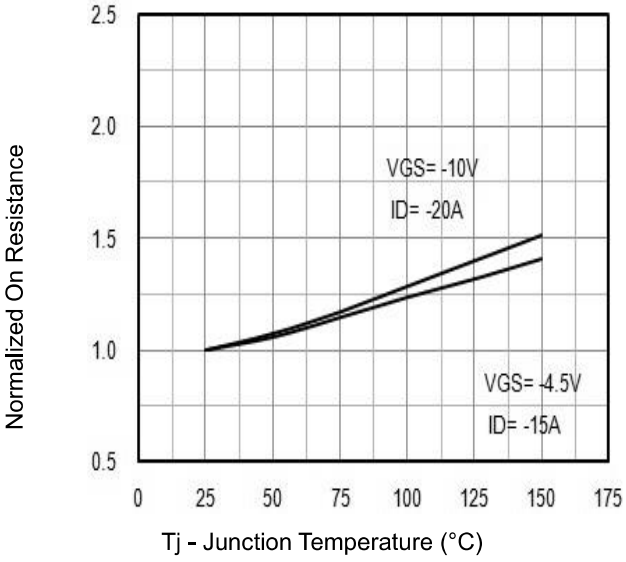


Fig4. Normalized On-Resistance Vs. Tj

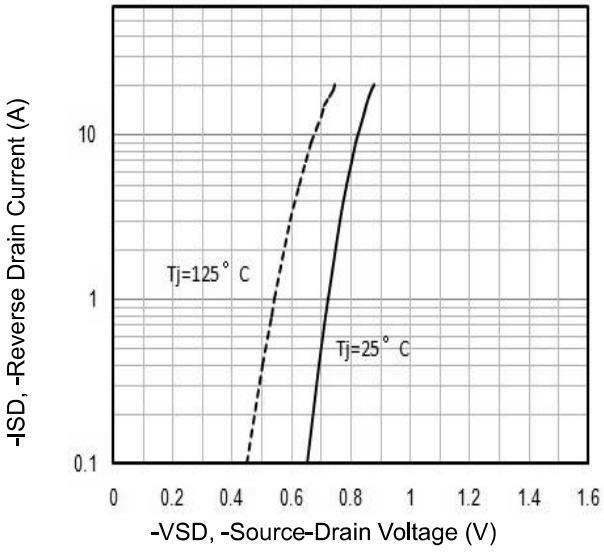


Fig5. Typical Source-Drain Diode Forward Voltage

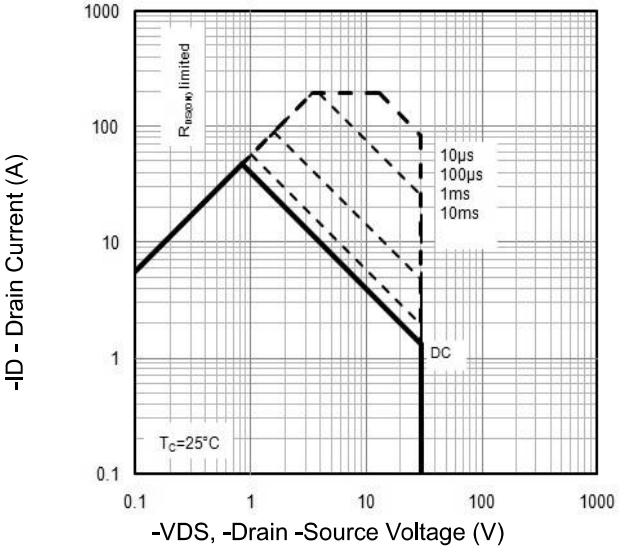


Fig6. Maximum Safe Operating Area

Typical Characteristics

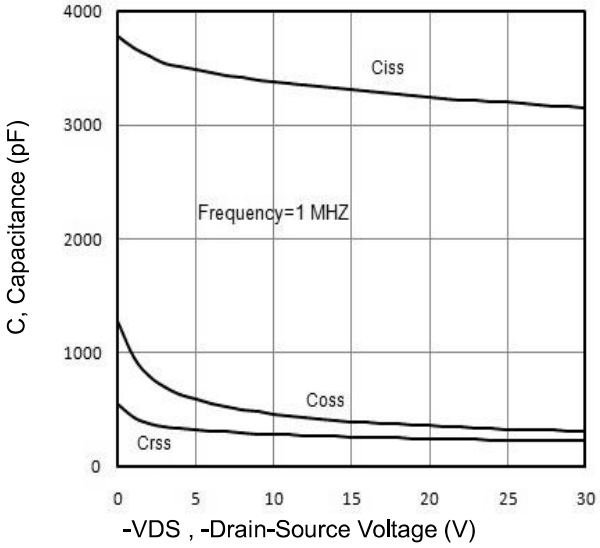


Fig7. Typical Capacitance Vs.Drain-Source Voltage

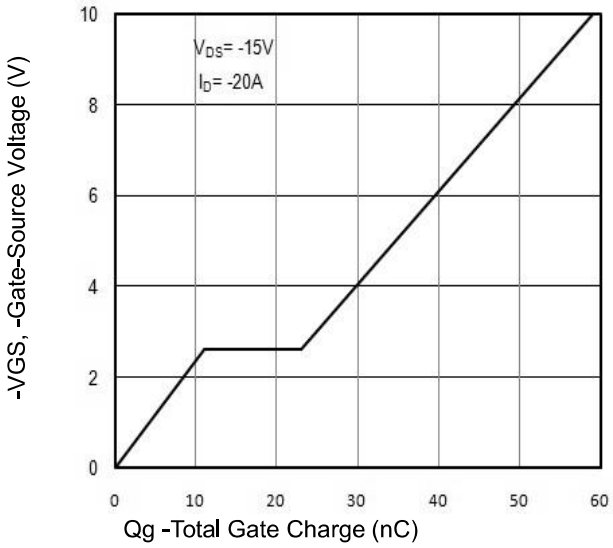


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

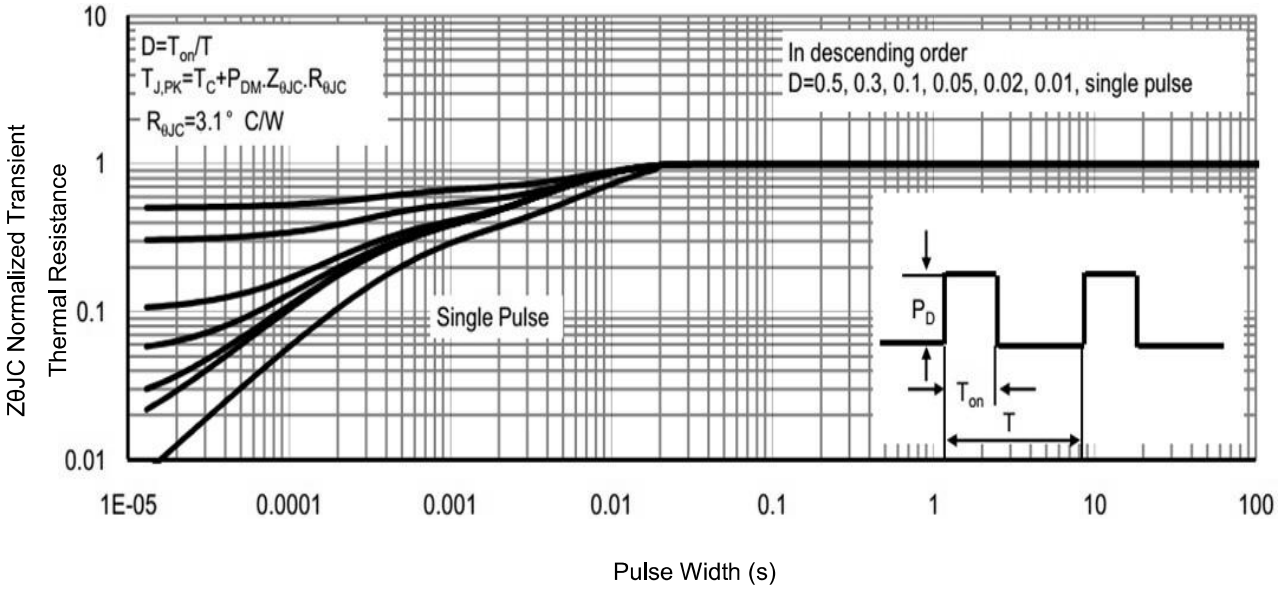


Fig9. Normalized Maximum Transient Thermal Impedance

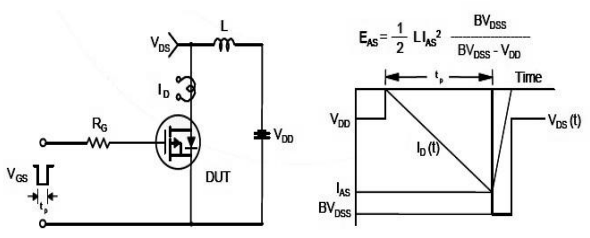


Fig10. Unclamped Inductive Test Circuit and Waveforms

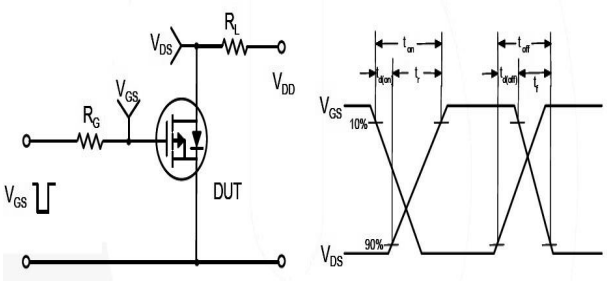
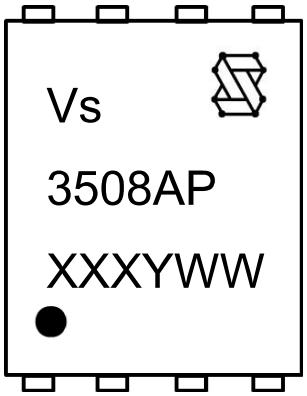


Fig11. Switching Time Test Circuit and waveforms

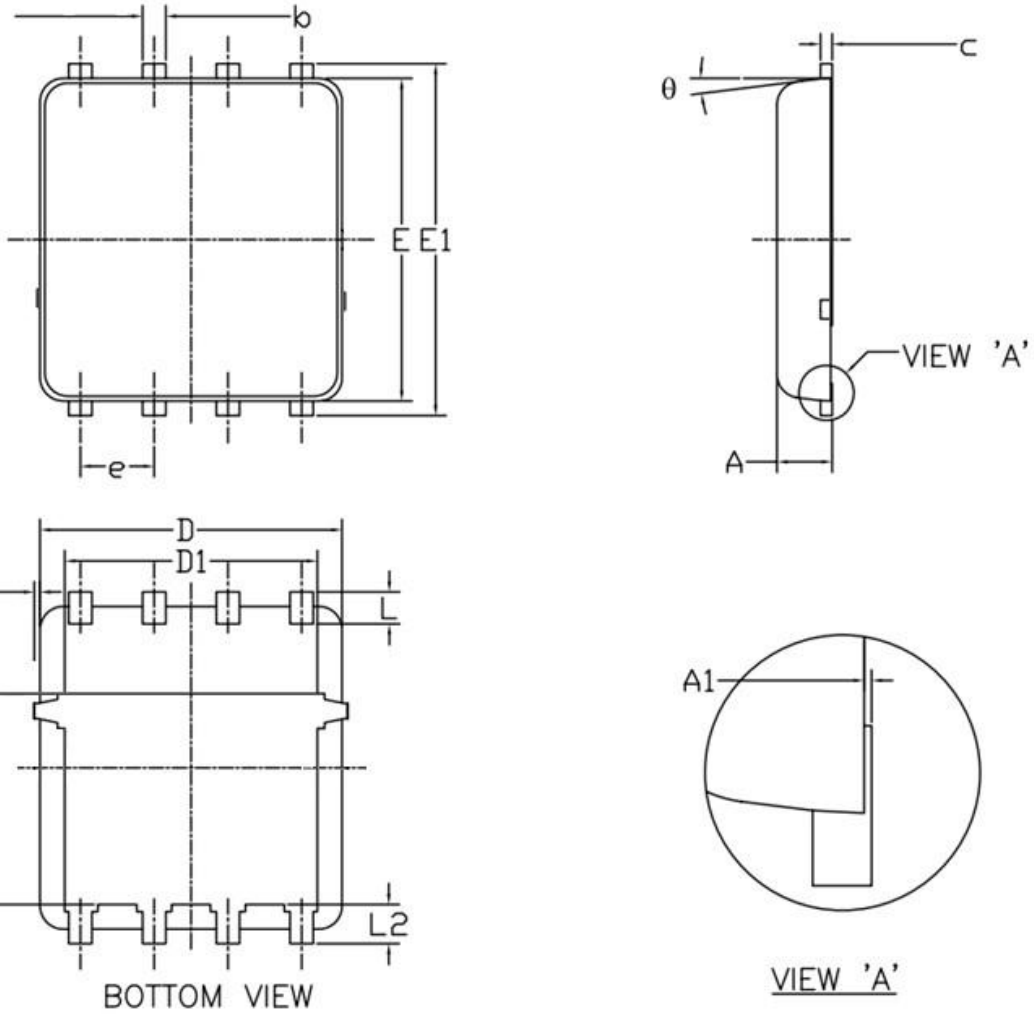
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（3508AP）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code, code changed with Lot Number
Y: Year Code，refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.