30V 1.2A Step-Down Dimmable LED Driver

Features

- Wide 8.0V to 30V Operating Input Range
- 1.2A Continuous Output Current
- Maximum 1MHz Switching Frequency
- Over Temperature Protection
- Inherent Open-Circuit LED Protection
- High-side Current Sense
- Hysteretic Control: No Compensation
- 400mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High efficiency (up to 97%)
- Adjustable Constant LED current
- PWM and Analog Dimming
- Typical 6% Output Current Accuracy
- Available in SOT89-5 Package
- -40°C to +85°C Temperature Range

Applications

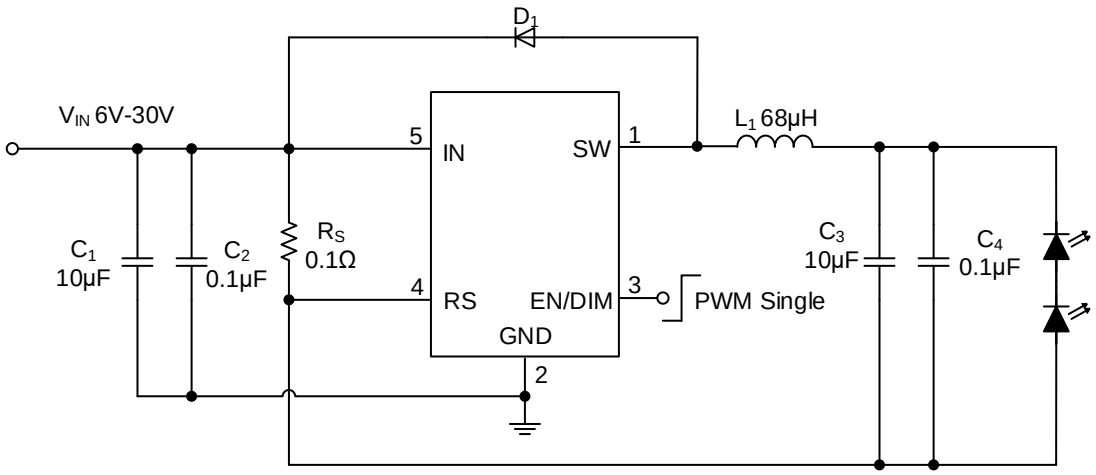
- Low voltage halogen replacement LEDs
- Automotive/Decorative LED Lighting
- Low-Voltage Halogen Replacement
- Signs/Emergency Lighting
- LED Backlighting
- SELV Lighting

General Description

The PT4115 is step-down regulator for dimmable LED driver, which is designed in continuous current mode for driving the high-brightness LEDs from a wide input voltage of 8.0V to 30V. The PT4115 employs a hysteretic control scheme to regulate LED current. Moreover, the control scheme provides optimal loop stabilization and a very quick response time. The PT4115 implements PWM and analog dimming together on the EN/DIM pin. The PT4115 includes under-voltage lockout and thermal overload protection to prevent damage in the event of an output overload.

The PT4115 requires a minimal number of readily available, external components and is available in a space saving SOT89-5 package.

Typical Application Circuit



Typical Application Circuit

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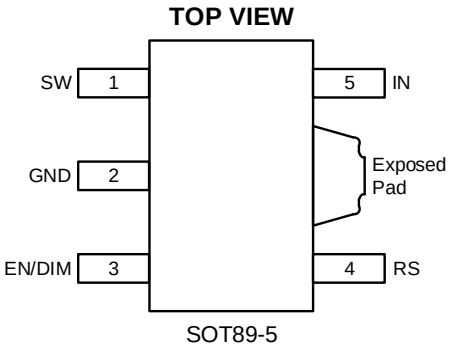
Package and Pin Description

Pin Configuration



Top Marking: PT4115 NNNNN (device code: PT4115, NNNNN= lot number code)

Pin Description

Pin	Name	Function
1	SW	Drain of Internal MOSFET. Connect the inductor common terminal and Schottky anode to this pin.
2	GND	Ground.
3	EN/DIM	Enable/Dimming Command Input. For PWM dimming, apply a square wave signal to this pin. Apply a typical value of 5V to fully turn on the chip. Turn off the output current when pulling this pin below 0.3V.
4	RS	LED Current Sense Input. Connect a current-sense resistor to program the LED average current to IN pin.
5	IN	Input Supply Pin. Connect an appropriate decoupling capacitor from the IN pin to GND.

Order Information (1)

Marking	Part No.	Model	Description	Package	T/R Qty
PT4115 NNNNN	70380012	PT4115	PT4115 dimmable LED driver IC, 30V, 1.2A, SOT89-5	SOT89-5	3000PCS

Note (1): All RYCHIP parts are Pb-Free and adhere to the RoHS directive.

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Specifications

Absolute Maximum Ratings (1)(2)

Item	Min	Max	Unit
V_{IN} voltage	-0.3	34	V
EN/DIM voltage	-0.3	6	V
SW voltage	-0.3	36	V
SW voltage (10ns transient)	-5	36	V
RS voltage	-0.3	34	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	-65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 140°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD\text{-}HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD\text{-}CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH\text{-}UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Supply Voltage V_{IN}	8.0	30	V

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

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Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	105	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1) (2)

V_{IN} = 24V, T_J =-40°C to 125°C (3), unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		8.0		30.0	V
IN UVLO Rising Threshold	V_{UVLO}	V_{IN} Rising		7.5	7.9	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			700		mV
Shutdown Supply Current	I_{SD}			150		μA
Feedback Reference Voltage (with respect to V_{IN})	V_{IN-VCS}		93	100	107	mV
EN/DIM Input High Voltage	V_{EN_HIGH}		2.7			V
EN/DIM Input Low Voltage	V_{EN_LOW}				0.35	V
EN/DIM Pull-Up Resistor	R_{EN}			200		kΩ
EN/DIM Internal Supply Voltage	V_{DIM}	EN/DIM floating		4		V
EN/DIM PWM Dimming Frequency Range	F_{DIM}		100	1K	10K	Hz
PWM Dimming Duty Cycle Range		F_{DIM}=1KHz	1		100	%
Switch On Resistance	$R_{DS\ ON}$			0.4		Ω
SW leakage current	I_{LEAK}			2	10	μA
Thermal Shutdown (4)	T_{SD}			160		°C
Thermal Hysteresis (4)	T_{HYS}			20		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

Note (3): Not test in production, guaranteed by characterization. Typical value represents the most likely parametric norm at +25°C

Note (4): Guaranteed by design

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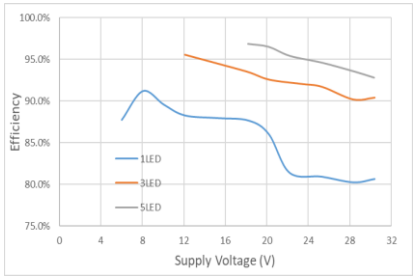
Typical Performance Characteristics (1) (2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): V_{IN} =24V, L=68μH , T_A = +25ºC, unless otherwise noted.

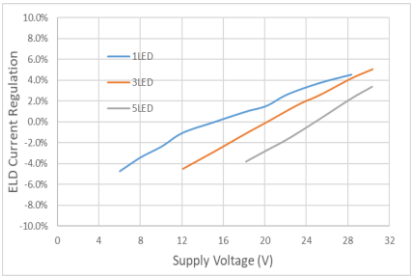
Efficiency vs. Supply Voltage

L=68μH



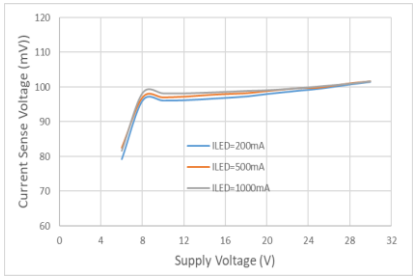
LED Current vs. Supply Voltage

I_{LED}=200mA



Current Sense Voltage vs. Supply Voltage

1 LED Series

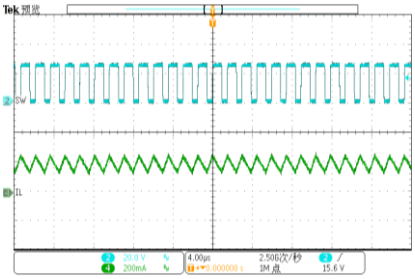


LED Current vs. PWM Duty Cycle

V_{IN}=24V, I_{LED}=1000mA, 3LEDs

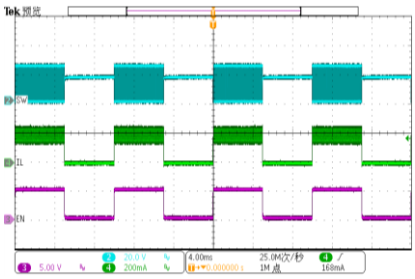
Steady State

V_{IN}=24V, I_{LED}=200mA, 3ILEDs



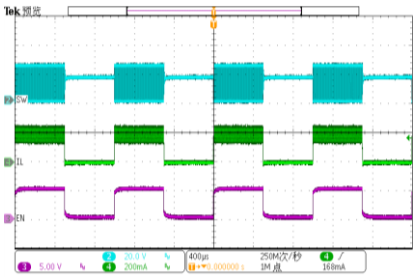
PWM Dimming

3ILEDs, F_{DIM}=100Hz, Duty Cycle=50%



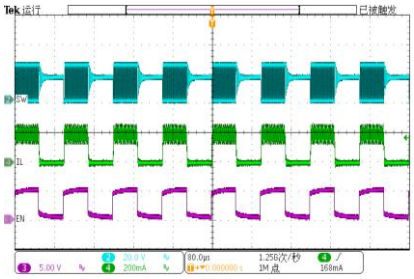
PWM Dimming

3ILEDs, F_{DIM}=1KHz, Duty Cycle=50%



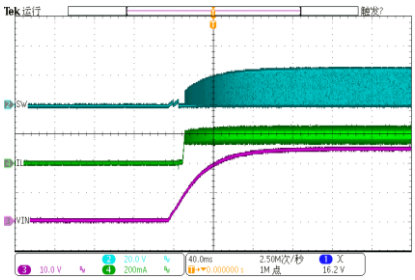
PWM Dimming

3ILEDs, F_{DIM}=10KHz, Duty Cycle=50%



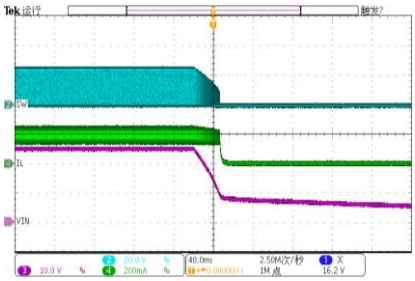
Start-Up through V_{IN}

V_{IN}=24V, I_{LED}=200mA, 3ILEDs



Shutdown through V_{IN}

V_{IN}=24V, I_{LED}=200mA, 3ILEDs



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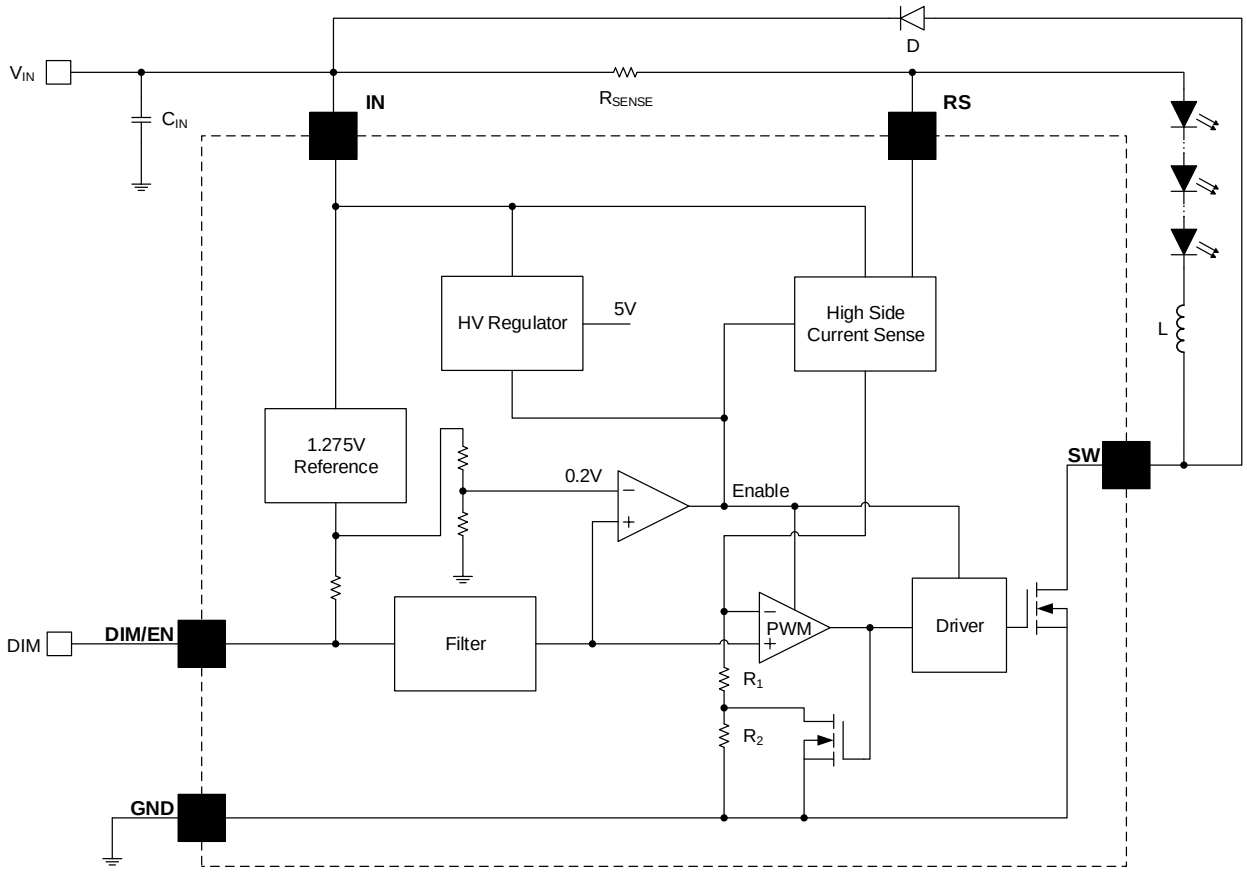
Functional Block Diagram



PT4115 Block Diagram

Functions Description

Steady State

The PT4115 is a hysteretic-controlled, step down LED driver that is easily configured for various applications with an input range from 8.0V to 30V. The converter employs a high-side current-sense resistor to detect and regulate the LED current. The voltage across the current sense resistor is measured and regulated to within 100mV±20mV. When V_{EN}>0.35V, the output of the comparator goes high and the other blocks are enabled. A high-side resistor, R_{SENSE}, senses the output current. When the switch is on, R2 is shorted and R1 sets the output current upper-threshold. When the switch is off, R1 and R2 set the output current lower-threshold, and the ratio of R1 and R2 determines the current hysteresis.

Enable Control

Once Input voltage is applied, the internal reference is connected to EN/DIM pin through pull up resistor. If the EN/DIM pin is left open, **the IC automatically starts up to the maximum brightness**. Adding a capacitor to this pin can hereby program a soft-start time.

Applying an external voltage range from 0.35V to 2.7V to the EN/DIM pin linearly controls the current-sense voltage reference from 0mV to 100mV for analog dimming.

Applying an external PWM voltage with an amplitude of 2.7V to the EN/DIM pin achieves PWM dimming. For additional information on the flexible external PWM dimming method, please refer to the "Selecting Dimming Control Mode" section.

System Soft Start

The voltage on the EN/DIM pin is the inductor current reference. An external capacitor from the EN/DIM pin to ground provides a soft-start delay.

Dimming Control

PT4115 provides two dimming methods: PWM dimming and DC analog dimming.
To use PWM dimming, apply a square wave to the EN/DIM pin. To use analog dimming, apply a 0.35V-to-2.7V DC voltage to this pin.

Application Information

Setting the LED Current

The LED current is set by the current-setting resistor between the IN and RS pins, where:

$$R_{SET} = \frac{100mV}{I_{LED}}$$

For R_{SET}=0.2Ω, the LED current is set to 500mA

Selecting the Inductor

Lower value of the inductor results in higher switching frequencies, leading to larger switch loss. For most applications, select a switching frequency between 200kHz and 600kHz. Estimate the inductor value based on the desired switching frequency, where:

$$L = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{0.4 \times I_{LED} \times f_{SW}}$$

For higher efficiency, use inductors with low DC resistance.

Selecting the Diode

The output diode supplies current flowing path to the inductor when the internal MOSFET is off. To reduce losses due to the diode forward voltage and recovery time, use a Schottky diode. Select a diode rated with a reverse voltage greater than the input voltage. The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the peak inductor current.

Selecting Soft-Start Capacitor

The delay time with the soft-start capacitor can be estimated by 0.2ms/nF. In PWM dimming, select a C<2.2nF to eliminate its effect on the average LED current.

Selecting Dimming Control Mode

PT4115 provides two dimming methods: DC analog dimming and PWM dimming.

1. DC analog dimming mode

Apply a 0.35V-to-2.7V DC voltage to the EN/DIM pin. The voltage from 0.35V to 2.7V changes the inductor current reference directly and linearly controls the inductor current range from 25% to 100% (see Figure 2).

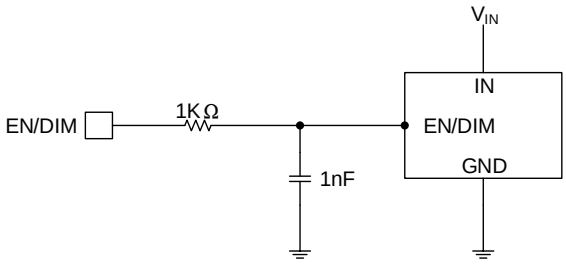


Figure 2: Analog Dimming External Circuit

2. PWM dimming mode

Apply Use a dimming frequency with a typical value of 1KHz and cannot exceed 10KHz to the EN/DIM pin. The average LED current is proportional to the PWM duty cycle.

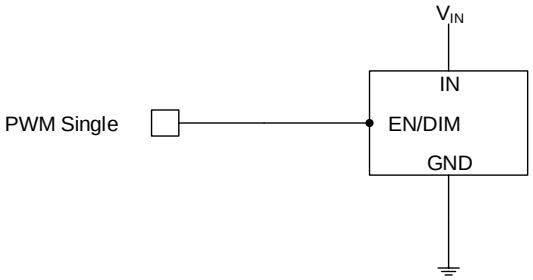


Figure 3: PWM Dimming External Circuit

Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. Input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with an enough width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

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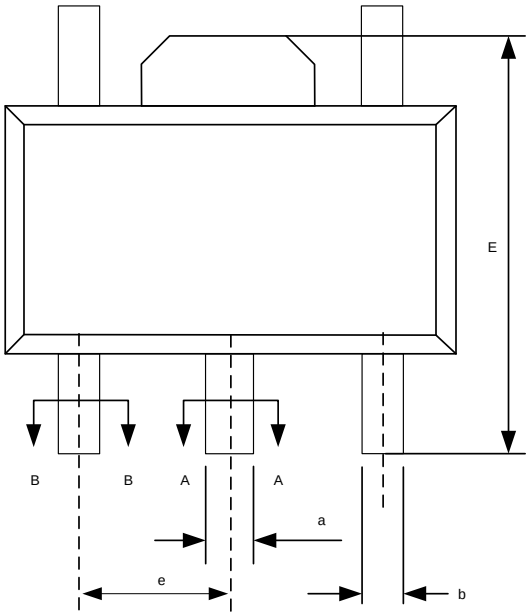
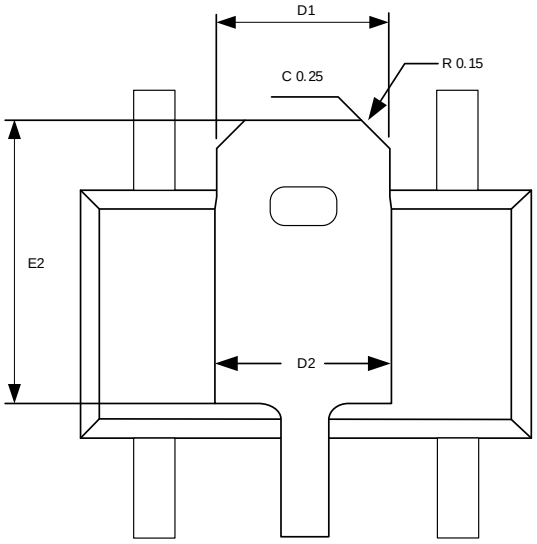
Package Description

SOT89-5

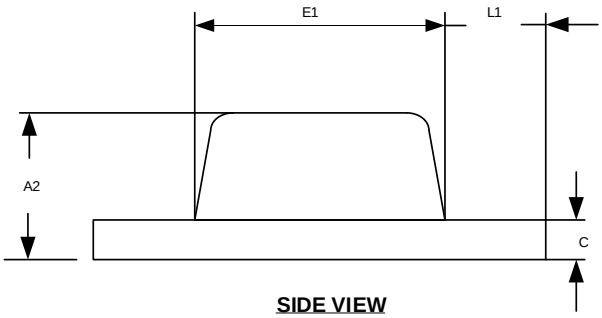


TOP VIEW



BOTTOM VIEW

FRONT VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A2	1.40	1.50	1.60
b	0.38	-	0.46
a	0.46	-	0.56
D	4.40	4.50	4.60
E	4.00	4.20	4.40
E1	2.40	2.50	2.60
e	1.50BSC		
L1	0.80	1.00	1.20

Size(mm) / L/F Size(mil)	D1	D2	E2
85×70	1.70REF	1.75REF	2.84REF

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.