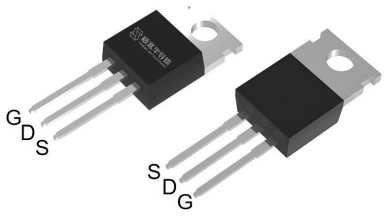
Features

V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	2.2	mΩ
$I_{D(Silicon\ Limited)}$	278	A
$I_{D(Package\ Limited)}$	180	A

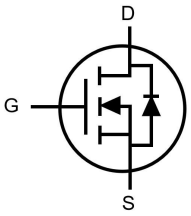
- Enhancement mode
- Very low on-resistance
- VitoMOS® Ⅱ Technology
- 100% Avalanche Tested, Rg 100% Tested
- Optimized Qg, Qgd, and Qgd/Qgs ratio to minimize switching losses

TO-220AB



Pb-Free RoHS HF Halogen-Free

Part ID	Package Type	Marking	Packing
VS1696GTH	TO-220AB	1696GTH	50pcs/Tube



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current (Silicon limited)	T_C = 25°C	278	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 25°C	278	A
I_D	Continuous drain current @VGS=10V (Silicon limited)	T_C = 100°C	197	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C = 25°C	180	A
I_{DM}	Pulse drain current tested ①	T_C = 25°C	1112	A
I_{DSM}	Continuous drain current @VGS=10V	T_A = 25°C	20	A
		T_A = 70°C	16	A
EAS	Avalanche energy, single pulsed ②		1681	mJ
P_D	Maximum power dissipation ③	T_C = 25°C	417	W
P_{DSM}	Maximum power dissipation ④	T_A = 25°C	2.1	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.3	0.36	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	50	60	°C/W

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Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current(Tj=25℃)	V_{DS}=100V,V_{GS}=0V	–	–	1	μA
	Zero Gate Voltage Drain Current(Tj=125℃)⑦	V_{DS}=100V,V_{GS}=0V	–	–	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	–	–	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.4	2.9	3.4	V
$R_{DS(on)}$	Drain-Source On-State Resistance ⑧	V_{GS}=10V, I_D=40A	--	2.2	2.9	mΩ
		Tj=100℃ ⑦	–	3	–	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance ⑦	V_{DS}=50V,V_{GS}=0V, f=1MHz	–	13510	–	pF
Coss	Output Capacitance ⑦		–	2025	–	pF
Crss	Reverse Transfer Capacitance ⑦		–	55	–	pF
Rg	Gate Resistance	f=1MHz	–	1	–	Ω
Qg	Total Gate Charge ⑦	V_{DS}=50V,I_D=40A, V_{GS}=10V	–	177	–	nC
Qgs	Gate-Source Charge ⑦		–	50	–	nC
Qgd	Gate-Drain Charge ⑦		–	47	–	nC
Switching Characteristics ⑦						
Td(on)	Turn-on Delay Time	V_{DD}=50V, I_D=40A, R_G=3Ω, V_{GS}=10V	–	34	–	ns
Tr	Turn-on Rise Time		–	67	–	ns
Td(off)	Turn-Off Delay Time		–	85	–	ns
Tf	Turn-Off Fall Time		–	69	–	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=40A,V_{GS}=0V	–	0.8	1.2	V
Trr	Reverse Recovery Time ⑦	I_{sd}=40A, V_{GS}=0V di/dt=100A/μs	–	134	–	ns
Qrr	Reverse Recovery Charge ⑦		–	223	–	nC

NOTE:

① Single pulse; pulse width ≤ 100μs.

② EAS of 1681mJ is based on starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 82A, V_{GS} =10V； 100% FT tested at L = 0.5mH, I_{AS} = 45A.

③ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

④ The power dissipation Pdsm is based on Tj(max), using junction-to-ambient thermal resistance RθJA.

⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑥ These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

⑦ Guaranteed by design, not subject to production testing.

⑧ Pulse width ≤ 380μs; duty cycle≤ 2%.

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Typical Characteristics

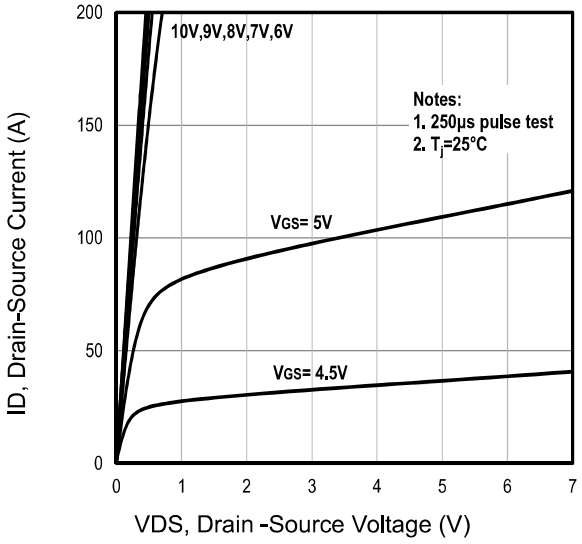

Fig1. Typical Output Characteristics

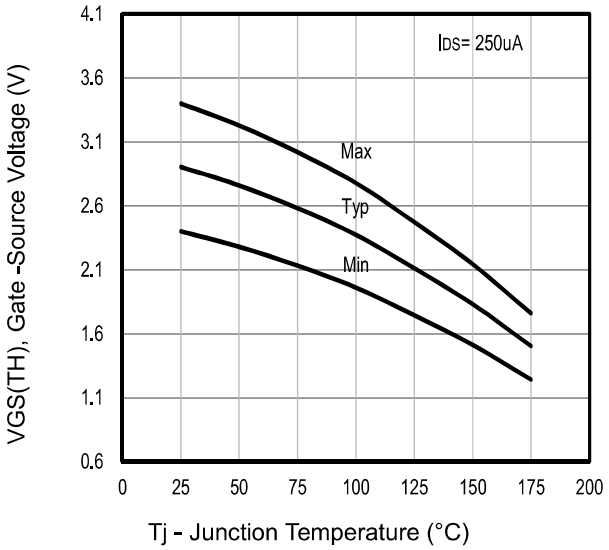

Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

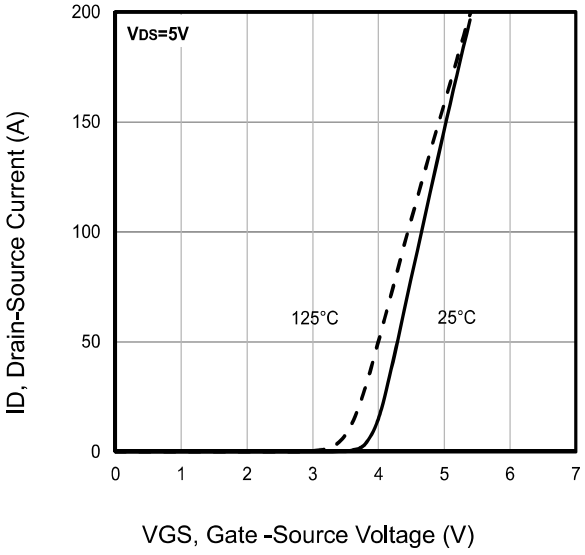

Fig3. Typical Transfer Characteristics

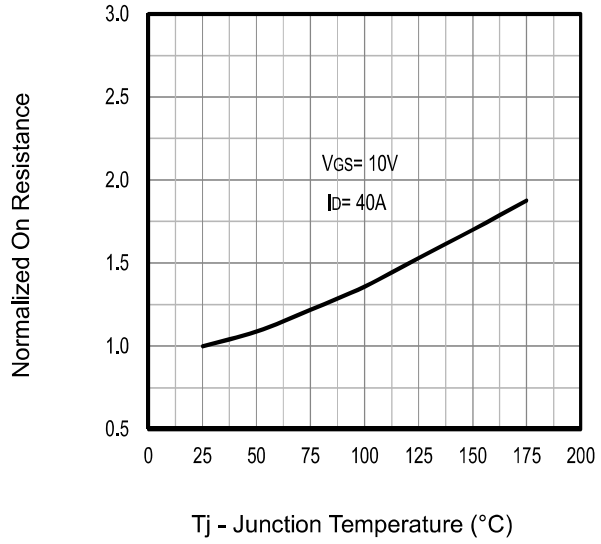

Fig4. Typical Normalized On-Resistance Vs. Tj

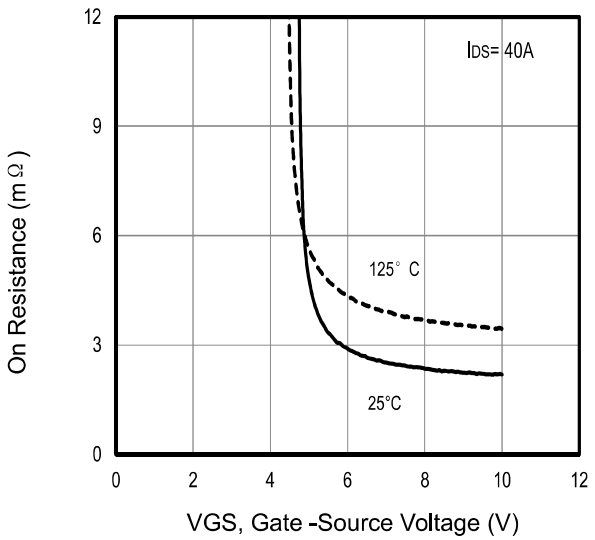

Fig5. Typical On Resistance Vs Gate -Source Voltage

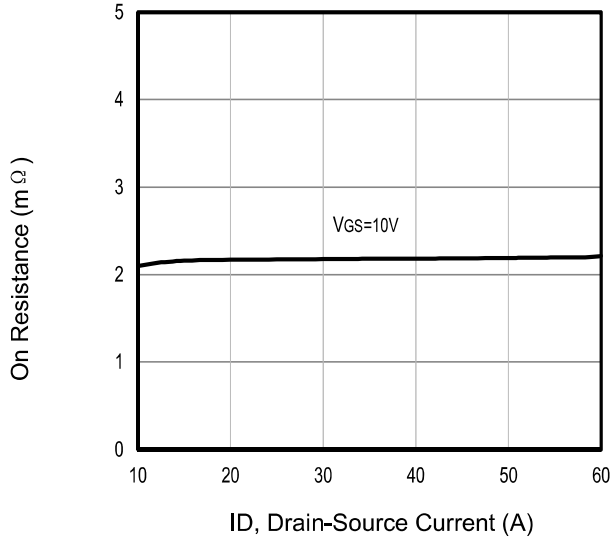

Fig6. Typical On Resistance Vs Drain Current

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Typical Characteristics

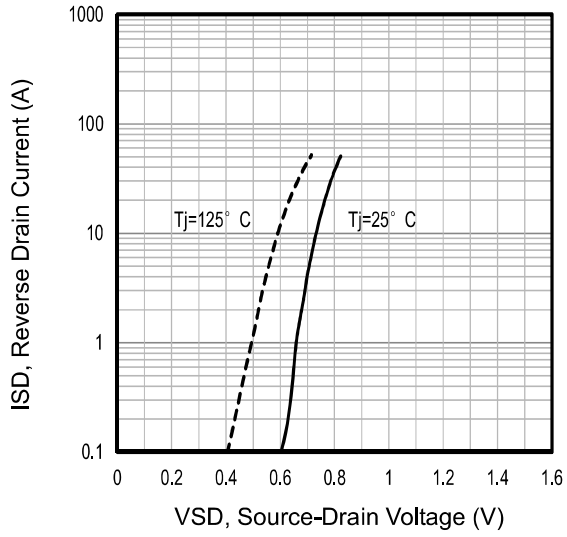

Fig7. Typical Source-Drain Diode Forward Voltage

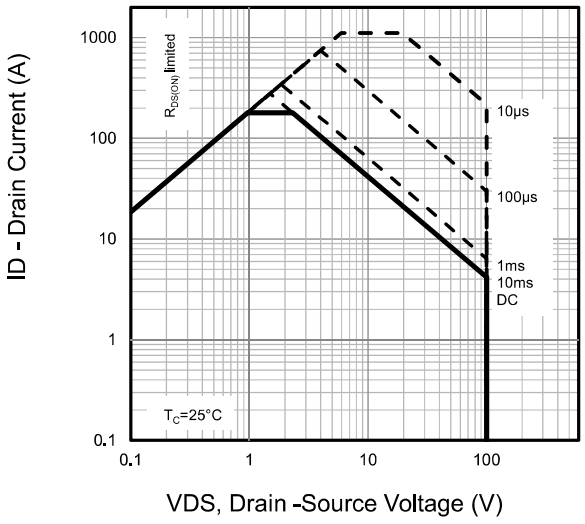

Fig8. Maximum Safe Operating Area

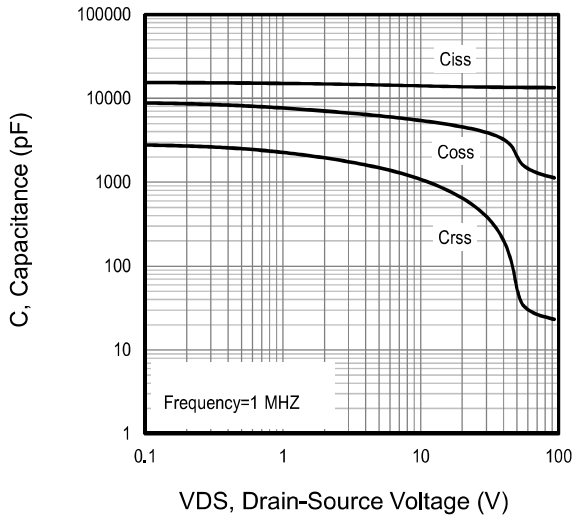

Fig9. Typical Capacitance Vs. Drain-Source Voltage

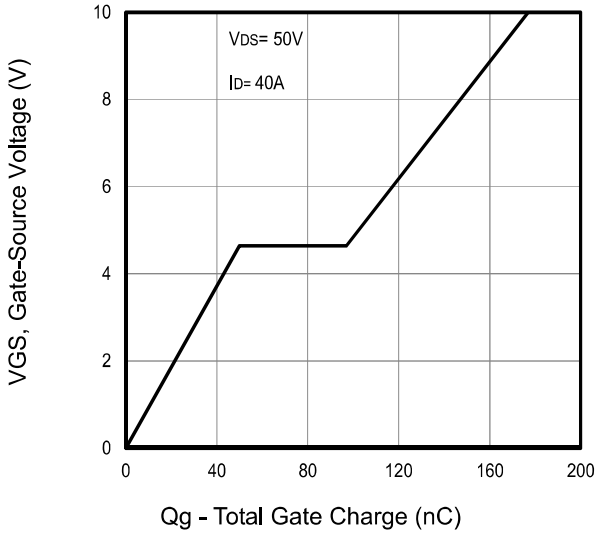

Fig10. Typical Gate Charge Vs. Gate-Source Voltage

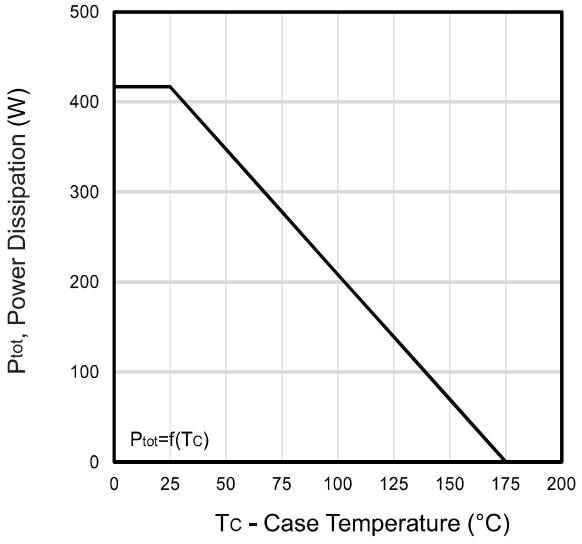

Fig11. Power Dissipation Vs. Case Temperature

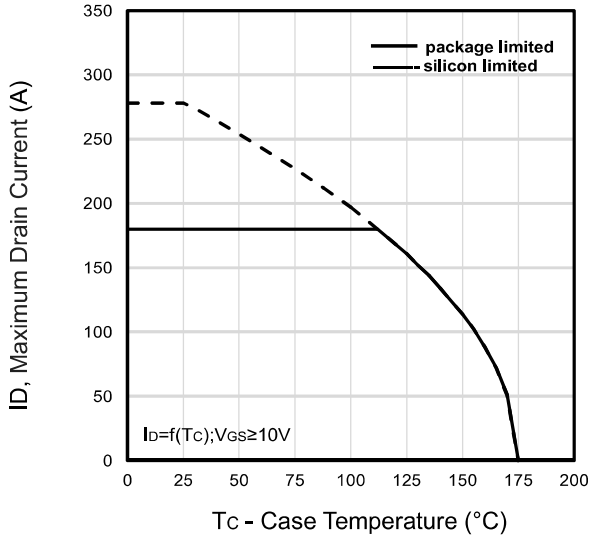

Fig12. Maximum Drain Current Vs. Case Temperature

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Typical Characteristics

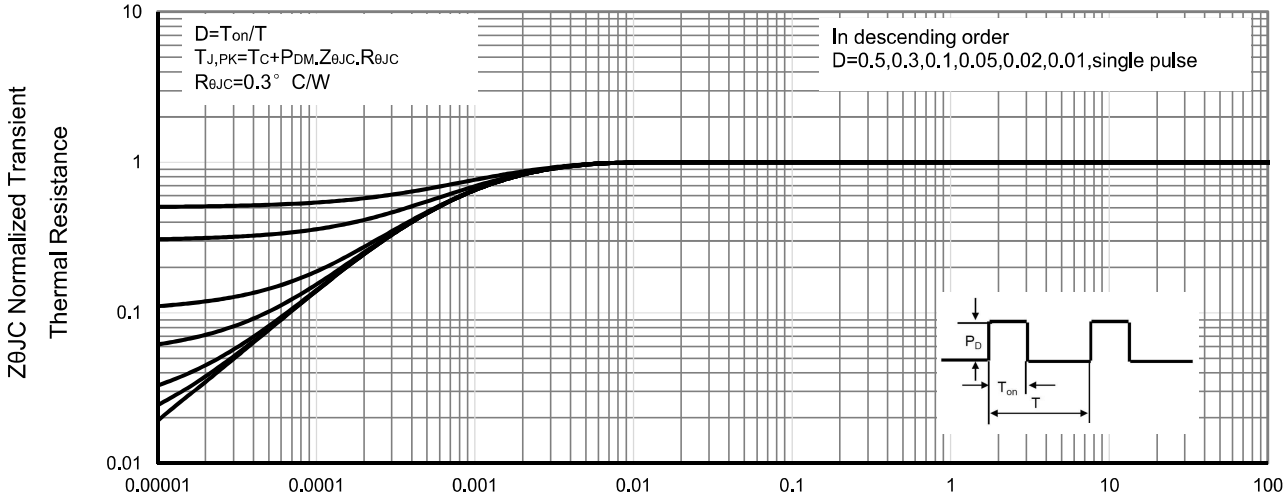

Fig13 . Normalized Maximum Transient Thermal Impedance

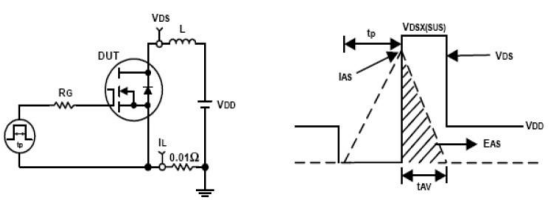

Fig14. Unclamped Inductive Test Circuit and waveforms

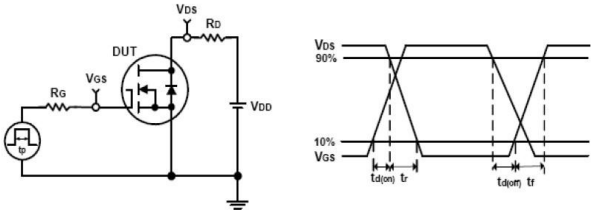

Fig15. Switching Time Test Circuit and waveforms

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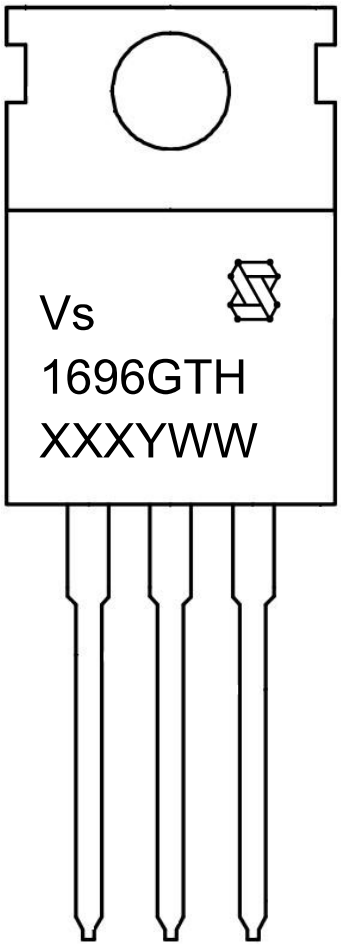
Marking Information



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（1696GTH）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

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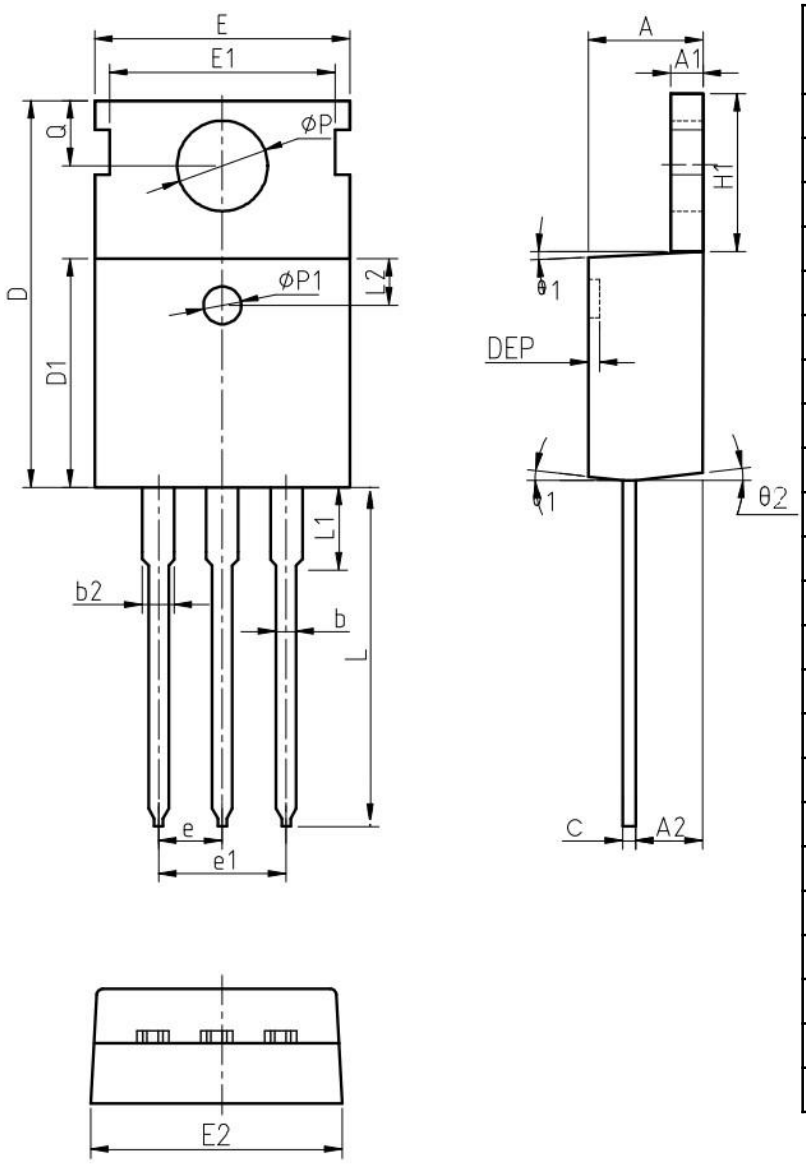
TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.32	1.50
c	0.45	0.50	0.61
D	15.30	15.65	15.90
D1	9.00	9.20	9.40
DEP	0.05	0.10	0.25
E	9.66	9.90	10.28
E1	-	8.70	-
E2	9.80	10.00	10.20
ΦP1	1.40	1.50	1.60
e	2.54 BSC		
e1	5.08 BSC		
H1	6.40	6.50	6.80
L	12.70	-	14.27
L1	-	-	3.95
L2	2.40	2.50	2.60
ΦP	3.53	3.60	3.70
Q	2.70	2.80	2.90
θ1	5 °	7 °	9 °
θ2	1 °	3 °	5 °

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

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