

## 100V N-Channel Power MOSFET

### DESCRIPTION

The IRF530 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It can be used in a wide variety of applications.

### Application

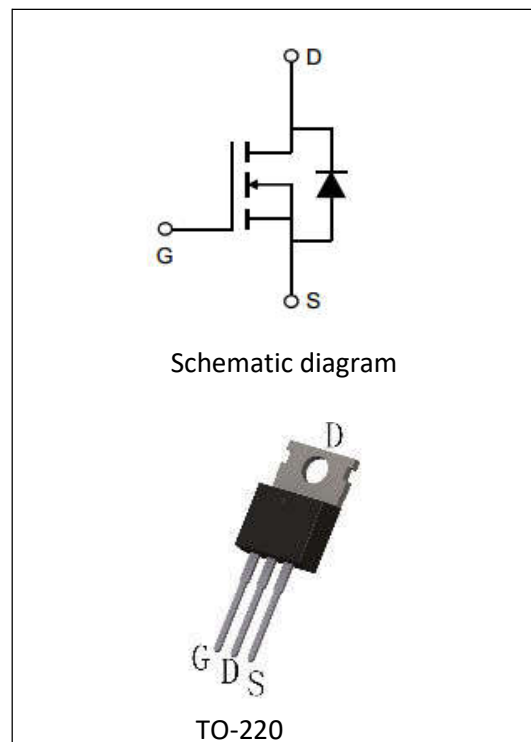
- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply

### KEY CHARACTERISTICS

- ①  $V_{DS}=100V, I_D=15A$   
 $R_{DS(ON)} < 90m\Omega @ V_{GS}=10V$   $R_{DS(ON)} < 115m\Omega @ V_{GS}=4.5V$
- ② High density cell design for lower  $R_{DS(ON)}$
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation

**100% UIS TESTED !**

**100% DVDS TESTED !**



### Package Marking And Ordering Information

| Device Marking | Ordering Codes | Package | Product Code | Packing |
|----------------|----------------|---------|--------------|---------|
| IRF530         | IRF530         | TO-220  | IRF530       | Tube    |

### Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

| Parameter                                        | Symbol         | Limit      | Unit        |
|--------------------------------------------------|----------------|------------|-------------|
| Drain-Source Voltage                             | $V_{DS}$       | 100        | V           |
| Gate-Source Voltage                              | $V_{GS}$       | $\pm 20$   | V           |
| Drain Current-Continuous                         | $I_D$          | 15         | A           |
| Drain Current-Pulsed (Note 1)                    | $I_{DM}$       | 40         | A           |
| Maximum Power Dissipation( $T_c=25^{\circ}C$ )   | $P_D$          | 31         | W           |
| Single pulse avalanche energy (Note 2)           | $E_{AS}$       | 21         | mJ          |
| Operating Junction and Storage Temperature Range | $T_J, T_{STG}$ | -55 To 175 | $^{\circ}C$ |

### Thermal Characteristic

|                                      |                 |     |               |
|--------------------------------------|-----------------|-----|---------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 4.8 | $^{\circ}C/W$ |
|--------------------------------------|-----------------|-----|---------------|

## Electrical Characteristics (TA=25 °C unless otherwise noted)

| Parameter                                            | Symbol              | Condition                                                                                 | Min | Typ | Max  | Unit |
|------------------------------------------------------|---------------------|-------------------------------------------------------------------------------------------|-----|-----|------|------|
| Off Characteristics                                  |                     |                                                                                           |     |     |      |      |
| Drain-Source Breakdown Voltage                       | B <sub>VDSS</sub>   | V <sub>GS</sub> =0V I <sub>D</sub> =250μA                                                 | 100 | -   | -    | V    |
| Zero Gate Voltage Drain Current                      | I <sub>DSS</sub>    | V <sub>DS</sub> =100V, V <sub>GS</sub> =0V                                                | -   | -   | 1    | μA   |
| Gate-Body Leakage Current                            | I <sub>GSS</sub>    | V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V                                                | -   | -   | ±100 | nA   |
| On Characteristics                                   |                     |                                                                                           |     |     |      |      |
| Gate Threshold Voltage                               | V <sub>GS(th)</sub> | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA                                  | 1   | 1.8 | 2.4  | V    |
| Drain-Source On-State Resistance <sup>(Note 3)</sup> | R <sub>DS(ON)</sub> | V <sub>GS</sub> =10V, I <sub>D</sub> =5A                                                  | -   | 80  | 90   | mΩ   |
|                                                      |                     | V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A                                                 |     | 90  | 115  |      |
| Forward Transconductance                             | g <sub>FS</sub>     | V <sub>DS</sub> =25V, I <sub>D</sub> =3.6A                                                | -   | 5   | -    | S    |
| Dynamic Characteristics                              |                     |                                                                                           |     |     |      |      |
| Input Capacitance                                    | C <sub>ISS</sub>    | V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz                                       | -   | 680 | -    | pF   |
| Output Capacitance                                   | C <sub>OSS</sub>    |                                                                                           | -   | 110 | -    | pF   |
| Reverse Transfer Capacitance                         | C <sub>RSS</sub>    |                                                                                           | -   | 85  | -    | pF   |
| Switching Characteristics <sup>(Note 4)</sup>        |                     |                                                                                           |     |     |      |      |
| Turn-on Delay Time                                   | t <sub>d(on)</sub>  | V <sub>DD</sub> =50V, I <sub>D</sub> =5A,<br>V <sub>GS</sub> =10V, R <sub>GEN</sub> =2.5Ω | -   | 10  | -    | nS   |
| Turn-on Rise Time                                    | t <sub>r</sub>      |                                                                                           | -   | 7   | -    | nS   |
| Turn-Off Delay Time                                  | t <sub>d(off)</sub> |                                                                                           | -   | 34  | -    | nS   |
| Turn-Off Fall Time                                   | t <sub>f</sub>      |                                                                                           |     | 9   | -    | nS   |
| Total Gate Charge                                    | Q <sub>g</sub>      | V <sub>DS</sub> =80V, I <sub>D</sub> =3A V <sub>GS</sub> =10V                             | -   | 16  | -    | nC   |
| Gate-Source Charge                                   | Q <sub>gs</sub>     |                                                                                           | -   | 4   | -    | nC   |
| Gate-Drain Charge                                    | Q <sub>gd</sub>     |                                                                                           | -   | 5   | -    | nC   |
| Drain-Source Diode Characteristics                   |                     |                                                                                           |     |     |      |      |
| Diode Forward Voltage                                | V <sub>SD</sub>     | V <sub>GS</sub> =0V, I <sub>S</sub> =15A                                                  | -   | -   | 1.2  | V    |

## Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition :T j=25 °C ,VDD=50V,VGS=10V,L=0.5mH,Rg=25 $\Omega$
- 3.Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
- 4.Guaranteed by design, not subject to production.

## Characteristics Curves

Figure 1 Output Characteristics

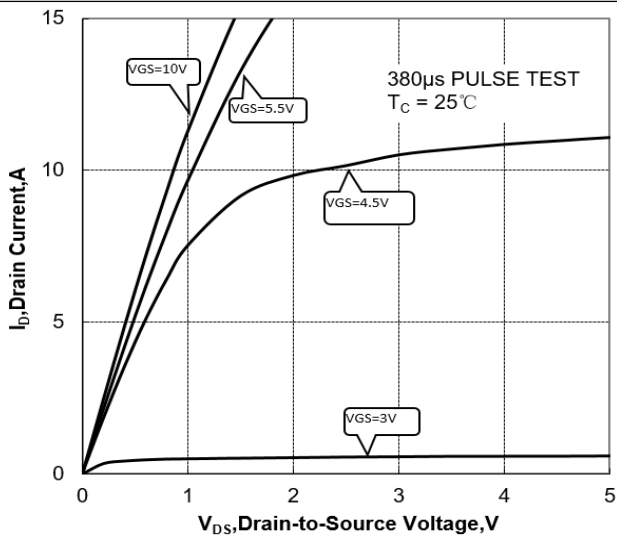


Figure 2 Transfer Characteristics

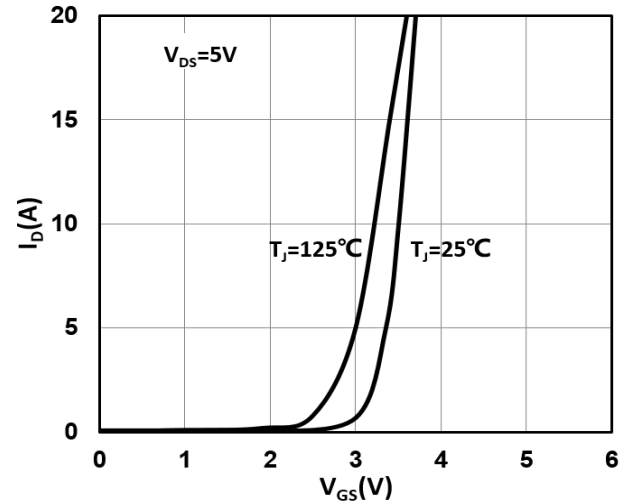


Figure 3 On-Resistance vs.  $I_D$  and  $V_{GS}$

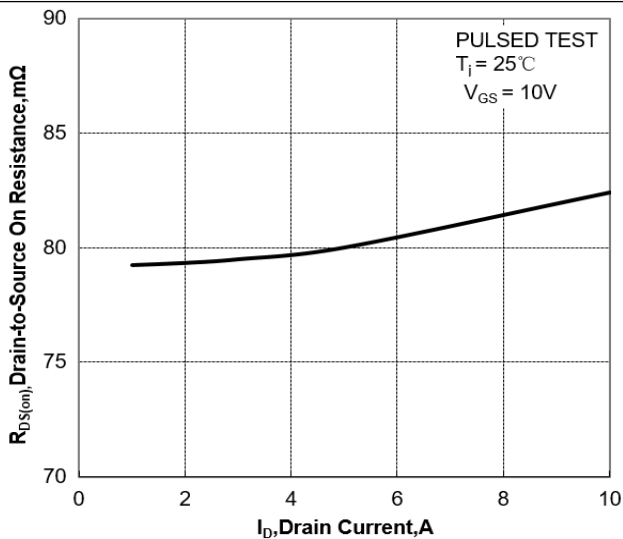


Figure 4 On-Resistance vs. Junction Temperature

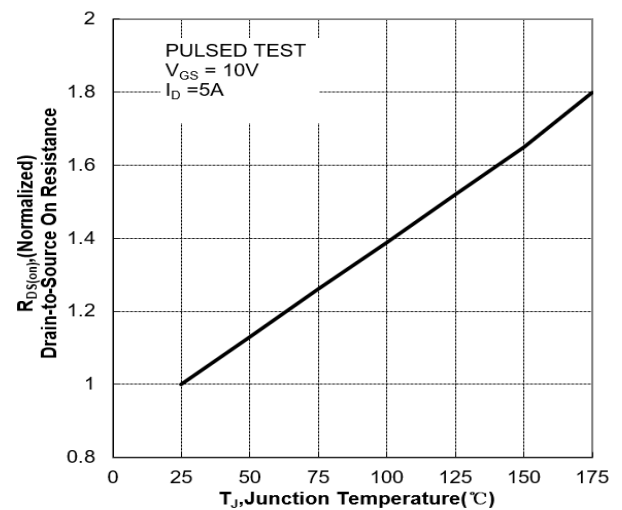


Figure 5 On-Resistance vs.  $V_{GS}$

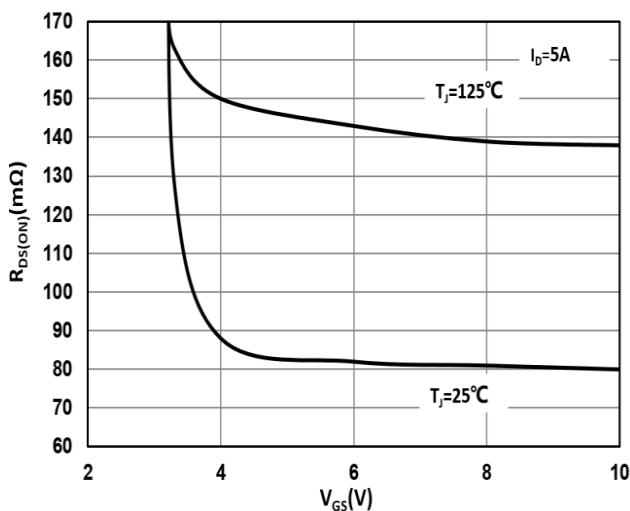


Figure 6 Body Diode Forward Voltage

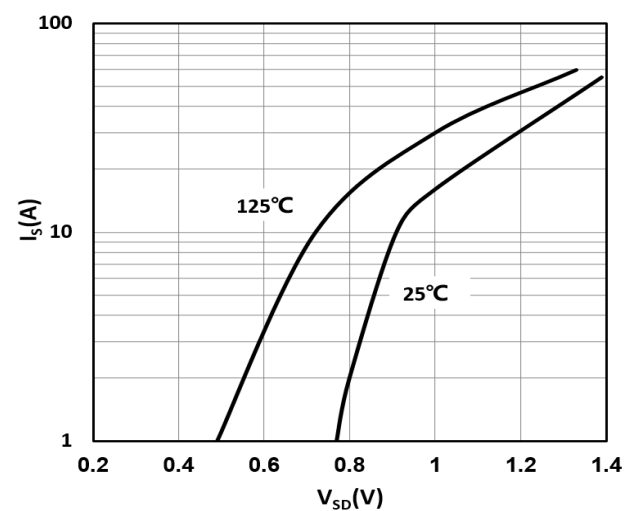


Figure 7 Gate-Charge Characteristics

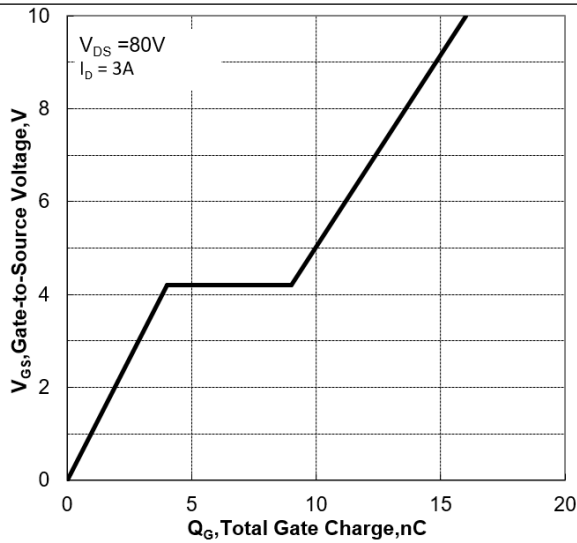


Figure 8 Capacitance Characteristics

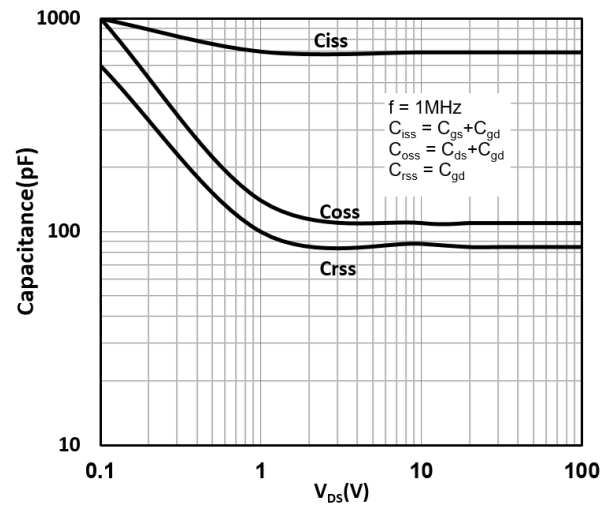


Figure 9 Maximum Forward Biased Safe Operation Area

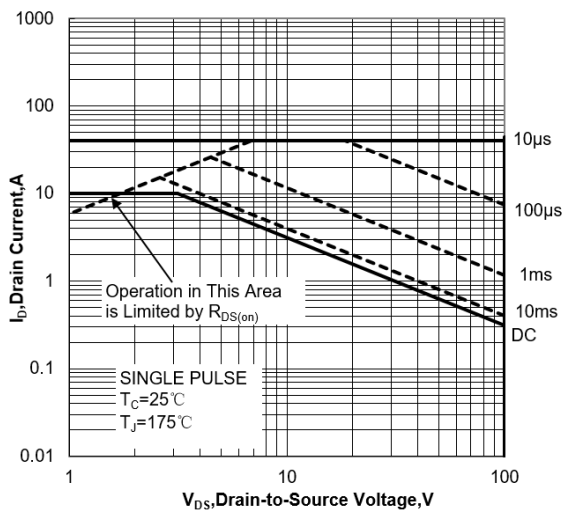


Figure 10 Single Pulse Power Rating Junction-to-Ambient

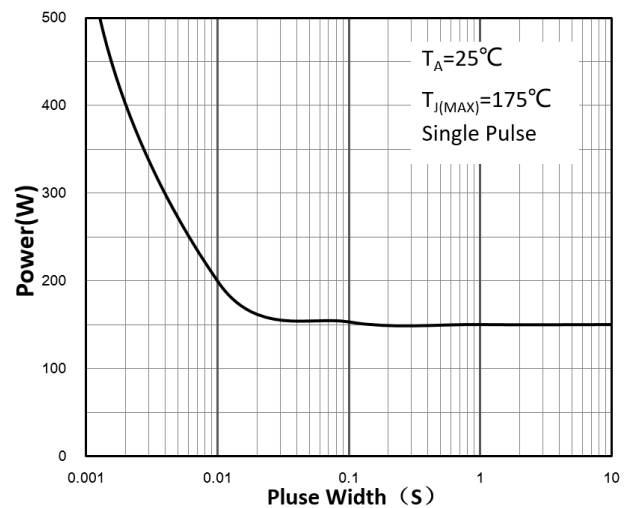
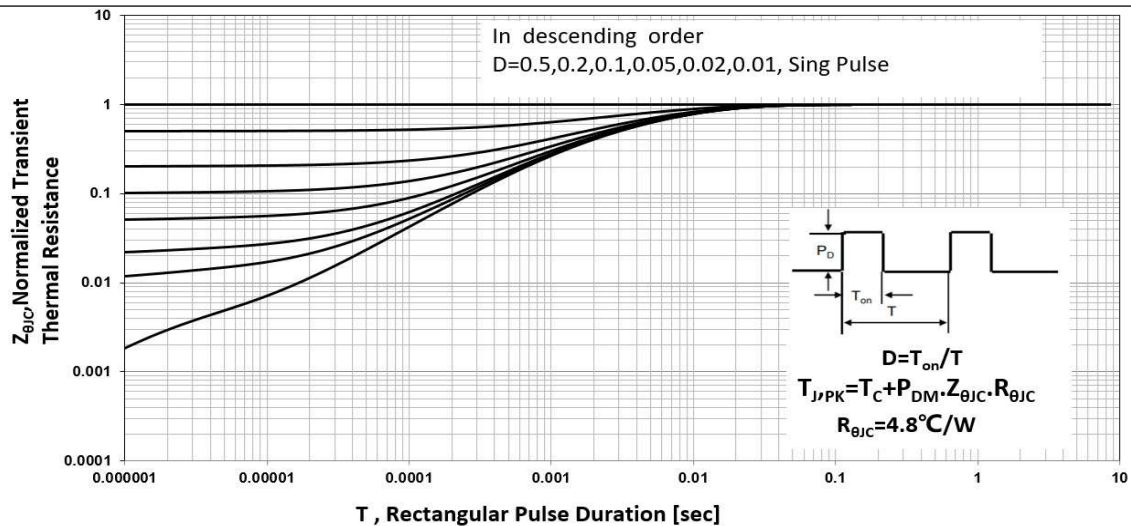
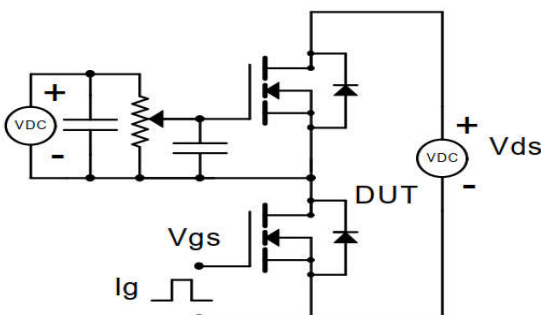
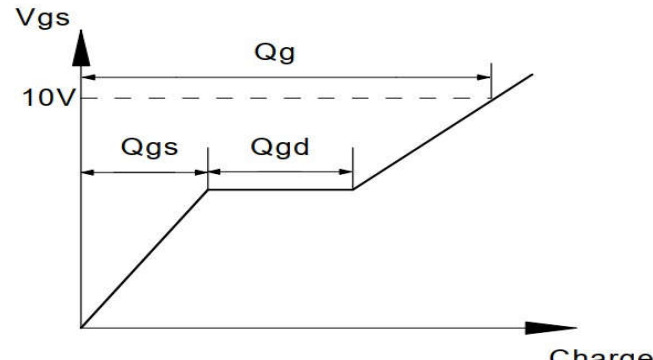
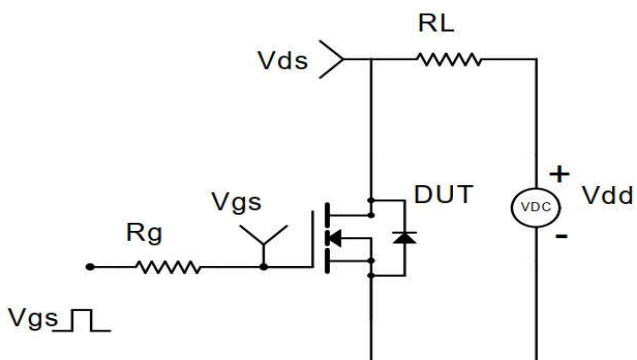
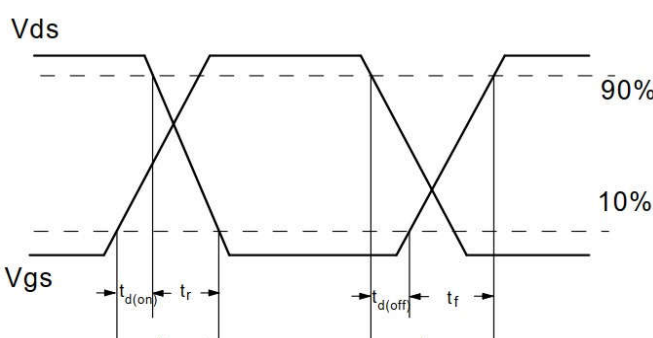
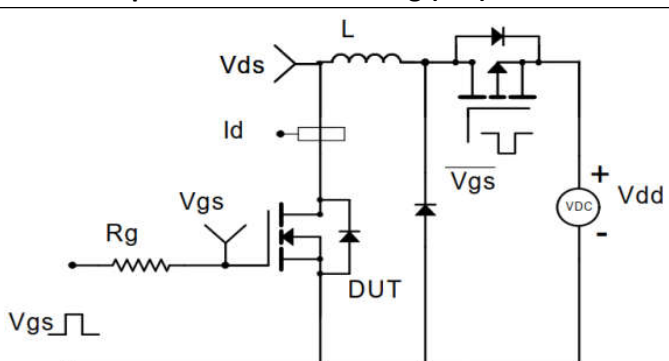
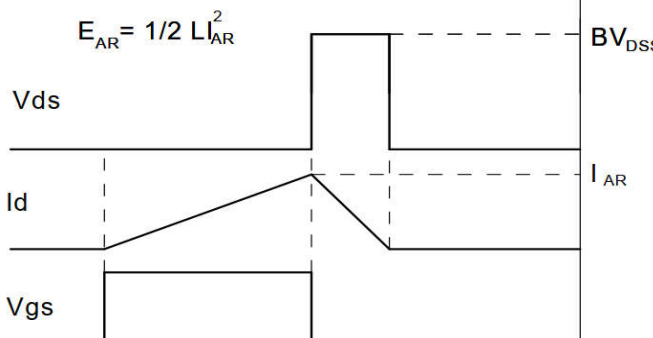
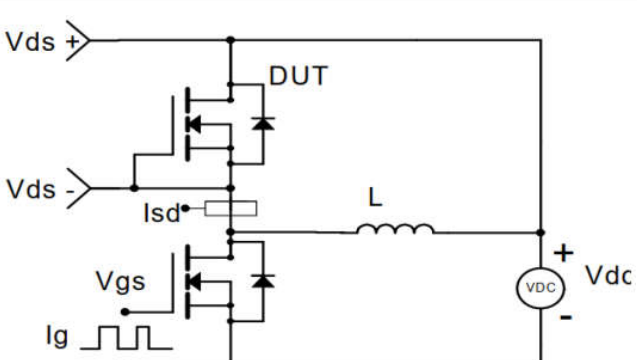
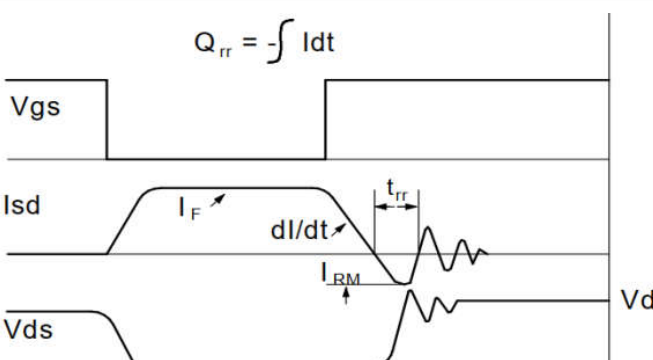


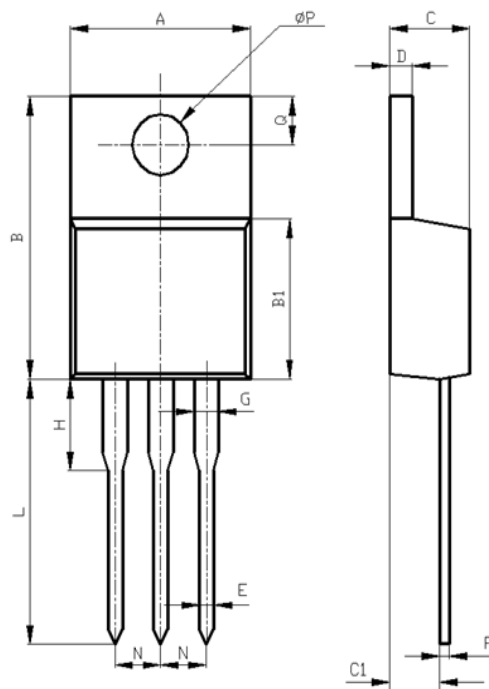
Figure 11 Normalized Maximum Transient Thermal Impedance



## Test Circuit and Waveform

| Gate Charge Test Circuit                                                                                                                                                                                                                                                                                                                                             | Gate Charge Test Waveform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Ig) through a resistor. The drain is connected to a load resistor and a DC voltage source (VDC). The source is connected to ground. The gate voltage (Vgs) is shown as a pulse.</p>              |  <p>The graph shows Vgs on the y-axis and Charge on the x-axis. The waveform starts at 0V, rises linearly to 10V, remains constant at 10V for a duration Qg, and then falls linearly back to 0V. The rising and falling times are labeled Qgs and Qgd respectively.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Resistive Switching Test Circuit                                                                                                                                                                                                                                                                                                                                     | Resistive Switching Test Waveforms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to a load resistor (RL) and a DC voltage source (VDC). The source is connected to ground. The drain voltage (Vds) is shown as a pulse.</p> |  <p>The graph shows Vds and Vgs on the y-axis and time on the x-axis. Vds is a trapezoidal pulse. Vgs is a square wave pulse. The switching times are labeled: t<sub>d(on)</sub>, t<sub>r</sub>, t<sub>d(off)</sub>, t<sub>f</sub>, t<sub>on</sub>, and t<sub>off</sub>. The pulse levels are marked at 90% and 10%.</p>                                                                                                                                                                                                                                                                                                                                                                                    |
| Unclamped Inductive Switching (UIS) Test Circuit                                                                                                                                                                                                                                                                                                                     | Unclamped Inductive Switching (UIS) Test Waveforms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to an inductor (L) and a DC voltage source (VDC). The source is connected to ground. The drain current (Id) is shown as a pulse.</p>       |  <p>The graph shows Vds, Id, and Vgs on the y-axis and time on the x-axis. Vds is a trapezoidal pulse. Id is a triangular pulse. Vgs is a square wave pulse. The switching times are labeled: t<sub>d(on)</sub>, t<sub>r</sub>, t<sub>d(off)</sub>, t<sub>f</sub>, t<sub>on</sub>, and t<sub>off</sub>. The pulse levels are marked at 90% and 10%. The energy dissipation formula is given: <math>E_{AR} = 1/2 L I_{AR}^2</math>. The peak drain voltage is labeled BV<sub>DSS</sub> and the peak drain current is labeled I<sub>AR</sub>.</p>                                                                                                                                                            |
| Diode Recovery Test Circuit                                                                                                                                                                                                                                                                                                                                          | Diode Recovery Test Waveforms                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|  <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a resistor (Rg). The drain is connected to an inductor (L) and a DC voltage source (VDC). The source is connected to ground. The drain current (Id) is shown as a pulse.</p>      |  <p>The graph shows Vgs, Id, and Vds on the y-axis and time on the x-axis. Vgs is a square wave pulse. Id is a triangular pulse. Vds is a trapezoidal pulse. The switching times are labeled: t<sub>d(on)</sub>, t<sub>r</sub>, t<sub>d(off)</sub>, t<sub>f</sub>, t<sub>on</sub>, and t<sub>off</sub>. The pulse levels are marked at 90% and 10%. The energy dissipation formula is given: <math>Q_{rr} = \int Idt</math>. The peak drain current is labeled I<sub>F</sub> and the reverse recovery current is labeled I<sub>RM</sub>. The reverse recovery time is labeled t<sub>rr</sub>. The peak drain voltage is labeled BV<sub>DSS</sub> and the peak drain current is labeled I<sub>AR</sub>.</p> |

## Package Description



| Items | Values (mm) |      |
|-------|-------------|------|
|       | MIN         | MAX  |
| A     | 9.60        | 10.6 |
| B     | 15.0        | 16.0 |
| B1    | 8.90        | 9.50 |
| C     | 4.30        | 4.80 |
| C1    | 2.30        | 3.10 |
| D     | 1.20        | 1.40 |
| E     | 0.70        | 0.90 |
| F     | 0.30        | 0.60 |
| G     | 1.17        | 1.37 |
| H     | 2.70        | 3.80 |
| L     | 12.6        | 14.8 |
| N     | 2.34        | 2.74 |
| Q     | 2.40        | 3.00 |

**TO-220 Package**



**NOTE:**

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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