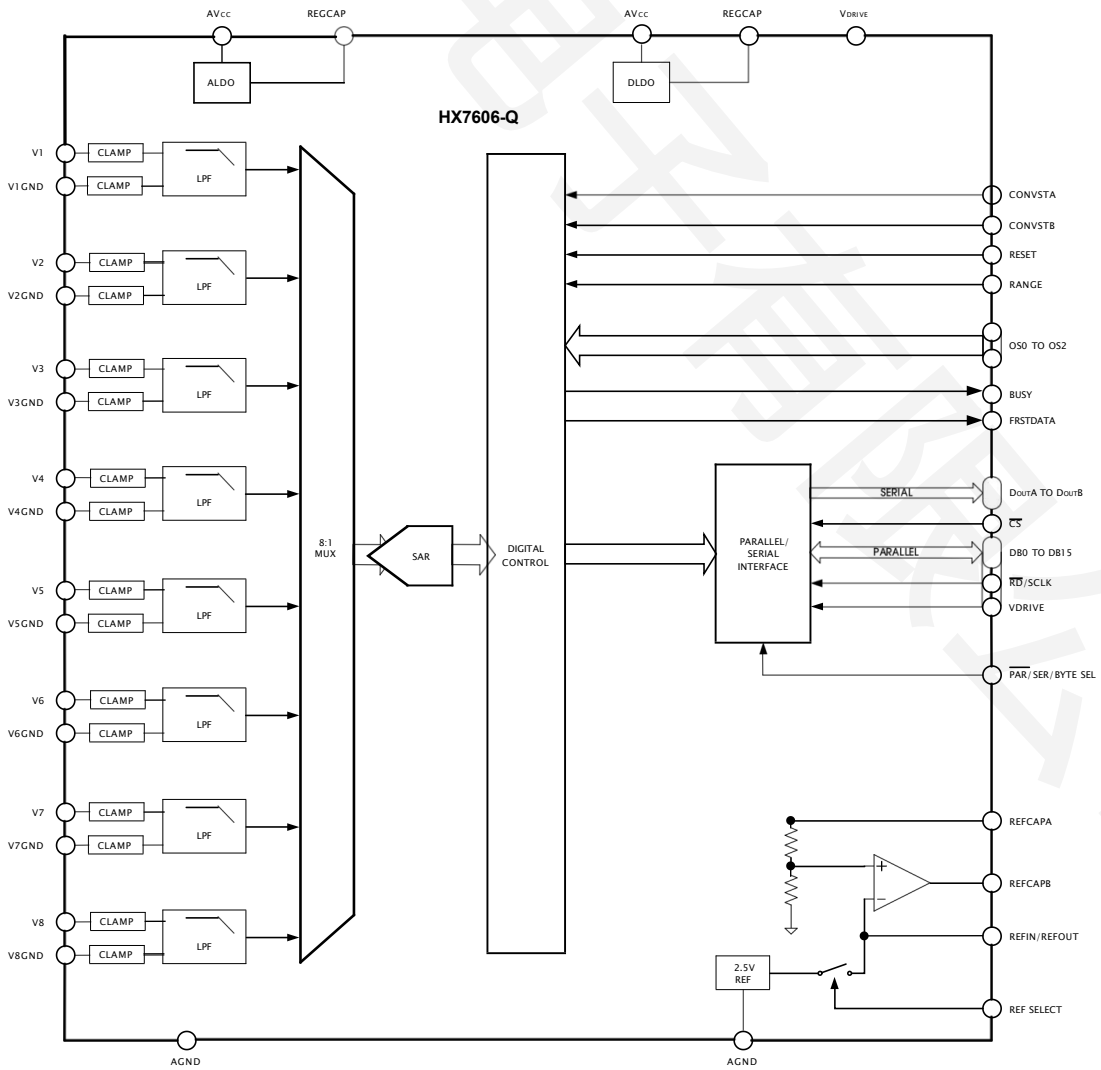
HX7606-Q Eight-channel 16-bit 200kSPS ADC

Peculiarity

- 16-bit, 200kSPS (all channels)
- An input buffer with a 1MΩ analog input impedance
- Operating temperature range: -40 °C to +85°C
- 5V single analog power supply
- VDRIVE power supply voltage: 2.3V to 5V
- ±30V input clamp protection, 8kV ESD
- Second-order anti-aliasing analog filter
- On-chip precision reference source and reference voltage source buffers
- True bipolar analog input range: ±10V, ±5V
- The oversampling function of integrated digital filters
- SNR: 86dB (no oversampling) or 95dB (64 times oversampling)
- LQFP-64 package: 10mm × 10mm

Apply

- Power line monitoring
- Relay protection
- Multiphase motor control
- Instruments and control systems
- Data acquisition system



Pin configuration and function

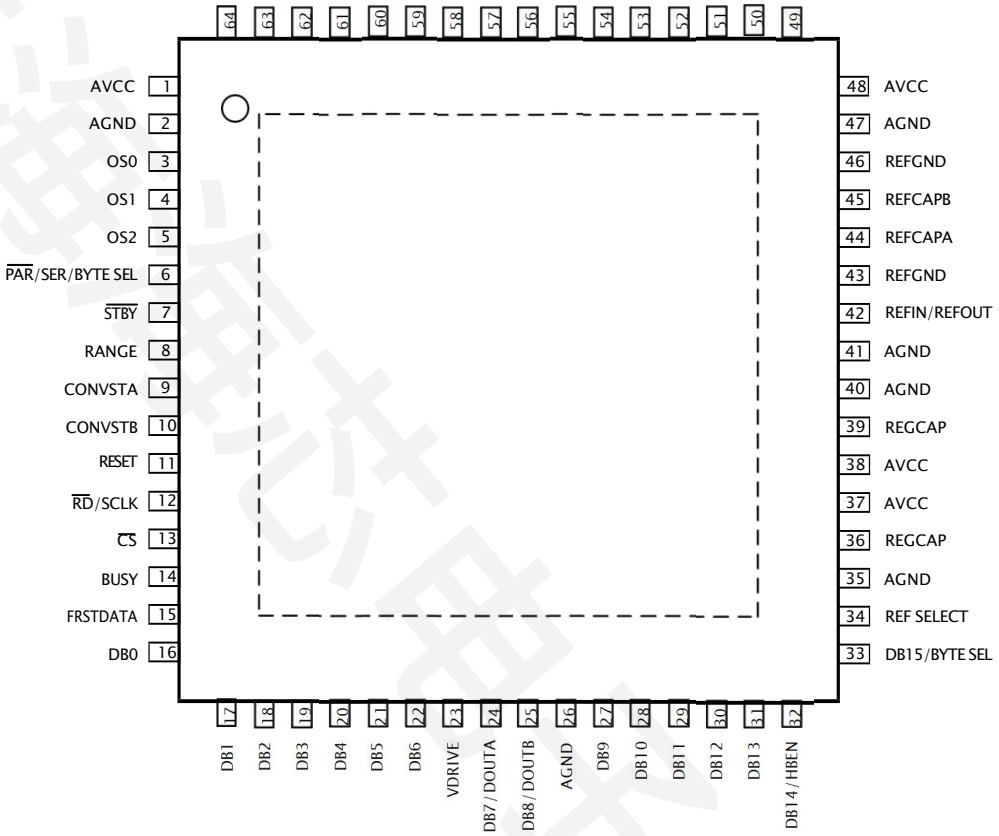


Figure 1. Pin Configuration

Table 2. Pin Functions

Position	Name	Type	Description
1, 37, 38, 48	AVCC	Power	Analog supply voltage 4.75V to 5.25V. Decouple the supply pins to AGND.
2, 26, 35, 40, 41, 47	AGND	Ground	Analog ground The six AGND pins must be connected to the system-layer ground plane as the ground points for all analog circuits on the chip.
3 to 5	OS0 to OS2	Digital input	Oversampling mode pins
6	$\overline{\text{PAR}}$/SER/BYTE SEL	Digital input	Parallel/serial interface select input If this pin is logic low level, the parallel interface input is selected; if this pin is logic high level, the serial interface input is selected.
7	$\overline{\text{STBY}}$	Digital input	Power mode selection When this pin is connected to a logic low level, the chip can be configured in standby mode or power-down mode by using this pin and the RANGE pin. Must be set to a logic high level for normal circuit operation.
8	RANGE	Digital input	Analog input range selection Under normal operation of the circuit, this pin determines the input range of the analog input channel. If the $\overline{\text{STBY}}$ pin is at logic high level and RANGE is 0, the input range is ±5V; when RANGE is 1, the input range is ±10V. If the $\overline{\text{STBY}}$ pin is at a logic low level, the chip enters a power-saving mode (standby or power-down mode).

Position	Name	Type	Description
9, 10	CONVSTA CONVSTB	Digital input	Conversion start input signal The ADC starts converting when the CONVST A and B pins change from low to high.
11	RESET	Digital input	Reset input, active high A RESET during an ADC conversion terminates the conversion; a RESET during a read resets the output registers to all 0s. It is recommended to RESET once after the device is powered on.
12	$\overline{RD}$/SCLK	Digital input	Parallel data read control input ($\overline{RD}$) in parallel interface mode Serial clock input (SCLK) in serial interface mode
13	$\overline{CS}$	Digital input	Chip select signal For both serial and parallel interfaces, this pin is active low and is used for ADC data reading or register data reading and writing.
14	BUSY	Digital output	Output busy signal This pin goes logic high with the rising edges of CONVSTA and CONVSTB. The BUSY output remains high until all channel conversion processes are complete.
15	FRSTDATA	Digital output	First data output flag The FRSTDATA output signal indicates when the data of the first channel V1 is read on the parallel or serial interface.
16 to 22	DB0 to DB6	Digital output	Parallel output data bits When using the parallel interface, these pins are used as tri-state parallel digital inputs and outputs; when using the serial interface, these pins should be connected to AGND. When using the parallel byte interface, DB[7:0] output the 16-bit conversion result after two read operations.
23	VDRIVE	Power	Logic power input The supply voltage (2.3V to 5.25V) on this pin is the operating voltage for the logic interface.
24	DB7/DOUTA	Digital output	Parallel output data bit (DB7) or serial interface data output pin (DOUTA) When using the parallel interface, this pin acts as a tri-state parallel digital input/output pin. When using the serial interface, this pin is used as DOUTA.
25	DB8/DOUTB	Digital output	Parallel output data bit 8 (DB8) or serial interface data output pin (DOUTB) When using the parallel interface, this pin is used as a tri-state parallel digital input/output pin; when using the serial interface, this pin is used as DOUTB.
27 to 31	DB[9:13]	Digital output	Parallel output data bits DB9 to DB13 When using the parallel interface, these pins are used as tri-state parallel digital input and output pins; when using the serial interface, these pins should be connected to AGND.
32	DB14/HBEN	Digital output/digital input	Data bit DB14 for parallel interface output or high byte enable (HBEN) When PAR/SER/BYTE SEL = 0, the pin is used as a tri-state gate parallel digital input and output pins. When both CS and RD are low level, output the conversion result of DB14. When PAR/SER/BYTE SEL = 0, and when DB15/BYTE SEL = 1, the chip enters the parallel byte interface mode, and HBEN decides the output sequence of high-order bytes. If HEBN = 1, the high-order byte (MSB) is output first. If HEBN = 0, the lower byte (LSB) is output first.
33	DB15/BYTE SEL	Digital output/digital input	Data bit DB15 for parallel interface output or parallel byte mode selection (BYTE SEL) When PAR/SER/BYTE SEL = 0, the pin is used as a tri-state gate parallel digital input and output pins. When both CS and RD are low level, output the conversion result of DB15. When PAR/SER/BYTE SEL = 1, BYTE SEL determines the chip interface serial parallel mode. If DB15/BYTE SEL= 0, it is serial interface mode; if DB15/BYTE_SEL = 1, it is parallel byte interface mode.

Position	Name	Type	Description
34	REF SELECT	Digital input	Internal/external reference select logic input If this pin is set to AVCC voltage, the internal reference voltage mode is selected. If this pin is set to logic low, the internal reference is disabled and an external reference must be used.
36, 39	REGCAP	Power	Decoupling capacitor pins Used for the voltage output of the 1.9V internal regulator, analog low dropout (ALDO), and digital low dropout (DLDO) regulators. A 1μF decoupling capacitor must be connected to AGND.
42	REFIN/REFOUT	Analog input/ouput	Reference voltage input (REFIN) or reference voltage output (REFOUT) When the REF SELECT pin is set to logic high, the internal 2.5V reference is used; when the REF SELECT pin is set to logic low, the internal reference is disabled and an external 2.5V reference can be used. For both internal and external reference options, use a 10μF decoupling capacitor from the REFIN pin to ground (near the REFGND pin).
43, 46	REFGND	Analog input	Reference voltage ground pins Both pins connect to AGND.
44, 45	REFCAPA, REFCAPB	Analog input/ouput	Reference voltage buffered outputs These pins must be tied together and decoupled to AGND with a low ESR (effective series resistance) 10μF ceramic decoupling capacitor. The voltage on the pin is typically 4.5V.
49	V1	Analog input	Channel 1 analog input
50	V1GND	Analog input	Channel 1 analog input
51	V2	Analog input	Channel 2 analog input
52	V2GND	Analog input	Channel 2 analog input
53	V3	Analog input	Channel 3 analog input
54	V3GND	Analog input	Channel 3 analog input
55	V4	Analog input	Channel 4 analog input
56	V4GND	Analog input	Channel 4 analog input
57	V5	Analog input	Channel 5 analog input
58	V5GND	Analog input	Channel 5 analog input
59	V6	Analog input	Channel 6 analog input
60	V6GND	Analog input	Channel 6 analog input
61	V7	Analog input	Channel 7 analog input
62	V7GND	Analog input	Channel 7 analog input
63	V8	Analog input	Channel 8 analog input
64	V8GND	Analog input	Channel 8 analog input

Specifications

Absolute maximum rated power

Table 3. Absolute maximum Ratings

Parameter	Description	Min	Max	Units
Voltage	AVCC to AGND	−0.3	7	V
	VDRIVE to AGND	−0.3	AVCC + 0.3	V
	Analog input voltage to AGND		±30	V
	Digital input voltage to AGND	−0.3	VDRIVE + 0.3	V
	Digital output voltage to AGND	−0.3	VDRIVE + 0.3	V
Temperature	Operating, T_A	−40	85	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	−65	150	°C

Note: Stresses beyond those listed under Table 3may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 5. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD ratings

Table 4. ESD Ratings

Parameter	Symbol	Description	VALUE	Units
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000V for analog pins	V
			±3500V for others	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	TBD	

Note 1: The JEDEC document JEP155 Indicate that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 Indicate that 250V CDM allows safe manufacturing with a standard ESD control process.

Thermal information

Table 5. Thermal Information

Parameter	Symbol	TBD	Units
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	TBD	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	TBD	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	TBD	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	TBD	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	TBD	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	—	°C/W

Electrical characteristics

The electrical characteristics of the HX7606-Q. AVCC = 4.75V to 5.25V,VDRIVE = 2.3V to 5.25V, 200kSPS sampling rate, single-ended input, 2.5V internal reference voltage, unless otherwise noted.

Table 6. Electrical Characteristics

Parameter	Symbol	CONDITIONS	Min	Typ	Max	Units
Resolution				16		Bits
Differential Nonlinearity	DNL	25°C		±2		LSB
Integral Nonlinearity	INL	25°C		±4		LSB
Input Impedance		25°C		1		MΩ
Analog Input Range		+10V	−10		10	V
		+5V	−5		5	V
Input Capacitance				5		pF
Supply Voltage	AVCC		4.75	5	5.25	V
	VDRIVE		2.3		5.25	V
Supply Current	I_{AVCC}			20		mA
	I_{VDRIVE}			1.1		mA
Power Dissipation		Normal mode		100		mW
		Standby mode, 25°C		2		mW
		Power-down mode, 25°C		2.5	25	μW
Signal-to-Noise Ratio(1)	SNR	No oversampling, ±10V range		85		dB
		No oversampling, ±5V range		TBD		dB
		Oversampling, OSR = 16×, ±10V range		91.5		dB
		Oversampling, OSR = 16×, ±5V range		TBD		dB
Spurious Free Dynamic Range	SFDR	25°C		72		dB
Reference Temperature Drift				±3.5		ppm/°C

Note: Measured with 1kHz input frequency, full-scale sine wave.

Digital specifications

The digital specifications of the HX7606-Q. AVCC = 4.75V to 5.25V, VDRIVE = 2.3V to 5.25V, 200kSPS sampling rate, single-ended input, 2.5V internal reference voltage, unless otherwise noted.

Table 7. Digital Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LOGIC INPUT						
Logic 1 Voltage			0.7 × VDRIVE			V
Logic 0 Voltage			0		0.3 × VDRIVE	V
Input Current					±1	μA
Input Capacitance				5		pF
DIGITAL OUTPUT						
Logic 1 Voltage			VDRIVE - 0.2			V
Logic 0 Voltage					0.2	V
Coding Format (Default)				Two's complement		

Time requirement

General interface timing requirements

The timing requirements of the HX7606-Q. AVCC = 4.75V to 5.25V, VDRIVE = 2.3V to 5.25V, 200kSPS sampling rate, single-ended input, 2.5V internal reference voltage, unless otherwise noted. Test the interface timing with a 20pF load capacitance, depending on the load capacitance of VDRIVE and the serial interface.

Table 8. Universal Interface Timing Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum Time Between Consecutive CONVST Rising Edges (Excluding Oversampling Mode)	t_{CYCLE}				5	μs
CONVST Low-Level Pulse Width	t_{LP_CNV}		25			ns
CONVST High-Level Pulse Width	t_{HP_CNV}		25			ns
Delay Time from CONVST High Level to BUSY High Level	$t_{D\_CNV\_BSY}$				40	ns
Settling Time from Falling Edge of BUSY to Falling Edge of CS	$t_{S\_BSY\_CS}$		0			ns
Maximum Delay Time Between Rising Edges of CONVST A and CONVST B	$t_{D\_CNVA\_CNVB}$				0.5	ms
Maximum Interval Time from the Rising Edge of CS to the Falling Edge of BUSY	t_{CS_BSY}				25	ns
Conversion Time, No Oversampling	t_{CONV}			4		μs
Conversion Time, 2× Oversampling				9		μs
Conversion Time, 4× Oversampling				19		μs
Conversion Time, 8× Oversampling				39		μs
Conversion Time, 16× Oversampling				79		μs
Conversion Time, 32× Oversampling				159		μs
Conversion Time, 64× Oversampling				319		μs
RESET High-Level Pulse Width	t_{RESET}		50			μs
Time Between RESET Falling Edge and First CONVST Rising Edge	t_{DEVICE_SETUP}		25			ns
Wakeup Time after Standby Mode	t_{WAKE_UP}				100	μs
		Internal reference voltage			30	ms
Wakeup Time after Power-Down Mode	t_{WAKE_UP}	External reference voltage			13	ms

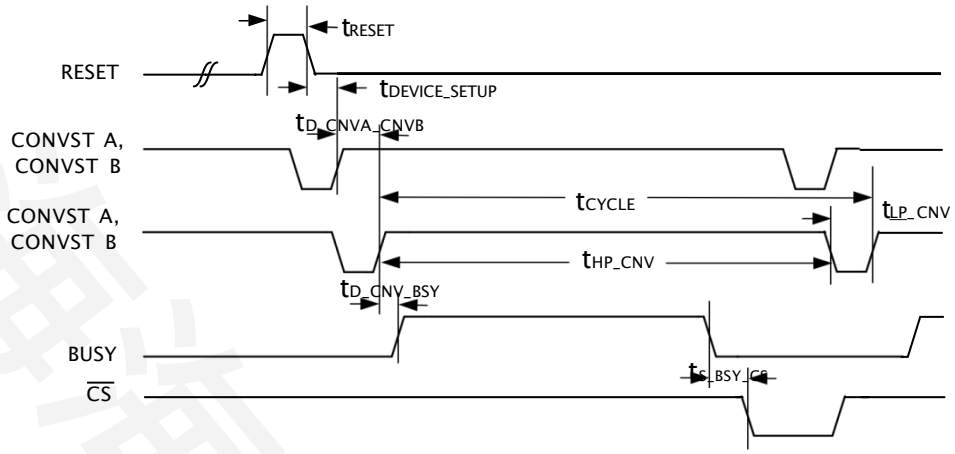


Figure 2. Conversion Timing Diagram (Read Data after Conversion)

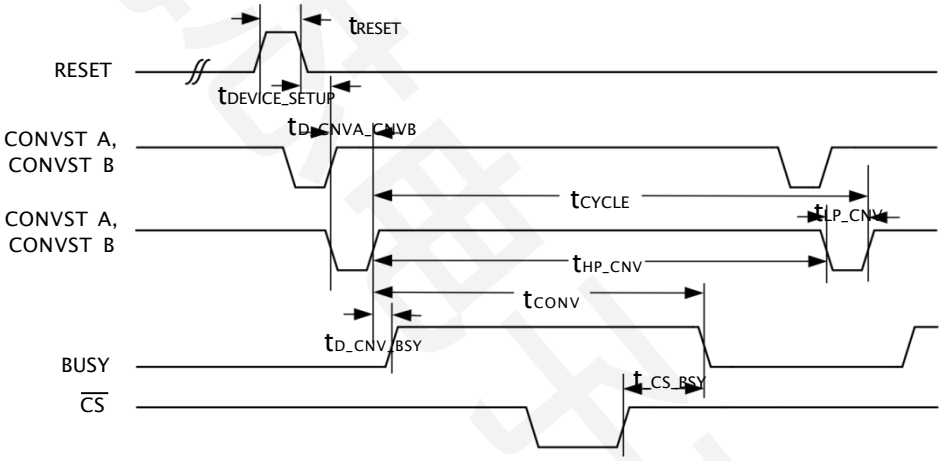


Figure 3. Conversion Timing Diagram (Read Data during Conversion)

Parallel interface timing requirements

Table 9. Parallel Interface Timing Requirements

Parameter	Symbol	ConditIons	Min	Typ	Max	Units
CS Falling Edge to RD Falling Edge Settling Time	$t_{S\_CS\_RD}$		0			ns
RD Rising Edge to CS Rising Edge Hold Time	$t_{H\_RD\_CS}$		0			ns
$\overline{RD}$ High-Level Pulse Width	t_{HP_RD}		15			ns
$\overline{RD}$ Low-Level Pulse Width	t_{LP_RD}		16			ns
CS High-Level Pulse Width	t_{HP_CS}		22			ns
Delay Time from CS to DBx Tri-State Disable	$t_{D\_CS\_DB}$				16	ns
CS to DBx Hold Time	$t_{H\_CS\_DB}$		6			ns
Data Transfer Time after Falling Edge of RD	$t_{D\_RD\_DB}$				16	ns
Data Hold Time after Falling Edge of $\overline{RD}$	$t_{H\_RD\_DB}$		6			ns
Delay Time from $\overline{CS}$ Rising Edge to DBx Tri-State Enable	$t_{DHZ\_CS\_DB}$				22	ns
Delay Time from CS Falling Edge to FRSTDATA Tri-State Disable	$t_{D\_CS\_FD}$				15	ns
Delay Time from Falling Edge of $\overline{CS}$ to High Level of FRSTDATA	$t_{D\_CS\_FDH}$				15	ns
Delay Time from Falling Edge of RD to High Level of FRSTDATA	$t_{D\_RD\_FDH}$				16	ns
Delay Time from Falling Edge of RD to Low Level of FRSTDATA	$t_{D\_RD\_FDL}$				19	ns
Delay Time from $\overline{CS}$ Rising Edge to FRSTDATA Tri-State Enable	t_{DHZ_FD}				24	ns
Delay Time from the 16th SCLK Falling Edge to Low Level of FRSTDATA	$t_{D\_SCK\_FDL}$				17	ns

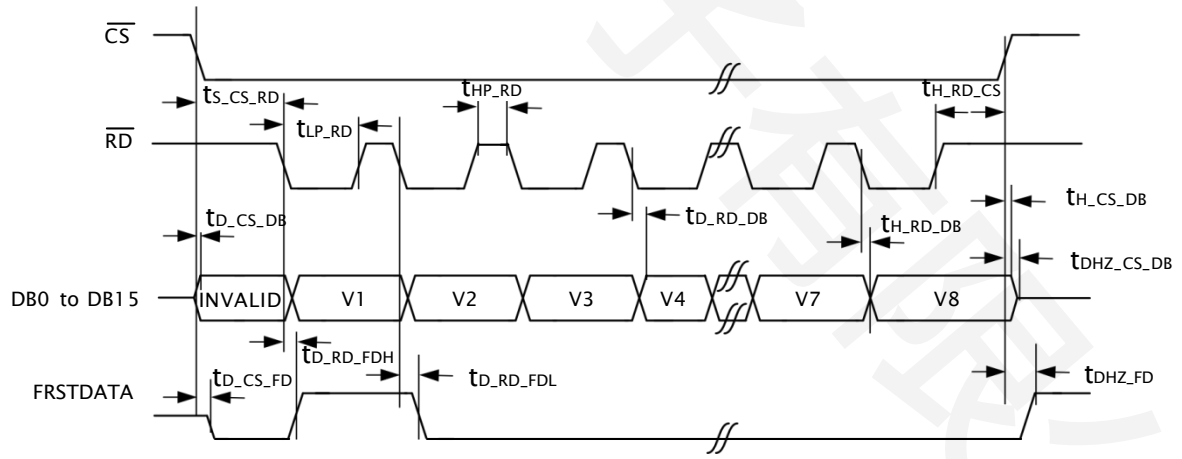


Figure 4. Parallel Interface Read Timing Diagram (Separate $\overline{CS}$ and $\overline{RD}$ Pulses)

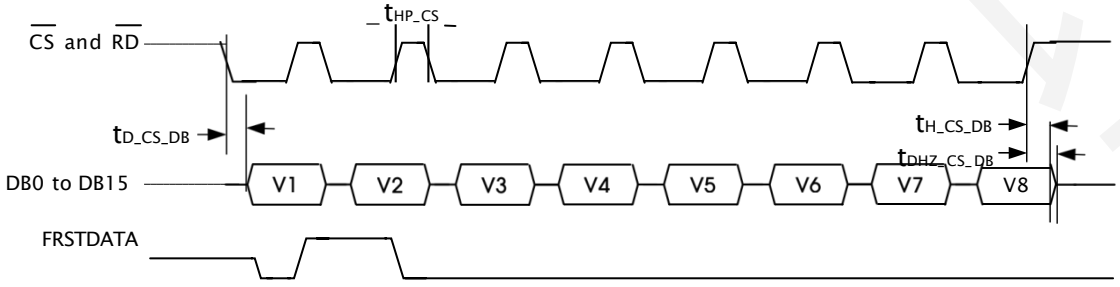


Figure 5. Parallel Interface Read Timing Diagram (Connected $\overline{CS}$ and $\overline{RD}$ Pulses)

Serial interface timing requirements

Table 10. Serial Interface Timing Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCLK Frequency	f_{SCLK}	$f_{SCLK} = 1 / t_{SCLK}$			30	MHz
Minimum SCLK Period	t_{SCLK}		$1 / f_{SCLK}$			µs
$\overline{CS}$ to SCLK Falling Edge Settling Time	$t_{S\_CS\_SCK}$		2			ns
SCLK to CS Rising Edge Hold Time	$t_{H\_SCK\_CS}$		2			ns
SCLK Low-Level Pulse Width	t_{LP_SCK}		$0.4 \times t_{SCLK}$			ns
SCLK High-Level Pulse Width	t_{HP_SCK}		$0.4 \times t_{SCLK}$			ns
Delay Time from CS Rising Edge to DOUTx Tri-State Enable	$t_{DHZ\_CS\_DO}$				22	ns
DOUTx Data Transfer Time after SCLK Rising Edge	$t_{D\_SCK\_DO}$				17	ns
DOUTx Output Data Hold Time after SCLK Rising Edge	$t_{H\_SCK\_DO}$		7			ns
Delay Time from CS to DOUTx Tri-State Disable or from CS to MSB Valid	$t_{D\_CS\_FD}$				15	ns

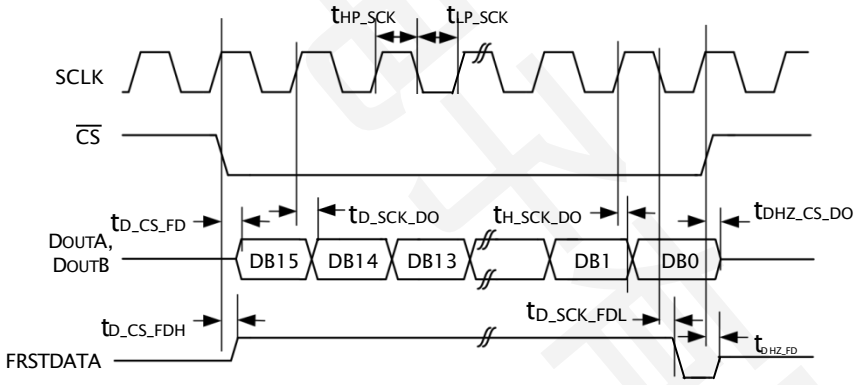


Figure 6. Serial Interface Timing Diagram, ADC Read Mode (Channel 1)

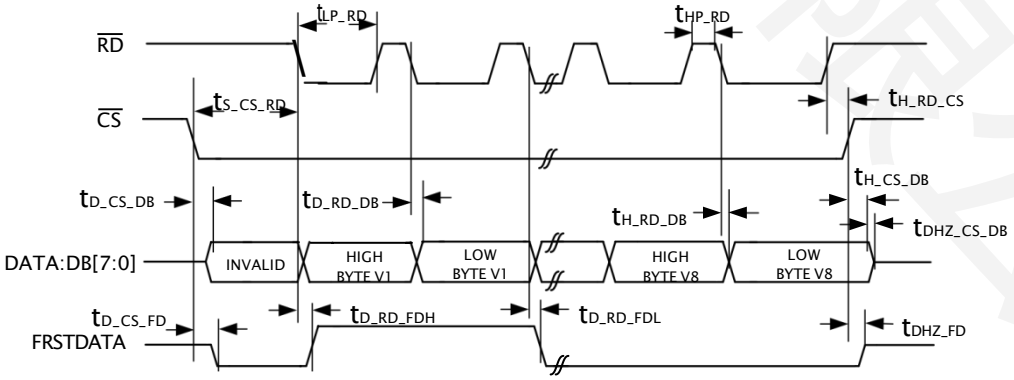


Figure 7. Serial Interface Timing Diagram, Byte Mode Read Operation

Detailed description

Block diagram of functional modules

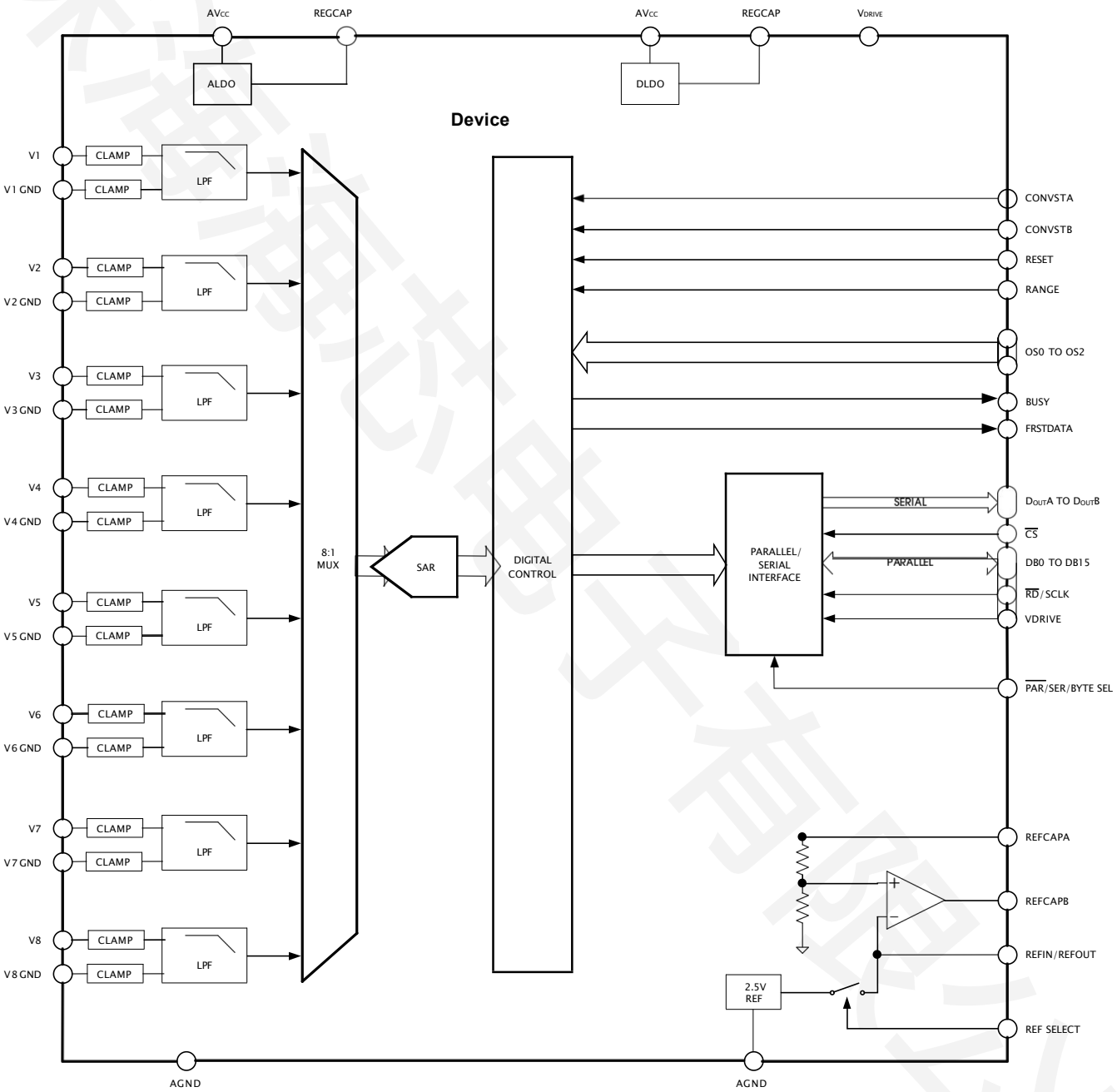


Figure 8. Functional Block Diagram

Characteristic description

Internal/external reference voltage

The HX7606-Q has two reference voltage modes: internal and external. When the REF SELECT pin is set to a high level, the internal reference mode is enabled, and the internal reference source provides the reference voltage. When the REF SELECT pin is set to low power, the internal reference is disabled and the external reference voltage can be input.

External reference mode

The external reference mode configuration of HX7606-Q is shown in the following figure.

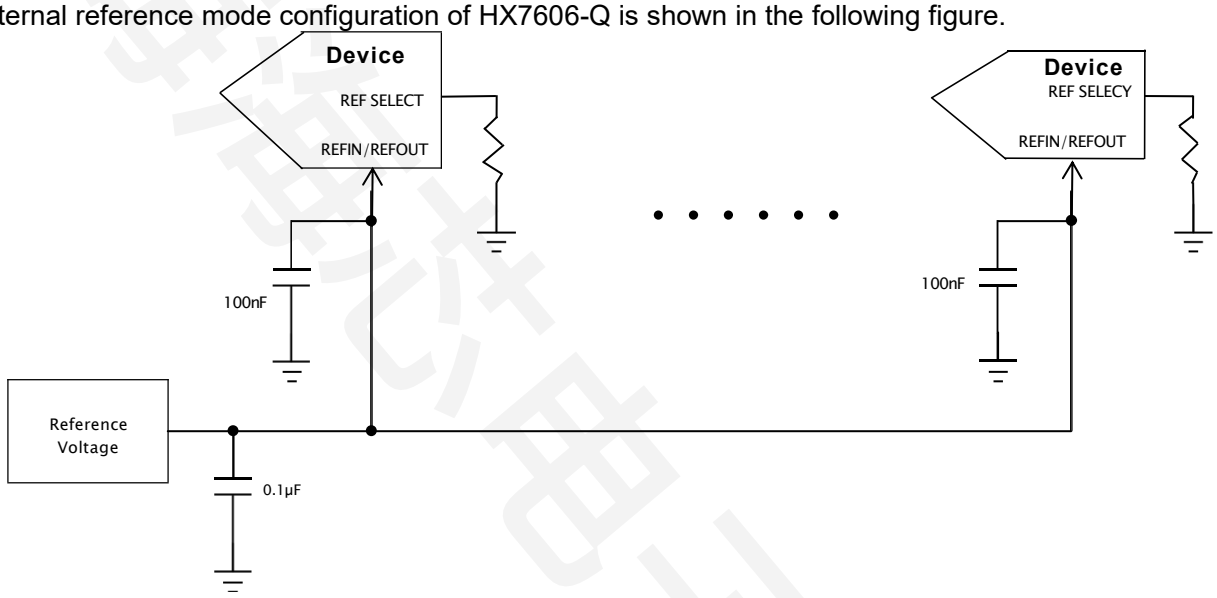


Figure 9. Single External Reference Driving Multiple HX7606-Q REFIN Pins

Internal reference mode

The internal reference mode configuration of HX7606-Q is shown in the following figure.VDRIVE

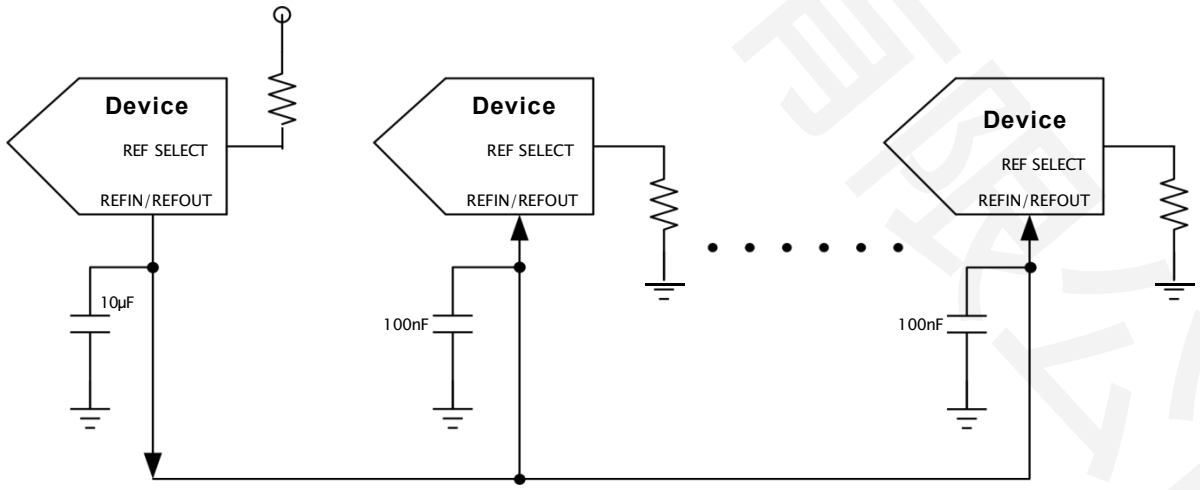


Figure 10. Internal Reference Driving Multiple HX7606-Q REFIN Pins

Power mode selection

The HX7606-Q has two power modes, namely normal operation mode (±5V, ±10V input) and power-saving mode (standby and off), which are controlled by the STBY and RANGE pins. The configuration relationship is shown in the table below.Table 11. Power Mode Select

Power Mode	Stby	Range
Power-Down	0	0
Standby	0	1
±5V Input Range	1	0
±10V Input Range	1	1

Conversion control

The rising edge of CONVST A enables the sampling-hold circuits of channels V1-V4 to enter the hold mode, and the rising edge of CONVST B enables the sampling-hold circuits of channels V5-V8 to enter the hold mode, achieving the synchronous sampling function. When the rising edges of both CONVSTA and CONVSTB arrive, the transformation process begins.

The BUSY signal represents the conversion process. When this signal drops the edge, the pick-hold circuit returns to the sampling mode, and the new data can be read from DB[15:0].

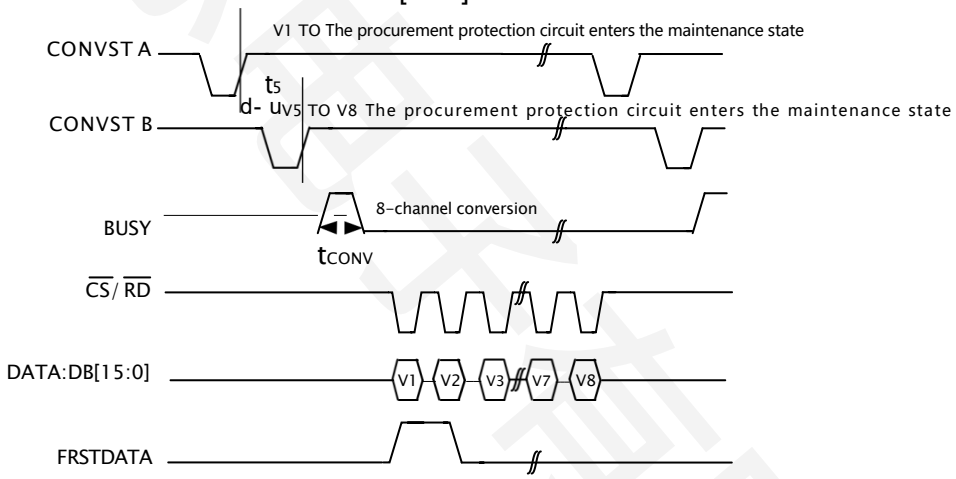


Figure 11. Simultaneous Sampling of Channel Sets when Using Separate CONVST A and CONVST B Signals (Parallel Mode)

Digital interface

The HX7606-Q has three interfaces to choose from: parallel interface, high-speed serial interface, and parallel byte interface. The three modes are controlled by two sets of pins, $\overline{\text{PAR}}$/SER/BYTESEL and DB15/BYTESEL. The configuration relationship is shown in the following table.

Table 12. Interface Mode Select

PAR/SER/BYTE SEL	DB15	INTERFACE
0	0	Parallel
1	0	Serial

Oversampling coding mode

Table 13. Over-Sampling Encoding

OS[2:0]	OS RATIO	SNR 5V Range (dBFS)	SNR 10V Range (dBFS)	3dB BW 5V Range (kHz)	3dB BW 10V Range (kHz)	HIGHEST CONVERSION RATE (kHz)
000	No OS	86.0	86.31	15	22	200
001	2	87.6	86.62	15	22	100
010	4	89.5	89.03	13.7	18.5	50
011	8	91.9	91.53	10.3	11.9	25
100	16	93.7	91.51	6	6	12.5
101	32	95.1	92.85	3	3	6.25
110	64	95.4	95.08	1.5	1.5	3.125
111	Invalid	—	—	—	—	—

Typical applications

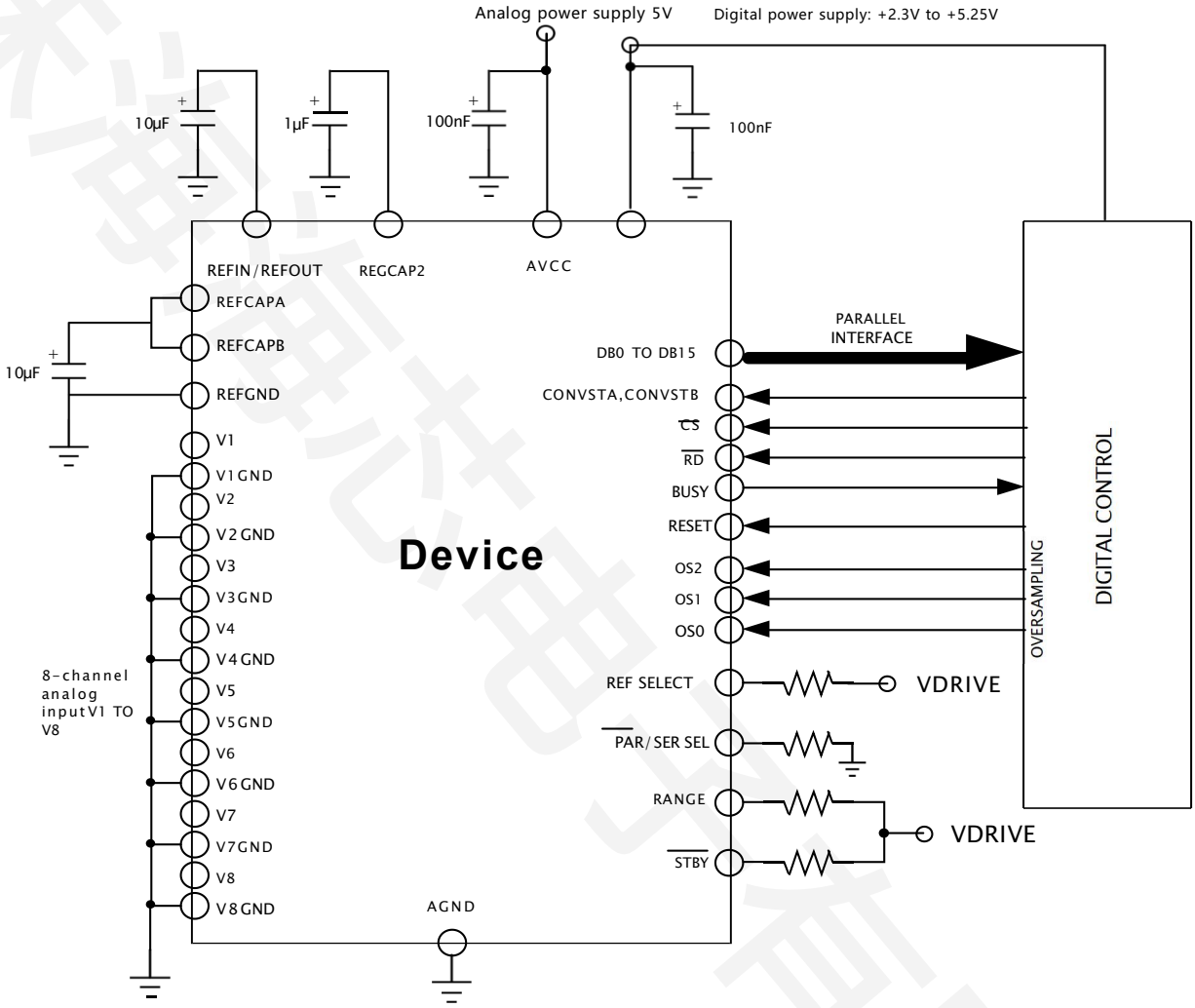


Figure 12. Typical Connection

Packet information

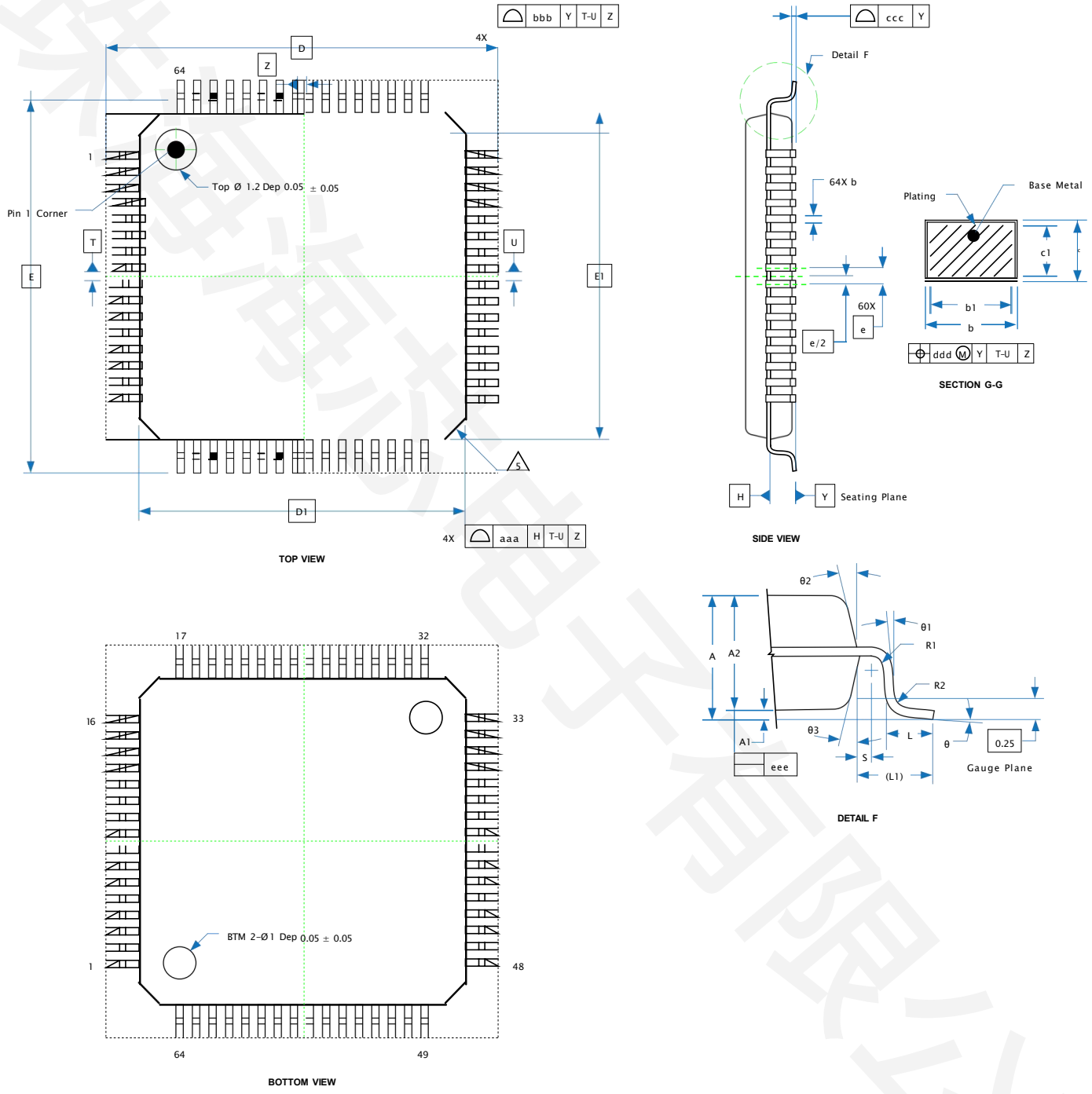


Figure 13. Package View

Table 14. provides detailed information about the dimensions.

Parameter		Symbol	Dimensions in Millimeters		
			Min	Nom	Max
Total Thickness		A	—	—	1.6
Stand Off		A1	0.05	—	0.15
Mold Thickness		A2	1.35	1.4	1.45
Lead Width (Plating)		b	0.18	0.22	0.26
Lead Width		b1	0.17	0.2	0.23
L/F Thickness (Plating)		c	0.13	—	0.17
L/F Thickness		c1	0.12	0.127	0.134
	X	D		12 BSC	
	Y	E		12 BSC	
Body Size	X	D1		10 BSC	
	Y	E1		10 BSC	
Lead Pitch		e		0.5 BSC	
		L	0.45	0.6	0.75
Footprint		L1		1 REF	
		θ	0°	3.5°	7°
		θ1	0°	—	—
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	—	—
		R2	0.08	—	0.2
		S	0.2	—	—
Package Edge Tolerance		aaa		0.2	
Lead Edge Tolerance		bbb		0.2	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.08	
Mold Flatness		eee		0.05	