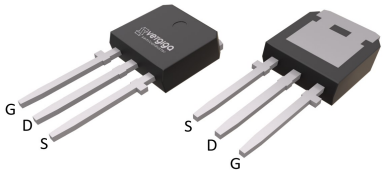
V_{DS}	100	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	8	mΩ
$I_{D(Wire\ bond\ limited)}$	56	A

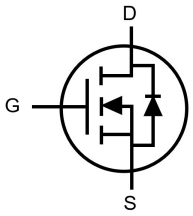
Features

- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=10 V
- VitoMOS® Ⅱ Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

QIPAK



Pb-Free RoHS HF Halogen-Free



Part ID	Package Type	Marking	Packing
VSI008N10MS3-K	QIPAK	008N10M	75pcs/Tube

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current (Wire bond limited)	T_C =25°C	56	A
I_D	Continuous drain current @VGS=10V (Wire bond limited)	T_C =25°C	56	A
	Continuous drain current @VGS=10V (Silicon limited)	T_C =100°C	53	A
I_{DM}	Pulse drain current tested ①	T_C =25°C	296	A
I_{DSM}	Continuous drain current @VGS=10V	T_A=25°C	9	A
		T_A=70°C	7	A
V_{SPIKE}	V_{DS} Spike(t=10us)		120	V
EAS	Avalanche energy, single pulsed ②		25	mJ
P_D	Maximum power dissipation	T_C =25°C	88	W
P_{DSM}	Maximum power dissipation ③	T_A=25°C	1.3	W
T_{STG},T_J	Storage and Junction Temperature Range		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.7	2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	120	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.4	1.8	2.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance ④	V_{GS}=10V, I_D=35A	--	8	10	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	1250	1470	1690	pF
Coss	Output Capacitance		595	690	795	pF
Crss	Reverse Transfer Capacitance		15	25	35	pF
Rg	Gate Resistance	f=1MHz	0.2	1.0	3	Ω
Qg	Total Gate Charge	V_{DS}=50V,I_D=35A, V_{GS}=10V	--	24	32	nC
Qgs	Gate-Source Charge		--	4.9	6.5	nC
Qgd	Gate-Drain Charge		--	5.1	7.7	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V_{DD}=50V, I_D=30A, R_G=3Ω, V_{GS}=10V	--	8	--	ns
Tr	Turn-on Rise Time		--	35	--	ns
Td(off)	Turn-Off Delay Time		--	20	--	ns
Tf	Turn-Off Fall Time		--	26	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=35A,V_{GS}=0V	--	0.9	1.2	V
Trr	Reverse Recovery Time	T_j=25℃,I_{sd}=35A, V_{GS}=0V di/dt=100A/μs	--	47	94	ns
Qrr	Reverse Recovery Charge		--	52	104	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH,R_G = 25Ω, I_{AS} = 10A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

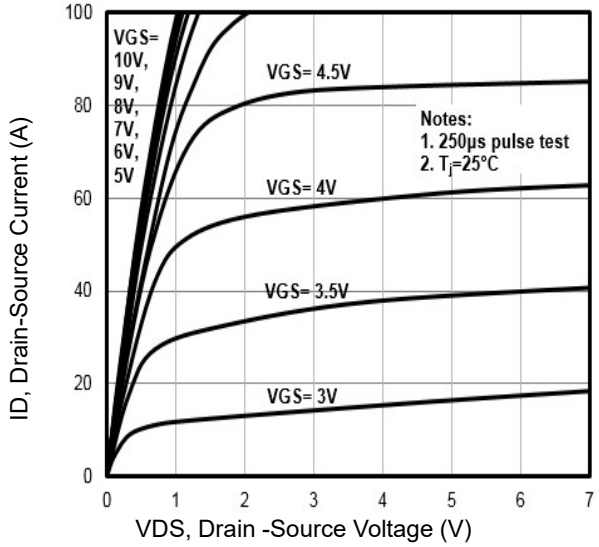


Fig1. Typical Output Characteristics

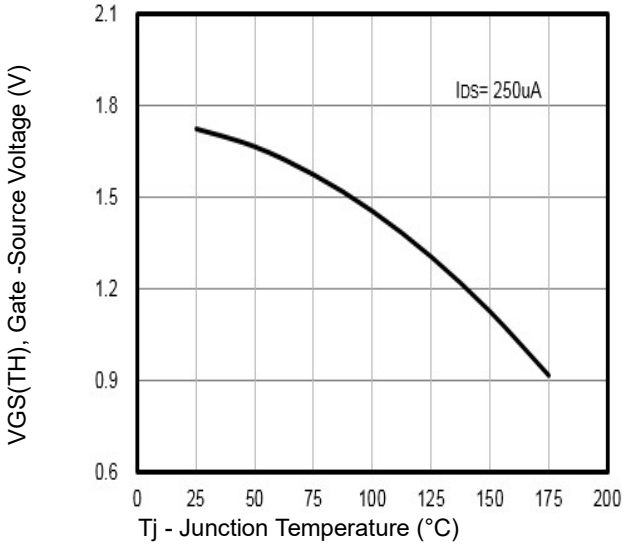


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

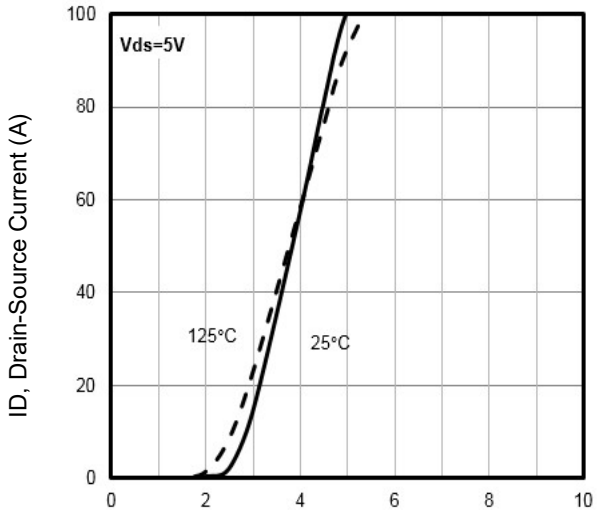


Fig3. Typical Transfer Characteristics

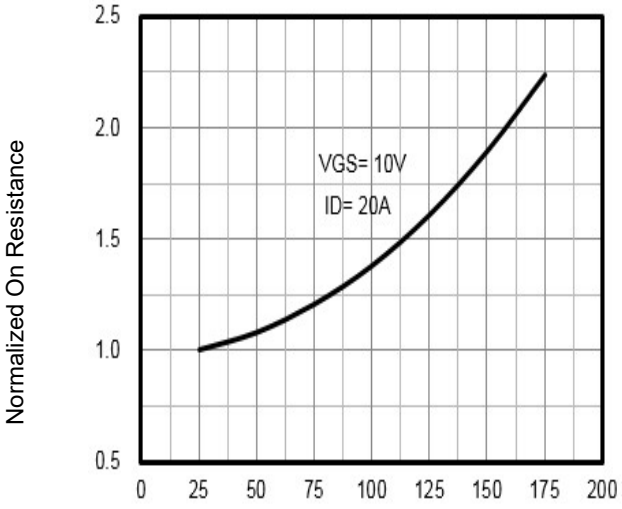


Fig4. Normalized On-Resistance Vs. Tj

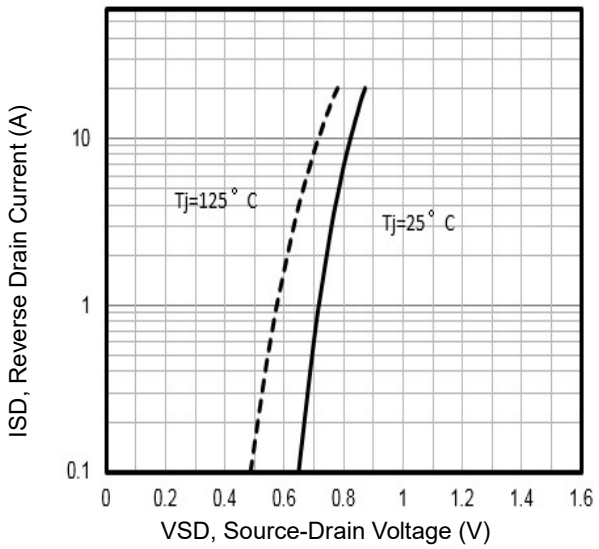


Fig5. Typical Source-Drain Diode Forward Voltage

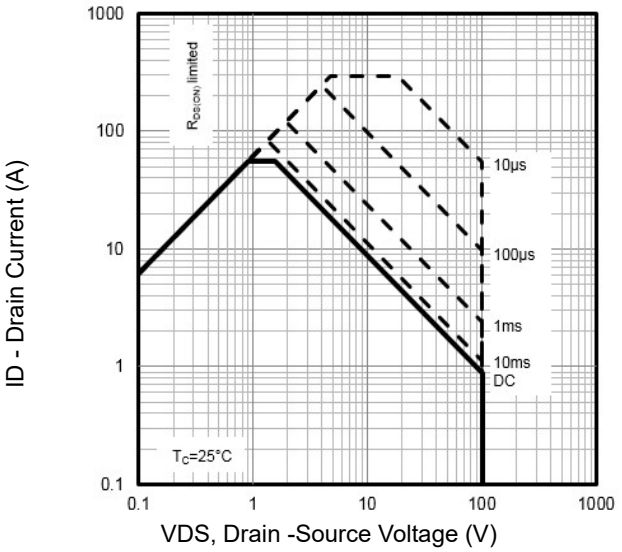


Fig6. Maximum Safe Operating Area

Typical Characteristics

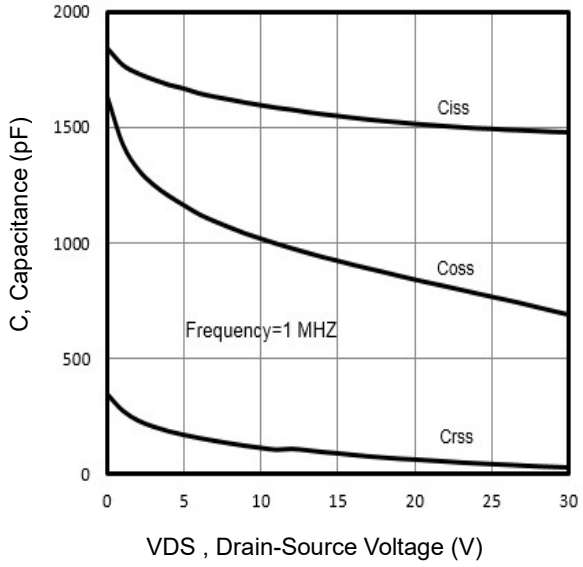


Fig7. Typical Capacitance Vs.Drain-Source Voltage

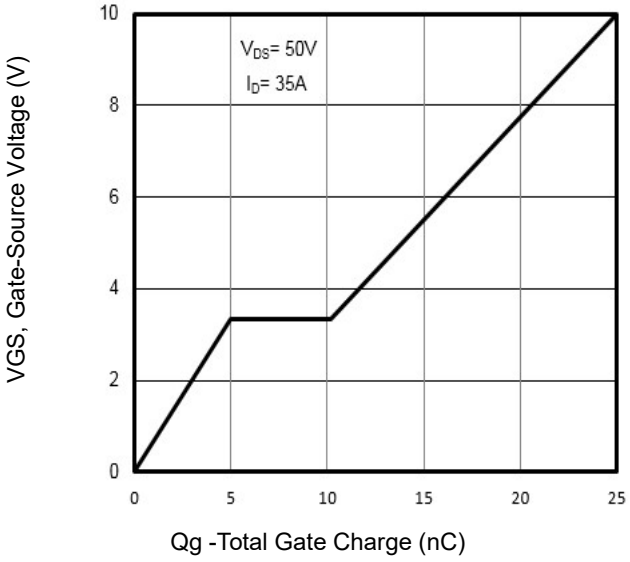


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

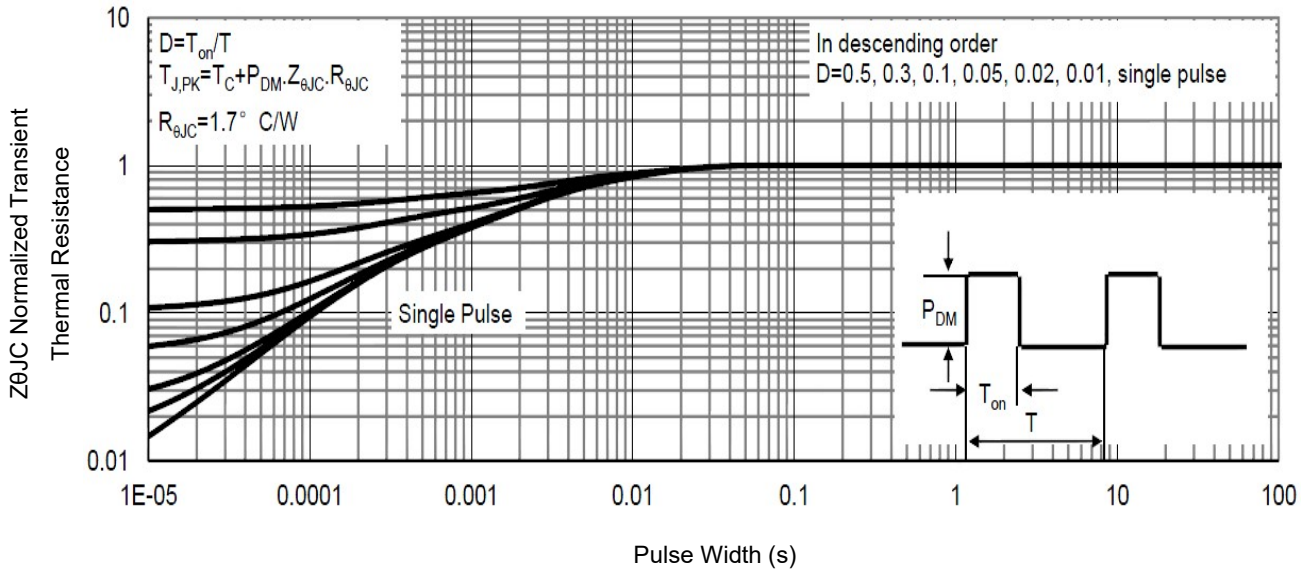


Fig9. Normalized Maximum Transient Thermal Impedance

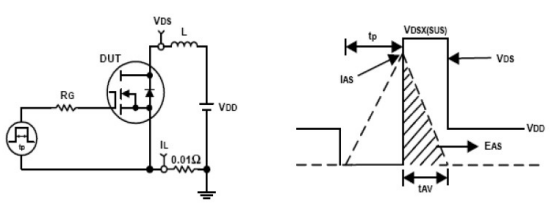


Fig10. Unclamped Inductive Test Circuit and waveforms

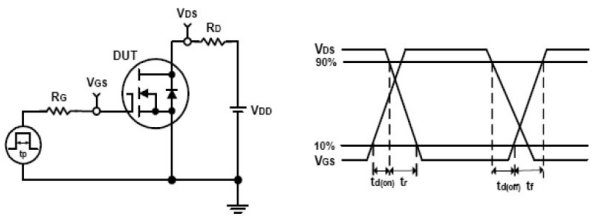
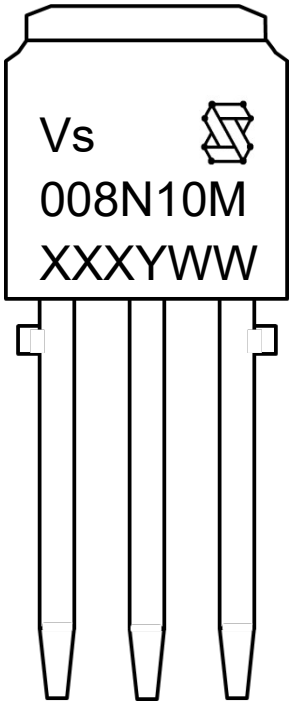


Fig11. Switching Time Test Circuit and waveforms

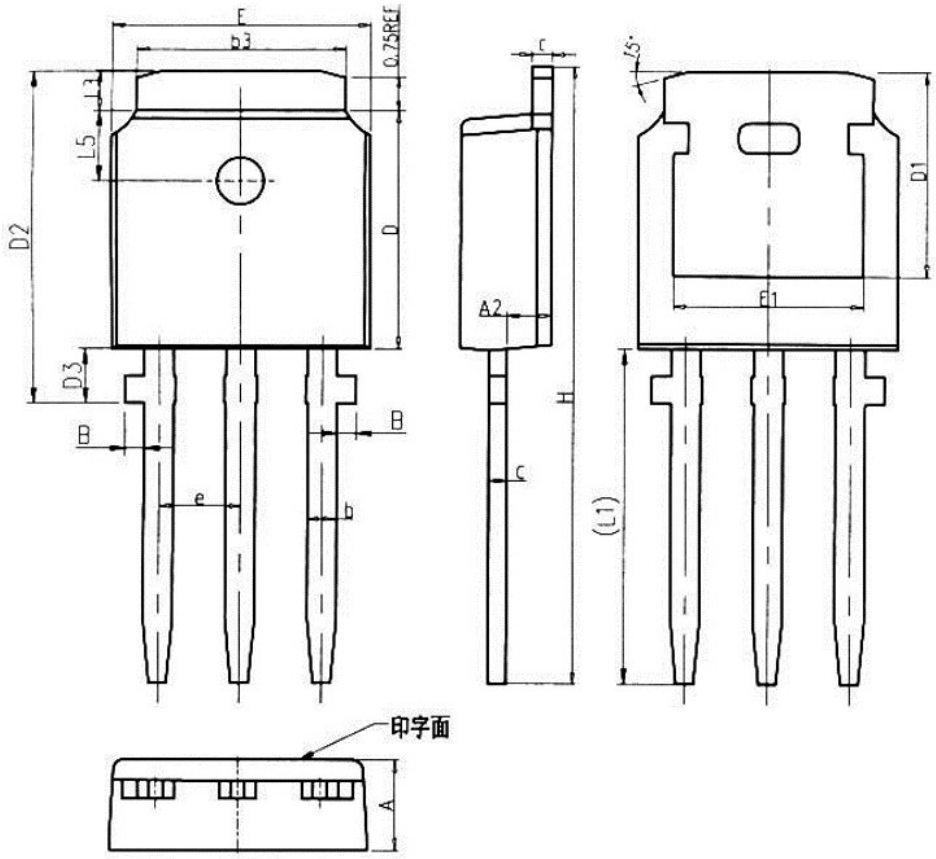
Marking Information(for E)



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（008N10M）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code，code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

QIPAK Package Outline Data(for E)



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.40
A2	0.97	1.07	1.17
B	0.25	0.40	0.55
b	0.68	0.78	0.85
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1	5.30 REF		
D2	7.96	8.16	8.36
D3	0.85	1.05	1.25
E	6.40	6.60	6.80
E1	4.63	--	--
e	2.286 BSC		
H	16.22	16.52	16.82
L1	9.15	9.40	9.65
L3	0.88	1.02	1.28
L5	1.65	1.80	1.95

Note:
Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Customer Service

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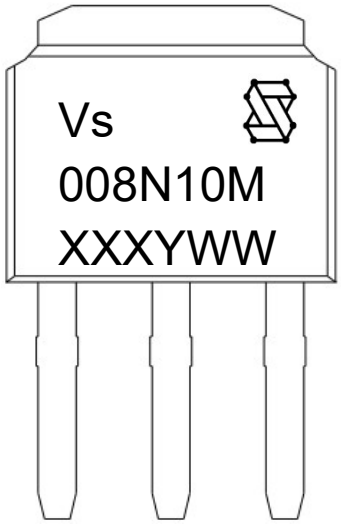
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: www.vergiga.com

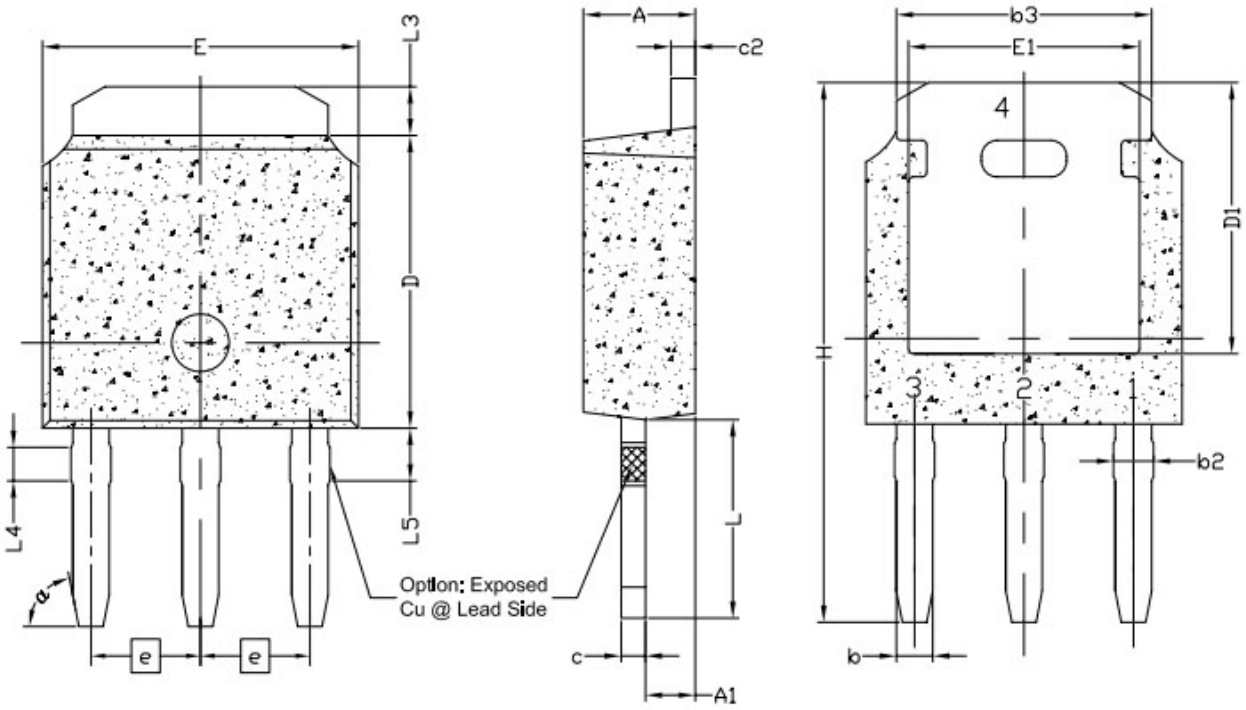
Marking Information(for M)



1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（008N10M）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

QIPAK Package Outline Data(for M)



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.39
A1	0.89	1.04	1.15
b	0.64	0.76	0.89
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
c	0.46	0.50	0.60
c2	0.46	0.50	0.60
D	5.98	6.10	6.223
D1	5.10	--	--
E	6.40	6.60	6.731
E1	4.40	--	--
e	2.286 BSC		
H	11.05	11.25	11.45
L	3.98	4.13	4.35
L3	0.89	--	1.27
L4	0.698 REF		
L5	0.972	1.099	1.226
α	79° REF		

Notes:

1. Dimension "D" and "E" do NOT include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.1mm per side.

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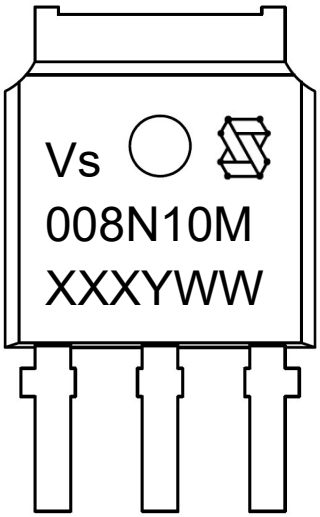
Marking Information(for PT)



1st line: Vergiga Code（Vs）， Vergiga Logo
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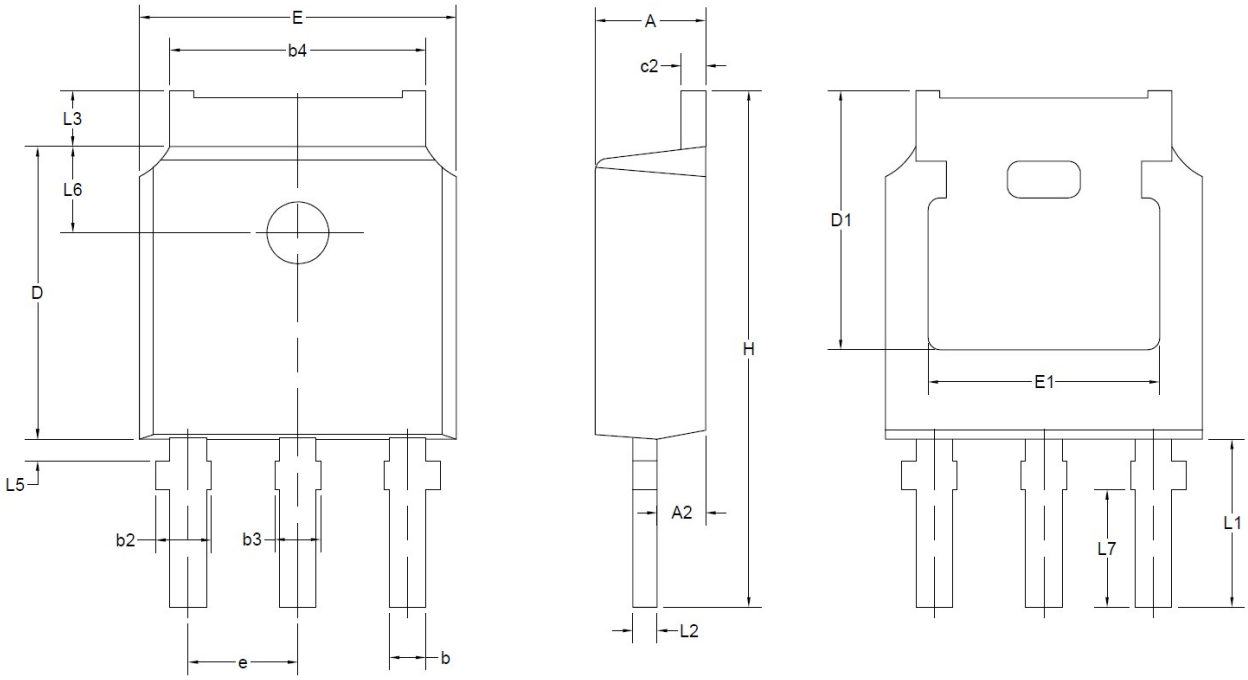
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

QIPAK Package Outline Data(for PT)



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A2	0.90	1.01	1.10
b	0.72	--	0.85
b2	1.00	--	1.30
b3	0.72	--	1.00
b4	5.13	5.33	5.46
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1	5.25	--	--
E	6.50	6.60	6.70
E1	4.70	--	--
e	2.186	2.286	2.386
H	10.40	10.70	11.00
L1	3.35	3.50	3.75
L2	0.508 BSC		
L3	0.90	--	1.25
L5	0.15	--	0.75
L6	1.80 REF		
L7	2.35	--	2.55

Notes:

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