16V 1A 1MHz Sync Step-Down Dimmable LED Driver

Features

- Wide 4.5V to 16V Operating Input Range
- 1A Continuous Output Current
- Fixed 1MHz Switching Frequency
- Over temperature protection
- Built-in Over Current Limit
- Built-in Over Voltage Protection
- Internal Soft-Start
- 120mΩ/70mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High Efficiency
- PWM and Analog Dimming
- Thermal Shutdown
- Available in SOT23-6 Package
- -40°C to +85°C Temperature Range

Applications

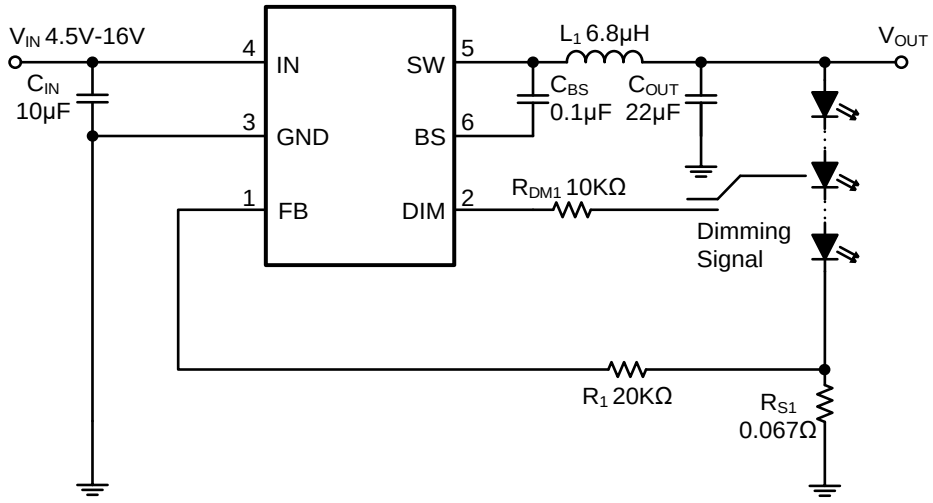
- CCTV/IP Camera
- Automotive/Decorative LED Lighting
- Low-Voltage Halogen Replacement
- Signs/Emergency Lighting
- LED Backlighting
- Low-Voltage General Illumination

General Description

The RY7117 is step-down regulator for dimmable LED driver, which is designed in continuous current mode for driving the high-brightness LEDs from a wide input voltage of 4.5V to 16V. It supports the analog dimming signal 0.65V-1.2V to achieve dimmable LED lighting application. The RY7117 includes under-voltage lockout and thermal overload protection to prevent damage in the event of an output overload.

The RY7117 requires a minimal number of readily available external components and is available in a space saving SOT23-6 package.

Typical Application Circuit



Typical Application Circuit

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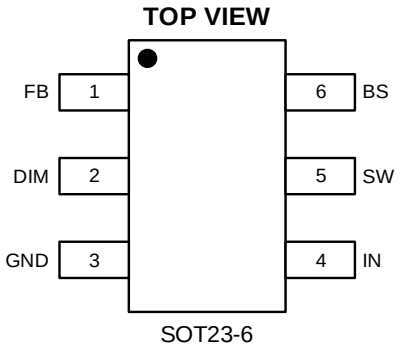
Package and Pin Description

Pin Configuration



Top Marking: JNYLL (device code: JN, Y=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	FB	Output current feedback pin, the output current: I_{OUT}=0.1V/R_{S1}.
2	DIM	Dimming signal input, the dimming voltage range: 0.65V-1.2V. Should not be float.
3	GND	Ground pin.
4	IN	Input supply pin, decouple this pin to GND pin with a 10μF ceramic cap.
5	SW	Switching Pin, connect this pin to the indicator.
6	BS	Bootstrap pin, supply for top side gate driver, decouple this pin to SW with 0.1μF ceramic cap.

Order Information (1)

Marking	Part No.	Model	Description	Package	T/R Qty
JNYLL	70380003	RY7117AT6	RY7117AT6 Sync dimmable LED driver IC, 4.5-16V, 1A, 1MHz, SOT23-6	SOT23-6	3000PCS

Note (1): All RYCHIP parts are Pb-Free and adhere to the RoHS directive.

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Specifications

Absolute Maximum Ratings (1)(2)

Item	Min	Max	Unit
V_{IN} voltage	-0.3	20	V
DIM voltage	-0.3	20	V
SW voltage	-0.3	20	V
SW voltage (10ns transient)	-5	20	V
BS voltage	-0.3	20	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	–55	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 140°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD\text{-}HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD\text{-}CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH\text{-}UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	4.5	16	V
Output current	0	1	A

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard

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Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	105	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1) (2)

V_{IN}=12V, T_A=25°C, unless otherwise specified.

Parameter	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range		4.5		16	V
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		4.1	4.4	V
	Shutdown V_{IN} Voltage	3.3	3.7		V
	Hysteresis V_{IN} voltage		400		mV
Shutdown Supply Current			170	250	μA
Quiescent Current	V_{DIM}=2V, V_{FB}=0.105V		2.5		mA
Over Input Voltage			31.4		V
Feedback Reference Voltage	V_{DIM}=1.2V	94	100	106	mV
Feedback Min Reference Voltage	V_{DIM}=0.65V	3	5	7	mV
High-Side FET On-Resistance		100	120	140	mΩ
High-Side FET Peak Current Limit	T_{ON}<300nS	2.3	2.6	3	A
Low-Side FET On-Resistance		60	70	80	mΩ
Low-Side FET Valley Current Limit		1.5	1.8	2.1	A
Analog Dimming Voltage		0.65		1.2	V
Dimming ON Threshold				0.67	V
Dimming OFF Threshold		0.55			V
Bias Voltage For High FET Driver	4.5V≤V_{IN}≤16V		3		V
Operation Frequency		0.8	1.0	1.2	MHz
Minimum On Time			80	100	nS
Minimum Off Time			80	100	nS
Max Duty Cycle			85%		
Thermal Shutdown			160		℃
Thermal Hysteresis			20		℃

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis

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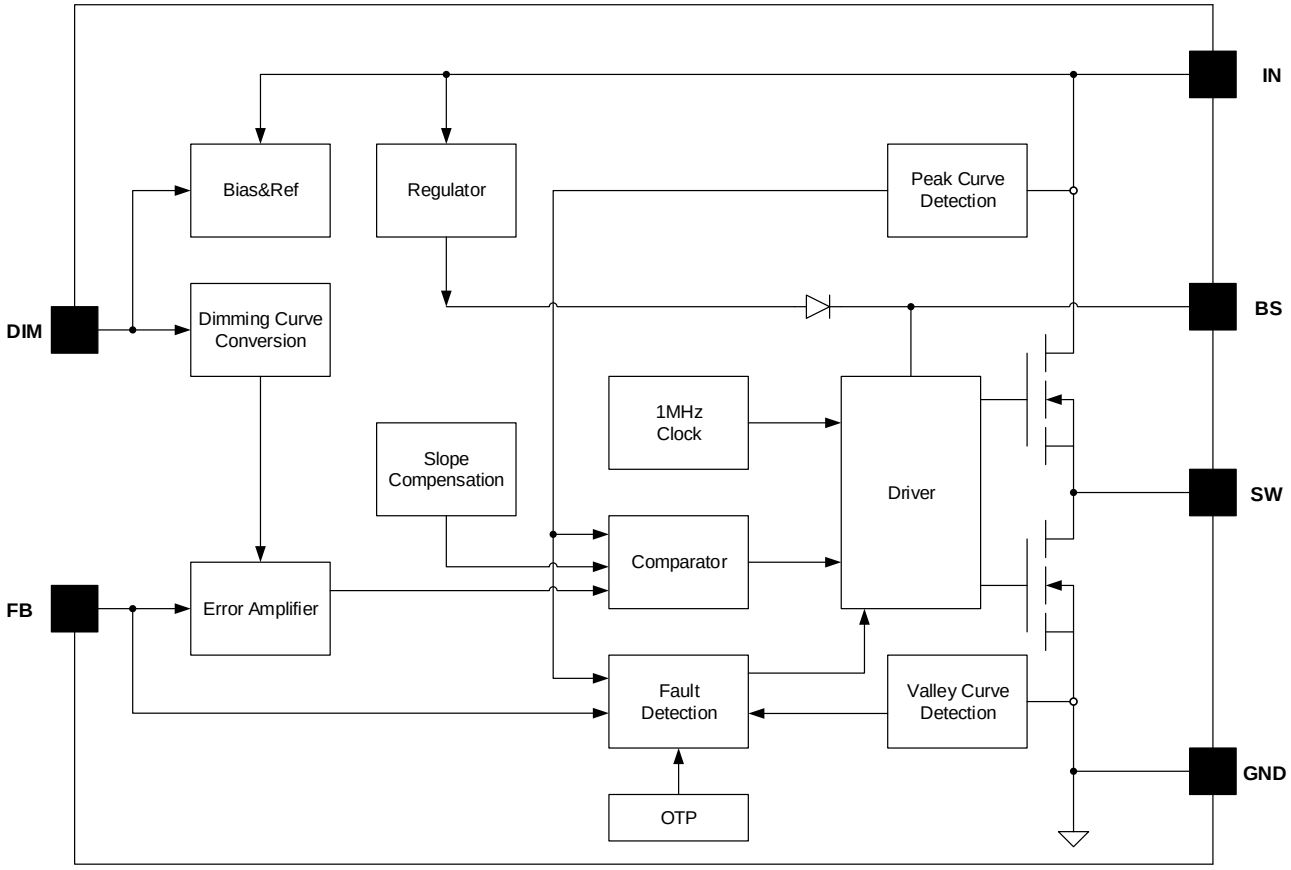
Functional Block Diagram



Block Diagram

Functions Description

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, 4.1V(typical), the device is shut off. The UVLO threshold has approximately 400mV of hysteresis, so the part operates until VIN drops below 3.7V(typical). Hysteresis prevents the part from turning off during power up if VIN is non-monotonic.

Dimming and Enable/Disable

When the input voltage is above maximal UVLO rising threshold and the DIM pin is pulled high (above 1.2V), the RY7117 is enabled. When the DIM pin is pulled low (below 0.55V), the RY7117 goes into shutdown mode. In shutdown mode, less than 1μA input current is consumed. The DIM pin allows disabling and enabling of the device as well as brightness control of the LEDs by applying a PWM signal. When a PWM signal is applied, the LED current is turned on when the DIM is high and off when DIM is pulled low. Changing the PWM duty cycle therefore changes the LED brightness. Meanwhile, add a 0.65V to 1.2V voltage to the DIM to adjust the LED current linearly. When dimming is not needed, we can connect DIM and VIN through a resistor.

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Peak Current Limit Mode

The RY7117 has both a peak current limit mode and a valley current limit mode to protect the chip from overcurrent damage. The device implements current-mode control, which uses the internal COMP voltage to control the turn-off of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference, the high-side switch turns off. During overcurrent conditions, such as when the sensing resistor is shorted, or an open circuit occurs in the feedback-filter RC network that drives FB low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch-current limit. This current limit is fixed at 2.6A (typical).

Valley Current Limit

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing-current limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle.

LED-Open

When the LED load is open, the FB voltage is low, and the internal COMP voltage is driven high and clamped, then output rises close to the input. At this time, the chip does not have load capacity.

LED Short Protection

When LED+ and LED- are shorted, the output current will be limited to near VFB/R_{S1}. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold. Once a UV is triggered, the RY7117 enters hiccup mode to periodically restart the part. At this time, the output voltage is close to VFB.

LED+ Short to GND Protection

When the LED+ is shorted to GND, the FB voltage is higher than V_{REF}, and the internal COMP voltage is driven low and clamped, and the high-side MOSFET is commanded on for a minimum on-time each cycle. The device enters fold-back mode, meanwhile, chip reaches internal current limit.

Efficiency and Feedback Voltage

The feedback voltage has a direct effect on the converter efficiency. Because the voltage drop across the feedback resistor does not contribute to the output power (LED brightness), the lower the feedback voltage, the higher the efficiency. Especially when powering only three or less LEDs, the feedback voltage impacts the efficiency around 2% depending on the sum of the forward voltage of the LEDs.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 140°C) the chip is enabled again.

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Applications Information

Setting the LED Current

The LED current is controlled by the feedback resistor, R_{S1}, in the following table. The current through the LEDs is given by the equation 100mV/R_{S1}. Following table shows the selection of resistors for a given LED current.

I_{LED} (A)	R_1 (Ω)
1	0.1
0.5	0.2
0.1	1

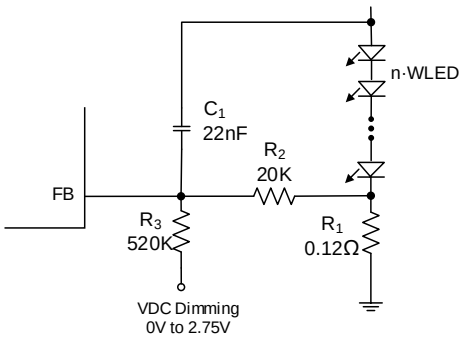
R_{S1}=0.1/I_{LED}

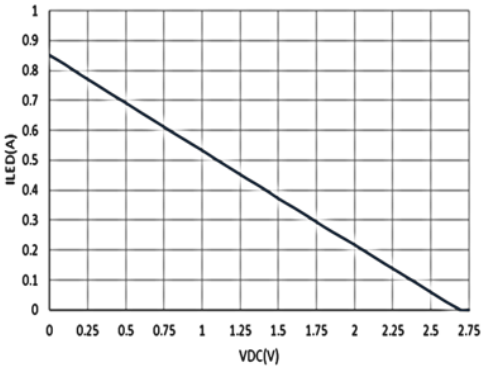
I_{LED} is average LED current.

Analog/PWM Dimming Control

1.Using a DC Voltage to FB Pin

When DIM pin remains high level, using a variable DC voltage to adjust the brightness is a popular method in some applications. According to the Superposition Theorem, as the DC voltage increases, the voltage contributed to VFB increases and the voltage drop on R2 increases, i.e. the LED current decreases. For example, if the VDC range is from 0V to 2.75V, the selection of resistors sets dimming control of LED current from 833mA to 0mA.





The LED current can be calculated by the following Equation:

$$I_{LED} = \frac{V_{FB} - \frac{R_2 \times (V_{DC} - V_{FB})}{R_3 + R_{DC}}}{R_1}$$

2.Using a PWM Signal to FB Pin

Another common application is using a filtered PWM signal as an adjustable DC voltage for LED dimming control. A filtered PWM signal acts as the DC voltage to regulate the output current. In this circuit, the output ripple depends on the frequency of PWM signal. For smaller output voltage ripple, the recommended frequency of 2.75V PWM signal should be above 10kHz. To fix the frequency of PWM signal and change the duty cycle of PWM signal can get different output current.

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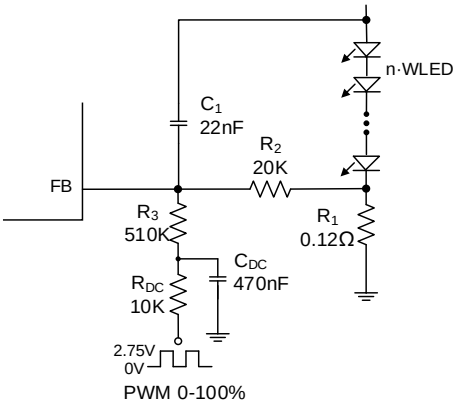

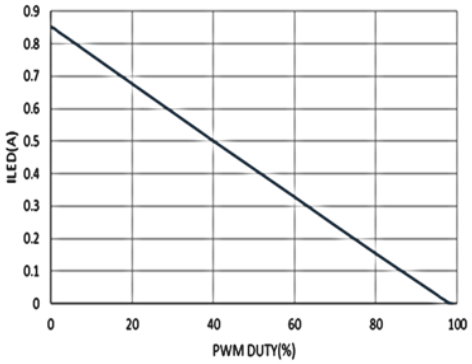

The LED current can be calculated by the following Equation:

$$I_{LED} = \frac{V_{FB} - \frac{R_2 \times (V_{PWM} \times Duty - V_{FB})}{R_3 + R_{DC}}}{R_1}$$

Inductor Selection

Select the appropriate inductance value according to different number of series lamp groups. For most applications, 4.7 to 10μH are recommended. Small size and better efficiency are the major concerns for portable device, such as RY7117 used for mobile phone. When selecting the inductor, the inductor saturation current should be rated as high as the peak inductor current at maximum load, and respectively, maximum LED current.

Output Capacitor Selection

The device is designed to operate with a wide selection of ceramic output capacitors. The selection of the output capacitor value is a trade-off between output voltage ripple and capacitor cost and form factor. In general, capacitor values of 10μF up to 22μF can be used. For better voltage filtering, ceramic capacitors with low ESR are recommended. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 10μF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering and EMI reduction, this value can be increased. The input capacitor should be placed as close as possible to the input pin of the converter.

Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. Input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with an enough width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

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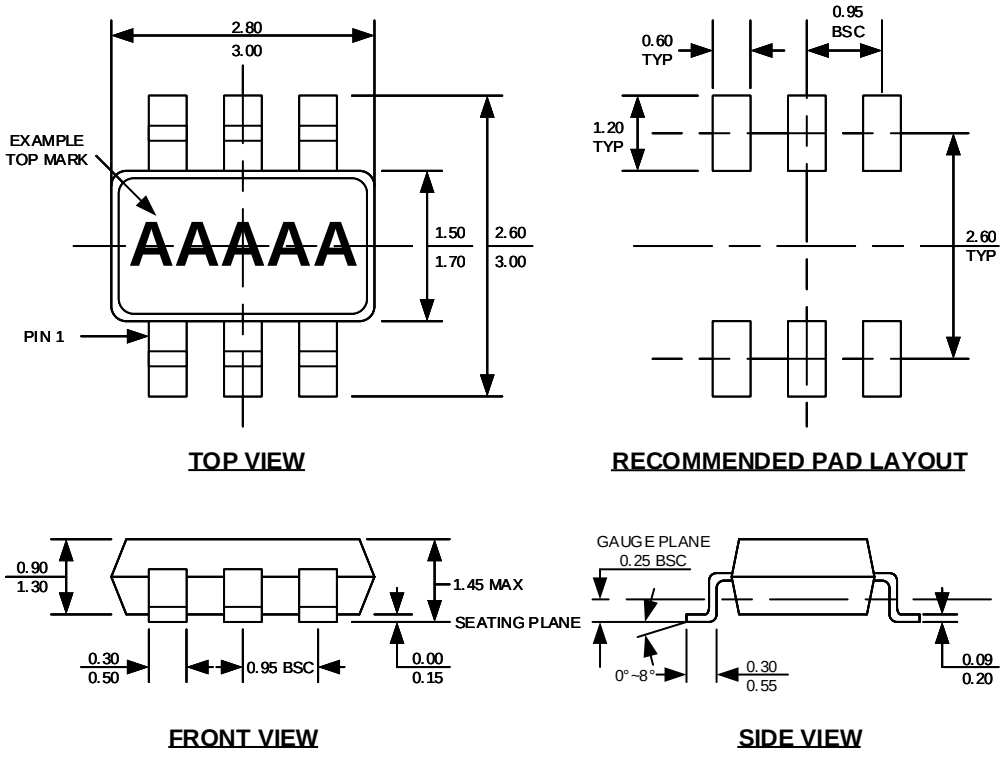
Package Description

SOT23-6



NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.