Switching regulator series

Step-down DC-DC converter PCB layout EMC Design guide

In switching power supply design, PCB layout design is as important as circuit design. Various power supply issues can be avoided by proper layout. The main issues that may be caused by improper layout are increased noise superimposed on the output and switching signals, poor regulation, and lack of stability. The proper layout reduces the occurrence of these issues.

Checkpoint summary

Table 1 shows a list of PCB checkpoints and explains the details of each item on the next page.

No.	Item	Importance	Checkpoint	✓
1	Input capacitor	Must	Strongly recommend minimizing the loop area of the current path as much as possible.	
			Place the input capacitor closest to the power supply pins and the power ground pin.	
		Case-by-case	Place the smallest capacitance capacitor as close to the device as possible. However, it depends on the specifications of the device and the cost of additional parts.	
2	Output capacitor	Must	Place the output capacitor near the inductor.	
3	Power ground	Must	Minimize the surface power ground area as much as possible.	
4	Other Ground	Must	Place the ground plane in a layer closest to the surface layer where the device is mounted.	
5	Number of PCB layers and inter-layer distance	Must	PCB with 4layer or more layers are strongly recommended.	
		Case-by-case	Do not expand the power supply plane more than necessary.	
6	π-type filter	Must	Place the π-type filter.	
			Do not delete the ground plane in the lower layer of the π-type filter.	
7	Surface ground plane and VIA	Must	Do not create isolated ground areas.	
			Space the vias according to the wavelength of the frequency that needs to be addressed.	
8	Crosstalk and I/O pin arrangement	Must	Avoid placement and wiring patterns of components that cause crosstalk.	
9	Common mode filter	Must	Delete the ground plane in the lower layer of the common mode filter.	

Table 1. List of PCB checkpoints

1. Input capacitor

In DC-DC converters, it is important to minimize the loop area of the current path through which AC current flows during switching operation. A larger loop area can increase the risk of EMI (unwanted electromagnetic radiation) with other circuits and systems. In addition, a larger loop area increases parasitic inductance, which reduces power conversion efficiency and increases switching noise. For details, refer to "1. Current Path" in the PCB layout of the pressure-reducing converter.

First, the input capacitor is placed as the most important part. It is desirable to place two types of ceramic capacitors, a large capacitor and a decoupling capacitor should be placed as close to the device as possible. Large-capacity capacitors with a value of a few µF are used to reduce ripple noise, and decoupling capacitors with a value of about 0.1 µF to 0.47 µF are used to reduce switching noise. These ceramic capacitors are effective when placed as close as possible to the power supply and power ground pins.

Figure 1 shows the impedance-frequency characteristics of the capacitor. Capacitors have two main parasitic components: ESL (Equivalent Series Inductance) and ESR (Equivalent Series Resistance). Therefore, the capacitor behaves capacitively up to its self-resonant point. However, at frequencies beyond the self-resonant point, it becomes inductive, causing the impedance to increase.

Figure 2 shows the impedance-frequency characteristics of individual capacitor models with different values, as well as the combined characteristics when they are connected in parallel. In the high-frequency range, around 100MHz, where each capacitor becomes inductive, there is little difference in impedance between the individual capacitors. By using two capacitors, the ESL value is halved, resulting in the parallel impedance being 6dB lower than with a single capacitor. This approach is effective in the frequency range above several tens of MHz.

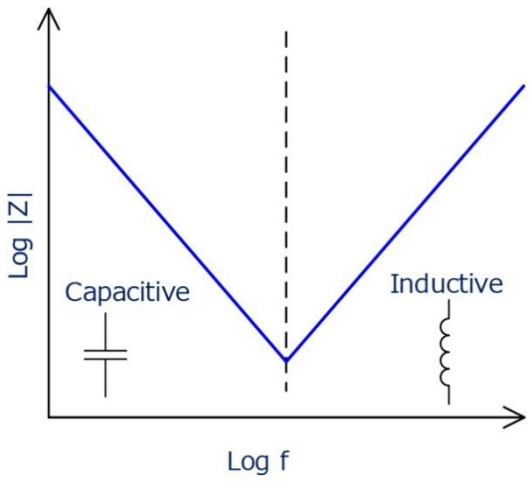

Figure 1. Capacitor frequency-impedance characteristics

Placing decoupling capacitors as close as possible to the device's power and ground pins maximizes noise reduction effectiveness in higher frequency ranges. This is because the inductance of the wiring increases as it gets farther from the device. This wiring inductance adds to the capacitor's ESL, which can shift the resonance frequency to a lower range.

Checkpoint

Must

- Strongly recommend minimizing the loop area of the current path as much as possible.
- Place the input capacitor closest to the power supply pins and the power ground pin.

Case-by-case

- Place the smallest capacitance capacitor as close to the device as possible. However, it depends on the specifications of the device and the cost of additional parts.

2. Output capacitor

While not as critical as the requirements for input capacitors, it is still advisable to place the output capacitor close to the inductor. The reason is to effectively suppress the output ripple current and minimize the voltage ripple. This improves circuit stability and enables efficient power supply. Additionally, shortening the distance between the capacitor and inductor reduces parasitic inductance and contributes to the suppression of high-frequency noise.

Checkpoint

Must

- Place the output capacitor near the inductor.

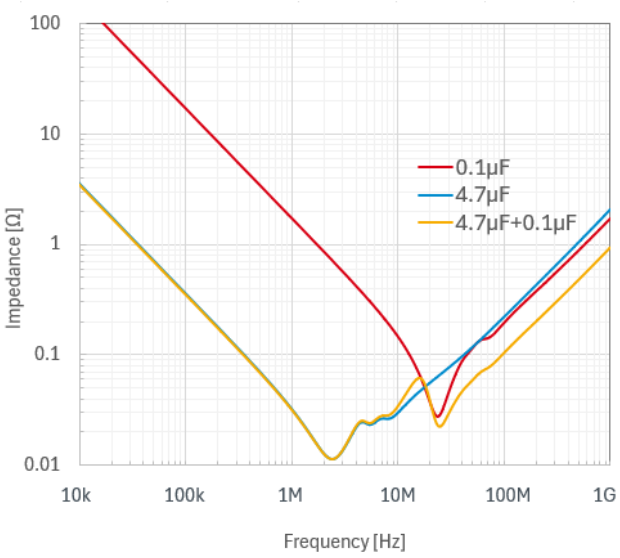

Figure 2. Ceramic capacitor frequency characteristics

3. Power ground

For a FET-integrated synchronous rectification type, the power ground corresponds to the device's power ground pin. For a diode rectification type, it refers to the anode of the Schottky diode and the ground of the input capacitor.

As shown in Figure 3, it is recommended to keep the power ground separate from other grounds in the surface layer. As shown in Figure 4, if the power ground is made common with other grounds, it may lead to increased noise from the power ground, resulting in higher conducted and radiated noise. Additionally, keep the area of the power ground on the surface layer as small as possible. This is to prevent spreading of unwanted noise components. Note that while the independent power ground in Figure 3 uses many vias to keep the impedance low, the number of vias should be kept to a level that does not obstruct the current path.

Checkpoint

Must

- Minimize the surface power ground area as much as possible.

4. Other ground

In DC-DC converters, to suppress the electric field generated by the switching current path, it is important to place a ground plane directly underneath the current path to contain the electric field. This arrangement helps minimize the impact of EMI. To achieve this, place the ground plane in a layer closest to the surface layer where the device is mounted. This means that the second layer should be a ground plane. For a controller-type IC, the layer closest to the ground plane should be the one containing the current loop, which includes the input capacitor, external FET, and external Schottky barrier diode.

Checkpoint

Must

- Place the ground plane in a layer closest to the surface layer where the device is mounted.

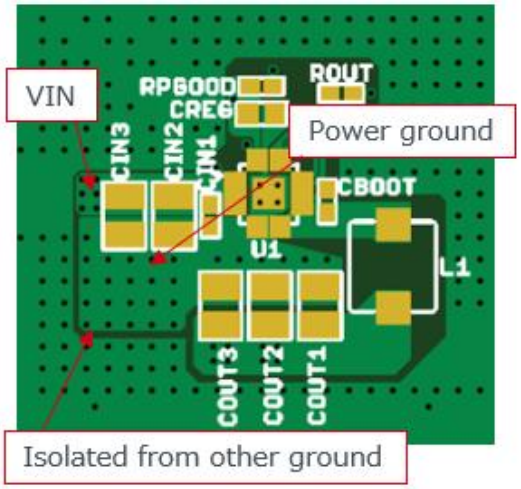

Figure 3. Board with power ground is isolated from other grounds on the top layer.

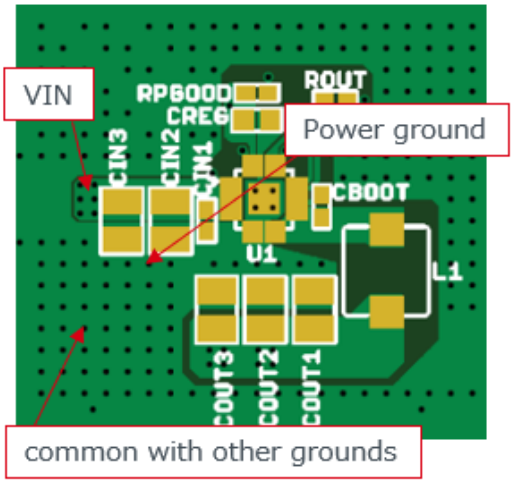

Figure 4. Board with power ground is made common with other grounds

5. Number of PCB layers and interlayer spacing

Number of PCB layers

A PCB with 4layer or more layers is strongly recommended. The advantage of using a multilayer PCB is that the power and ground planes are placed adjacent to each other. The physical arrangement of these two planes acts as additional decoupling capacitors, aside from the discrete components. The capacitors formed between these layers have very low ESL components, resulting in a high self-resonant frequency. This makes them effective for impedance reduction in the hundreds of MHz to several GHz frequency range. The capacitance value is determined by the parallel plate capacitor formula, where it is proportional to the board area and inversely proportional to the distance between the layers. A shorter distance between the power and ground planes results in greater capacitance, leading to more effective high-frequency noise reduction.

Power supply surface

The interlayer capacitance increases in proportion to the surface area of the power plane. However, if the power plane itself is too large, the pattern can act as an antenna, picking up noise from other areas and potentially worsening the noise performance. While the optimal size of the power plane cannot be quantified at this time, but it should be noted that making the power plane too large could lead to a deterioration in noise characteristics.

Checkpoint

Must

- PCB with 4layer or more layers are strongly recommended.

Case-by-case

- Do not expand the power supply plane more than necessary.

6. π-type filter

The π-type filter is a common countermeasure used in many electronic devices, and it is often considered an essential solution for power ICs and LED driver boards. Power fluctuations can appear as conducted or radiated noise through the input line. However, by implementing an LC filter on the input line, it helps to suppress the transmission of high-frequency components (ripple/noise) above the LC cutoff frequency into the input line. Additionally, using a π-type filter helps to reduce mutual interference of noise components entering the filter from both directions.

Selecting values for π-type filters

Select a relatively small inductance value such as 1μ to 10μH. Ceramic capacitors between 4.7 μF and 10 μF are used on the input side of the board end, while ceramic capacitors and bulk capacitors are used on the IC side. Ceramic capacitors are compatible with input capacitors of devices. For bulk capacitors, a low ESR electrolytic capacitor with a high capacitance should be suitable and the value should be chosen so that the output impedance of the π-type filter is smaller than the DC-DC input impedance (|ZDF|<|Zin|). For details, refer to the section "About the output impedance of the π filter" below.

The cutoff frequency in LC is determined by how many dB of attenuation is desired for the fundamental frequency (switching frequency) spectrum. First, measure the spectrum of the fundamental frequency using a spectrum analyzer without the π-type filter in place. Check how many dB the fundamental frequency exceeds the limit, and then determine the amount of attenuation needed by adding a margin to the excess value. For example, if the fundamental frequency is 400 kHz and the spectrum is at 60 dBμV, and it is required to reduce it by 40 dB, then the filter should be designed to achieve this level of attenuation. In this case, since an ideal LC filter attenuates at -40 dB/decade, the cutoff frequency should be set to 40 kHz or lower. As an example, when L=4.7 μH and C=4.7 μF are selected, the cutoff frequency of the LC is 34 kHz. However, in practice, the attenuation rate may decrease due to the ESR and ESL of the capacitors used. Therefore, it is recommended to verify the filter's passband characteristics through simulation.

About the Lower Ground Plane of the π-type Filter

To confine the magnetic field generated by current flowing through the inductor and minimize EMI effects, it is recommended not to remove the ground plane positioned below the π-type filter. However, when using a common mode filter, the processing of the lower ground plane is different. For details, refer to “About the Lower Ground Plane of the Common Mode Filter" below.

About the output impedance of the π-type filter

Although this is not related to noise characteristics, the impedance Zin of the IC side from the DC-DC input pin must satisfy the following relationship with the impedance Zf of the input line:

$$Z_{in} < Z_f$$

If this condition is not met, it can lead to oscillation of the device input, which may cause issues such as UVLO detection, over-voltage input, or malfunction of the power device. Especially, a low input voltage with a heavy load presents a strict condition. As an example, when an inductor for filtering is inserted into the input line as shown in Figure 5, the following equation must be satisfied:

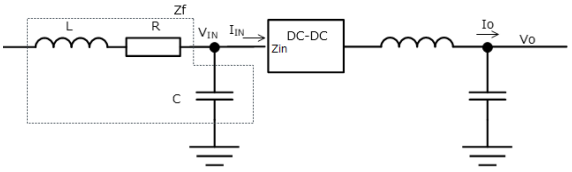

Figure 5 Input Filter and Output Impedance

$$Z_f = \frac{1}{\frac{1}{R + j\omega L} + j\omega C} = \frac{(R + j\omega L)(1 - \omega^2 CL - j\omega RC)}{(1 - \omega^2 CL)^2 + (\omega RC)^2}$$

Since Zf is maximized at the resonant frequency of the LC circuit, substituting $\omega = \frac{1}{\sqrt{LC}}$:

$$Z_f = \frac{\sqrt{L^2 + R^2 CL}}{RC} < |Z_{in}| = \frac{V_{IN}{}^2}{V_{OUT} \times I_{OUT}} \times \eta$$

As a countermeasure, reducing the value of L can be effective. However, to maintain the characteristics of the π-type filter, it is recommended to increase the capacitance on the device side.

As an example, in primary power supplies, bulk capacitors like electrolytic capacitors are often connected as backup power sources, so this issue is less common. However, in secondary power supplies, where only a small capacitor CIN might be connected, caution is needed.

Checkpoint

Must

- Place the π-type filter.
- Do not delete the ground plane in the lower layer of the π-type filter.

7. Surface ground plane and VIA

The ground pattern on the printed circuit board may generate noise if the VIA is not properly placement. Especially when layout and wiring constraints result in a narrow ground configuration, the ground itself can act as an antenna, potentially radiating or picking up noise. In such cases, it is important to properly place vias or cut unnecessary ground patterns.

About VIA Intervals

It is important not to create isolated ground areas on the top layer, as shown in Figure 6-a, where there is no connection to the lower layers through VIA. Ground VIAs should be placed at the endpoints. If there are isolated ground areas, VIAs should be placed as shown in Figure 6-b, or the areas that would become isolated ground should be cut. It is also recommended to place the VIAs at some intervals. Therefore, the VIA spacing should be less than one-twentieth of the expected highest frequency λ. For example, for 1 GHz, the wavelength reduction ratio is 46%. $\lambda = (3 \times 10^8 / 1 \times 10^9) \times 0.46 = 0.138\ m$ As the wavelength is 1/20 of the wavelength, $\lambda = 0.138/20 = 0.0069\ m = 6.9\ mm$ the values are as follows. In addition, cut the ground where the VIA cannot be placed.

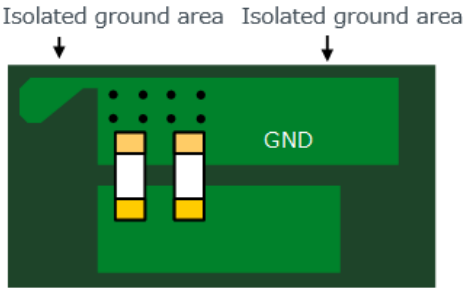

Figure 6-a. Example of isolated ground area

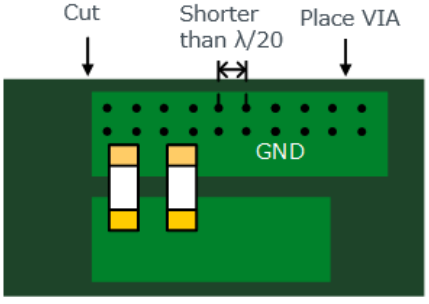

Figure 6-b. Examples of Measures in Isolated Ground Areas

Checkpoint

Must

- Do not create isolated ground areas.
- Space the vias according to the wavelength of the frequency that needs to be addressed.

8. Crosstalk and I/O pin arrangement

When arranging components and routing traces, it is important to ensure a proper PCB layout that prevents crosstalk.

Crosstalk

Crosstalk refers to the transmission of signals or noise between adjacent traces due to coupling, and is also known as signal leakage, interference, or crosstalk. Even though two wires (including thin PCB traces) are separated, electrical signals or noise should not transfer between them. However, when two wires run parallel, noise can be transmitted between them due to stray (parasitic) capacitance and mutual inductance.

Figure 7 shows good and bad wiring of the input filter section. In a good example, the noise-generating trace and the filtered trace are separated, reducing interference. However, in a bad example, these traces run parallel, causing coupling between them, which can reduce the effectiveness of the filter.

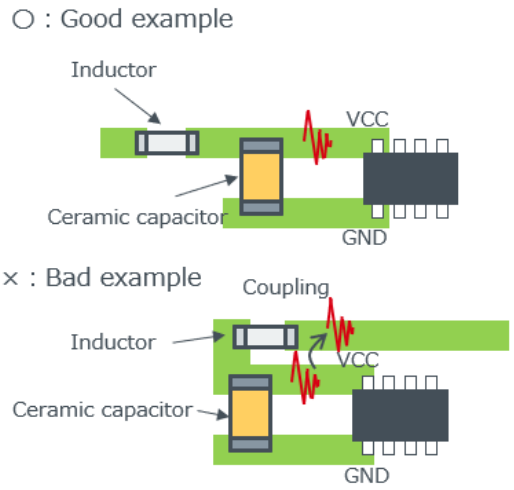

Figure 7. Example of cross talk due to filter placement

Figure 8 shows an example of the layout where crosstalk occurs. To make the PCB more compact, the layout between the input and output of the π-type filter has been folded back. In this layout, the switching inductor is placed next to the power (+B) line after the filter. As a result, the effectiveness of the filter is reduced, and significant radiated noise was observed across the entire frequency range.

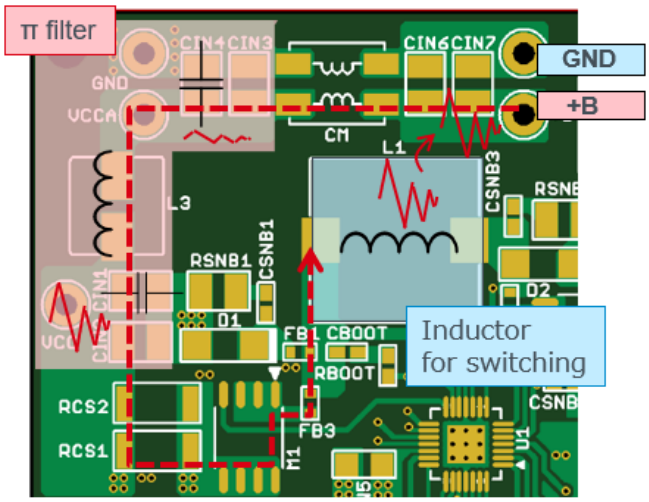

Figure 8. Example of crosstalk to the power supply (+B) line

Checkpoint

Must

- Avoid placement and wiring patterns of components that cause crosstalk.

9. Common mode filter

The use of common mode filters is optional. This filter is highly effective at reducing common-mode noise, but if the layout is not carefully managed, it may not achieve sufficient effectiveness due to the impact of differential-mode noise.

About the Lower Ground Plane of the Common Mode Filter

Figure 9 shows an example of common mode filter layout and the results. The example on the left shows the layout without a common-mode filter and the resulting conducted noise measurements, indicating that the noise level in the FM band is elevated. This is caused by common mode noise. The example in the center shows that simply placing a common-mode filter on the top layer for noise reduction is insufficient.

This is because it does not adequately address the noise that bypasses from the ground plane on the second layer to the connector side. To achieve the effectiveness of a common-mode filter, it is necessary to remove the ground pattern under the filter, as shown in the example on the right. It is recommended to remove the ground patterns from all layers: Top, Mid1, Mid2, and Bottom. However, as explained in the "π-type Filter" section, do not remove the lower-layer ground plane under the π-type filter.

The application notes "Precautions for PCB Layout Regarding Common Mode Filters" are also available for reference.

Checkpoint

Must

- Delete the ground plane in the lower layer of the common mode filter.

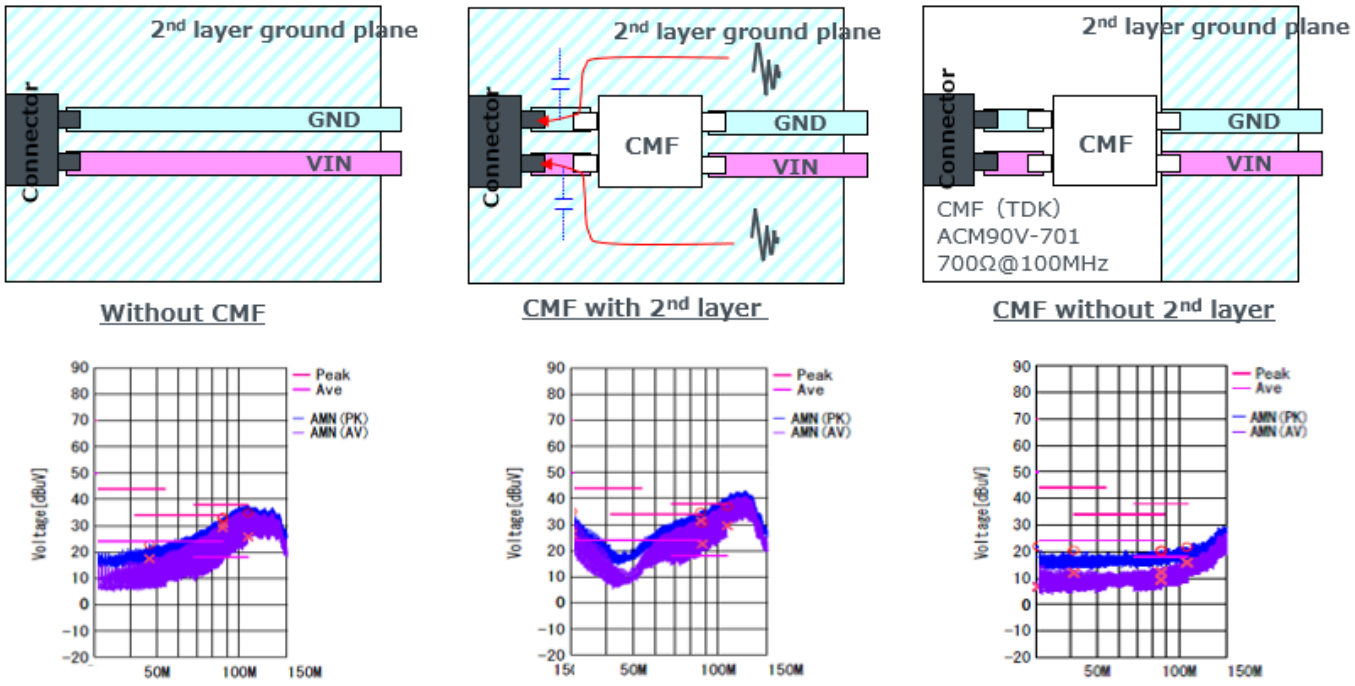

Figure 9. Effect of lower ground plane of common mode filter (measured by CISPR25 conduction noise voltage method)

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