Genesys Logic, Inc.

GL3231

USB 3.2 GEN1 Dual UHS-I Memory Card Reader Controller

Datasheet

Revision 1.03
Jul. 07, 2020

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Genesys Logic, Inc.
13F., No. 205, Sec. 3, Beixin Rd., Xindian Dist. 231,
New Taipei City, Taiwan
Tel : (886-2) 8913-1888
Fax : (886-2) 6629-6168
http ://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	07/19/2018	Formal release
1.01	01/11/2019	Update CH2 Features
1.02	04/20/2020	1. Update Table 5.2 - Operating Conditions 2. Update Table 5.3 - DC Characteristics 3. Update Table 8.1 - Ordering Information
1.03	07/07/2020	Update Table 6.1 – SPI NOR Flash Support List

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CHAPTER 1 GENERAL DESCRIPTION

GL3231 is an USB 3.1 GEN1 to dual SD 3.0 LUN Memory Card Reader Controller.

GL3231 supports various types of SD memory cards, such as Secure Digital™ (SD), SDHC, miniSD and microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro and MMCmobile. It also supports high density memory cards (Capacity up to 2TB), such as SDXC, ultra high speed memory cards and SD3.0 UHS-I. GL3231 also supports SANDISK EXTREME® 160 MB/s microSD UHS-I CARD.

The GL3231 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port. It integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce system BOM cost. It also integrates 5V to 1.2V DC-DC as alternative to improve the power efficiency.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.1 Specification (USB 3.1 GEN1)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 3 endpoints: Control (0) / Bulk Data Read In (1) / Bulk Data Write Out (2)
  - Support 5 Gbps/SuperSpeed, 480 Mbps/high-speed, and 12 Mbps/full-speed transfer rates
- Integrated USB building blocks
  - SuperSpeed USB/USB 2.0 transceiver macro (UTM), Serial Interface Engine (SIE), and embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficiency hardware DMA engine improves data transfer performance between USB and flash card interfaces
- Support Secure Digital™ v1.0 / v1.1 / v2.0/ SDHC / SDXC (capacity up to 2TB)
- Support Secure Digital™ v3.0 UHS-I (Ultra High Speed): SDR12/SDR25/SDR50/DDR50/SDR104
- Support DDR200 speed mode to enhance the UHS-I performance
- Support SANDISK EXTREME® 160 MB/s microSD UHS-I CARD
- Support MultiMediaCard™ (MMC)
  - MMC specification v3.x / v4.0 / v4.1 / v4.2 / v4.3 / v4.4
  - x1 / x4 bit data bus
- Support HUAWEI Nano Memory Card
- Support ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port
- On-Chip power MOSFETs for supplying flash media card power
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- On-chip 5V to 1.2V DC-DC to improve power efficiency.
- Support Over-Current protection mechanism
- Support USB 2.0 LPM (Link Power Management)
- Support USB 3.1 GEN1 LTM (Latency Tolerance Messaging)
- Support USB 3.1 GEN1 U1/U2/U3 low power link state
- Support Latency Tolerance Messaging
- Support remote wakeup function
- Support Intel Power Optimizer
- Support Windows Connected Standby
- Support Spread Spectrum Clock for SD to reduce EMI effect
- Available in QFN52 pin package (6x6mm)

CHAPTER 3 PIN ASSIGNMENT

3.1 QFN 52 Pinout

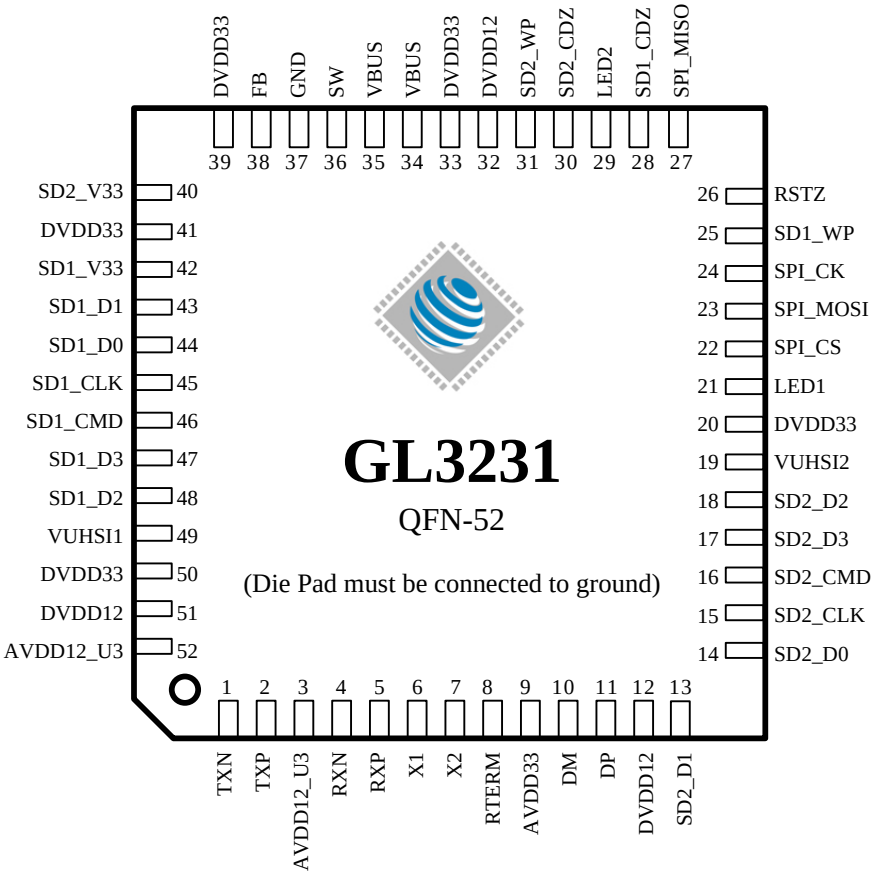


Figure 3.1 - QFN 52 Pinout Diagram

3.2 Pin Description

Table 3.1 - Pin Description

Pin Name	QFN 52 Pin	Type	Description
Power/Ground			
AVDD12_U3	3, 52	P	Analog 1.2V power source to SD
AVDD33	9	P	Analog 3.3V power source
DVDD12	12,32,51	P	Digital 1.2V power source
DVDD33	20,33,39,41,50	P	Digital 3.3V power source
VBUS	34, 35	P	5V power source
FB	38	P	Feedback pin, connected to 1.2V output
SW	36	P	Switch out of 5V to 1.2V DC-DC
VUHSI1	49	P	UHS-I IO PAD Power, the power source of this pin comes from the internal regulator of GL3231 and no need of external power input
VUHSI2	19	P	UHS-I IO PAD Power, the power source of this pin comes from the internal regulator of GL3231 and no need of external power input
SD1_V33	42	P	Card power switch 400mA for SD card power
SD2_V33	40	P	Card power switch 400mA for SD card power
GND	37	P	Ground
USB PHY Interface			
DP	11	A	USB 2.0 D+
DM	10	A	USB 2.0 D-
TXN	1	A	USB 3.1 GEN1 TX-
TXP	2	A	USB 3.1 GEN1 TX+
RXN	4	A	USB 3.1 GEN1 RX-
RXP	5	A	USB 3.1 GEN1 RX+
RTERM	8	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be populated between RTERM and GND
X1	6	I	25MHz XTAL input. It can be connected to external 25MHz clock input
X2	7	B	25MHz XTAL output
Memory Card Interface			
SD1_D0	44	B	SD1_DATA0
SD1_D1	43	B	SD1_DATA1
SD1_D2	48	B	SD1_DATA2
SD1_D3	47	B	SD1_DATA3
SD2_D0	14	B	SD2_DATA0
SD2_D1	13	B	SD2_DATA1
SD2_D2	18	B	SD2_DATA2
SD2_D3	17	B	SD2_DATA3

SD1_CDZ	28	I, pu	SD1 card detect 0: Card insert 1: No card Internal pull-up to DVDD33(3.3V)
SD2_CDZ	30	I, pu	SD2 card detect 0: Card insert 1: No card Internal pull-up to DVDD33(3.3V)
SD1_CLK	45	O	SD1 clock
SD2_CLK	15	O	SD2 clock
SD1_CMD	46	B	SD1 command/response
SD2_CMD	16	B	SD2 command/response
SD1_WP	25	I, pu	SD1 write protect 0: write enable 1: write protection Internal pull-up to DVDD33(3.3V)
SD2_WP	31	I, pu	SD2 write protect 0: write enable 1: write protection Internal pull-up to DVDD33(3.3V)
Others			
LED1	21	O	Card Access LED
LED2	29	O	Card Access LED
SPI_CS	22	O	SPI interface: chip select
SPI_CK	24	O	SPI interface: clock
SPI_MOSI	23	O	SPI interface: connect to SPI flash data input
SPI_MISO	27	I	SPI interface: connect to SPI flash data output
RSTZ	26	I, pu	Chip reset, active low Internal pull-up to DVDD33(3.3V)

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

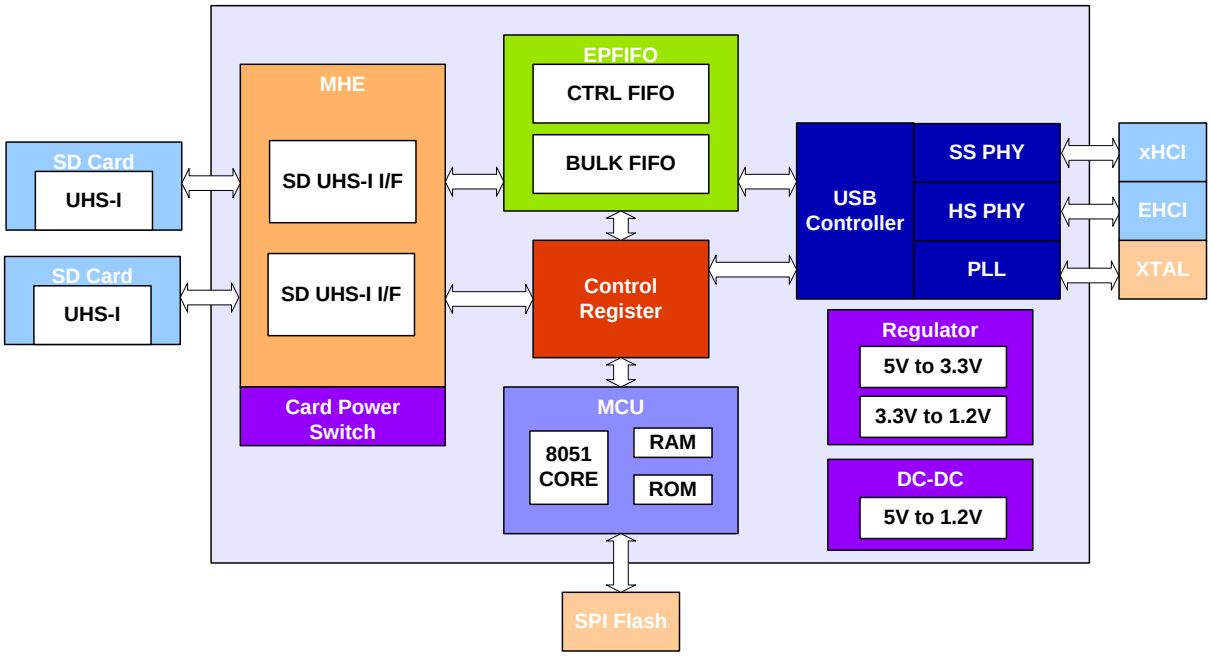


Figure 4.1 - Functional Block Diagram

4.1 Super Speed and HS PHY

The transceiver macro is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0) and Bulk In/Out FIFO

- **CTRL FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.1 GEN1 continuously.
  2. It can be directly accessed by micro-controller

4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **RAM** Internal RAM area for MCU access

4.5 MHE (Media Hardware Engine)

Media Interface: SD/MMC

4.6 Regulator

- **5V to 3.3V** 3.3V Power Source
- **3.3V to 1.2V** 1.2V Power Source

4.7 DC-DC

- **5V to 1.2V** 1.2V Power Source to analog

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Temperature Conditions

Table 5.1 - Temperature Conditions

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to +70 °C

5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	25 MHz ± 30ppm

5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{12}	Output Voltage	DC-DC mode	1.13	1.24	1.36	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.4	V
I_I	Input Leakage Current	$0 < V_{IN} <$ DVDD	-10		10	μA
V_{OH}	Output High Voltage	DVDD = 3.3V	2.8			V
V_{OL}	Output Low Voltage				0.4	V
I_{OH}	Output Current High			8		mA
I_{OL}	Output Current Low			8		mA
C_{IN}	Input Pin Capacitance			5		pF
*I_{NORMAL}	HS mode			35		mA
	SS mode	U0 state		46		mA
		U1 state		14		mA
		U2 state		9.8		mA
*I_{ACTIVE}	HS mode			46		mA
	SS mode	U0 state		55		mA

I_{RESET}				42		mA
I_{SUS}	HS Suspend current	1.5K pull-up included		0.80		mA
	SS Suspend current	U3 State		0.63		mA
R_{pu}	Reset Pad pull-up			46		KΩ
	SD_CDZ, SD_WP, GPIO Pad pull-up			46		KΩ
	SD_CMD pull-up			15		KΩ
	SD_CLK, D[3:0] Pad pull-up			15		KΩ
R_{pd}	SD_CMD pull-down			15		KΩ
	SD_CLK, D[3:0] Pad pull-down			15		KΩ
R_{IMP}	SD_CMD, SD_CLK, D[3:0] impedances			50		Ω

* $I_{NORMAL:}$ The memory card is inserted but not in read/write

* $I_{ACTIVE:}$ The memory card is in read/write

5.4 AC Characteristics of Reset Timing

5.4.1 Reset Timing

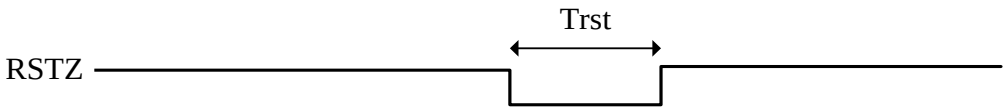


Figure 5.1 - Timing Diagram of Reset Width

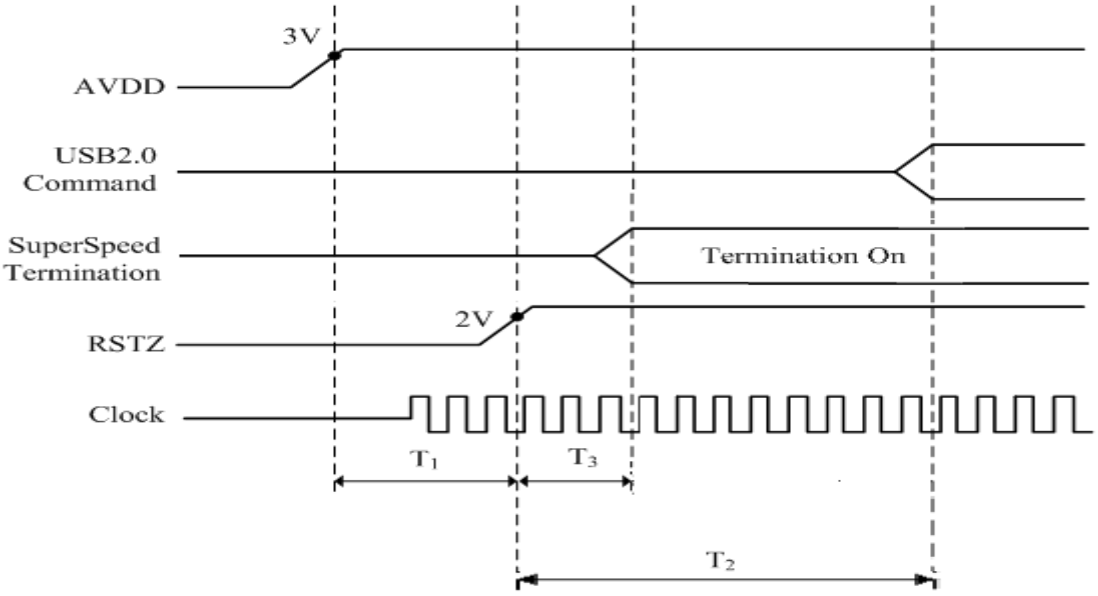


Figure 5.2 - Timing Diagram of Power-on to USB Bus Ready

Table 5.4 - Reset Timing

Parameter	Description	Min.	Max.	Unit
Trst	Chip reset sense timing width	2		us
T_1	AVDD power up to reset de-assert	500		us
T_2	Reset de-assert to respond USB2.0 command ready		100	ms
T3	Reset de-assert to SuperSpeed termination on		35	ms

5.4.2 SD Card Clock Frequency

Table 5.5 - SD Card Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	187	KHz
F_{DS}	Clock frequency Default Speed Mode	25	MHz
F_{HS}	SD Clock frequency High Speed Mode	50	MHz
F_{HS}	MMC Clock frequency High Speed Mode	52	MHz
F_{SDR25}	Clock frequency UHS-I Mode: SDR25	50	MHz
F_{DDR50}	Clock frequency UHS-I Mode: DDR50	50	MHz
F_{SDR50}	Clock frequency UHS-I Mode: SDR50	100	MHz
F_{SDR104}	Clock frequency UHS-I Mode: SDR104	208	MHz
F_{DDR200}	Clock frequency Ultra High Speed Mode: DDR200	200	MHz

CHAPTER 6 SPI NOR FLASH SUPPORT LIST

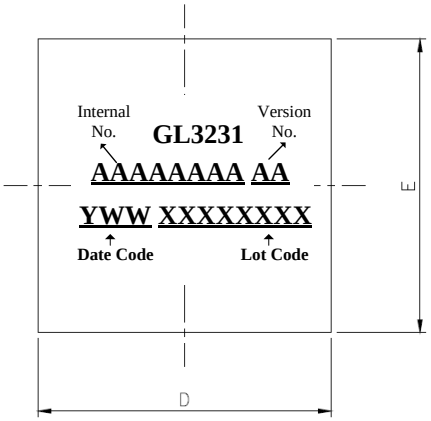
Table 6.1 - SPI NOR Flash Support List

Vendor	Model
GigaDevice	GD25D10B, GD25Q20, GD25Q40, GD25Q21B, GD25Q20C
PMC	PM25LD010, PM25LD020, PM25LD010C, PM25LD020C, PM25LQ020
WINBOND	W25X10CL, W25X20CL, W25X10BV, W25X20BV, W25Q40BL
MXIC	MX25L1006E, MX25L4006E, MX25L1021E, MX25L2006E, MX25V1006F
ESMT	F25L01PA(86P), F25L01PA(100P)
FMSH	FM25F01, FM25F005, FM25F04A
EON	EN25F10, EN25LF10, EN25F40
PEA	T25S40A
Boya	BY25Q10A, BY25Q20A
XTX	FT25H04, FT25LX04
Puya	P25Q21H

Note :

- GL3231 supports Page-Program SPI Flash only, not for Byte-program SPI Flash
- Firmware file (xxxx.bin) which provided by Genesys Logic is only used for Genesys Logic's Multi-Tool and MP Tool ISP (In System Programming via USB interface) purpose. If you would like to provide FW for SPI Flash vendor mass production or Flash ROM writer, please contact GL technical support team.

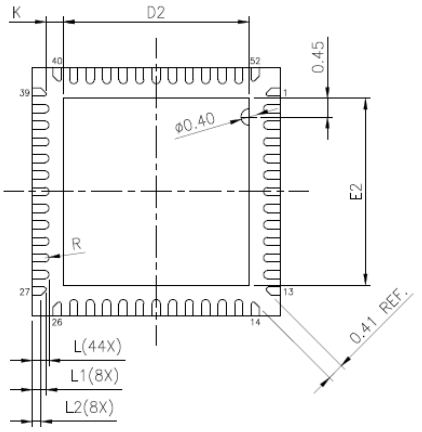
CHAPTER 7 PACKAGE DIMENSION



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	UQFN(W652)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.150 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	—	0.23
K	0.20	—	—
R	0.075	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE	VQFN	WQFN	UQFN
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF				
185X18* MIL	4.45	4.50	4.55	4.45	4.50	4.55	V	X	N/A	———	———	V
1 185X18* MIL	4.45	4.50	4.55	4.45	4.50	4.55	V	X	N/A	V	V	—

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.



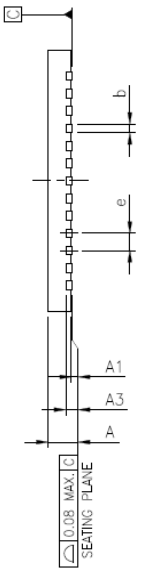


Figure 7.1 - QFN 52 Pin Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL3231-OOYXX	QFN 52	Green Package + CU Wire	XX	MP