RTL8723DU-CG

802.11b/g/n 1T1R WLAN and Bluetooth 2.1/4.2 Single-Chip Controller with USB 2.0 Multi-Function Interface

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.8	2016/03/30	Preliminary release.

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1. General Description

The Realtek RTL8723DU is a highly integrated single-chip 802.11b/g/n 1T1R WLAN, and an integrated Bluetooth 2.1/4.2 single chip with USB 2.0 multi-function. It combines a WLAN MAC, a 1T1R capable WLAN baseband, BT Protocol Stack (LM, LL, and LE), BT Baseband, modem, and WLAN/BT RF in a single chip. The RTL8723DU provides a complete solution for a high-performance integrated wireless LAN and Bluetooth controller. The RTL8723DU WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the 802.11n specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for 802.11g and 802.11n OFDM respectively.

A built-in enhanced signal detector, adaptive frequency domain equalizer, and a soft-decision Viterbi decoder help to alleviate multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8723DU WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain better performance in the analog portions of the transceiver.

The RTL8723DU WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensate for the extra

power required to transmit OFDM. The RTL8723DS-VC provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

The RTL8723DU Bluetooth controller complies with Bluetooth core specification v4.2, and supports dual mode (BR/EDR + Low Energy Controllers). It is backward compatible with previous versions including v2.1 + EDR. For BR/EDR, it can support scatternet topology up to four active links in slave mode, and active links in master mode. For Low Energy, it supports multiple states and allows active links in master mode. Both BR/EDR and LE can operate simultaneously.

RTL8723DU also integrates RF/PA/LNA/Balun/DPDT for both 802.11n and Bluetooth to reduce the number of external components.

2. Features

General

- 48-pin QFN
- 802.11b/g/n 1T1R WLAN and Bluetooth single chip

Host Interface

- Complies with USB2.0 for WLAN and BT controller
- USB Multi-Function for both BT (USB function 0) and WLAN (USB function 1)
- USB LPM and USB Selective Suspend supported

WLAN Controller

- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Integrated Balun and DPDT
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Backward compatible with 802.11b/g devices while operating in 802.11n mode
- I 802.11b/g/n compatible WLAN
- 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WAPI supported

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Multi MACID support with Fast Channel switch
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications
- Supports Wake-On-WLAN via Magic Packets and Wake-up frame
- Support S3/S4 AES/TKIP group key update
- Support Win8 Network List Offload
- Support TCP/UDP/IP checksum offload
-

WLAN PHY Features

- 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Support 2.4GHz band channels
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCKmodulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g; and 150Mbps in 802.11n
- Switch diversity for DSSS/CCK
- Packet based hardware antenna diversity
- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Bluetooth Controller

- Compatible with Bluetooth v2.1, v4.2Systems
- Supports Bluetooth 4.0 Low Energy(BLE)
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports piconets in a scatternet
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff/Sniff Sub-rating)
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

Peripheral Interfaces

- General Purpose Input/Output (14 pins)
- Three configurable LED pins

- Flexible XTAL frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support XTAL or external clock input

3. Application Diagram

3.1. Single-Band 11n (1x1) Solution with Integrated Bluetooth Controller with Antenna Diversity

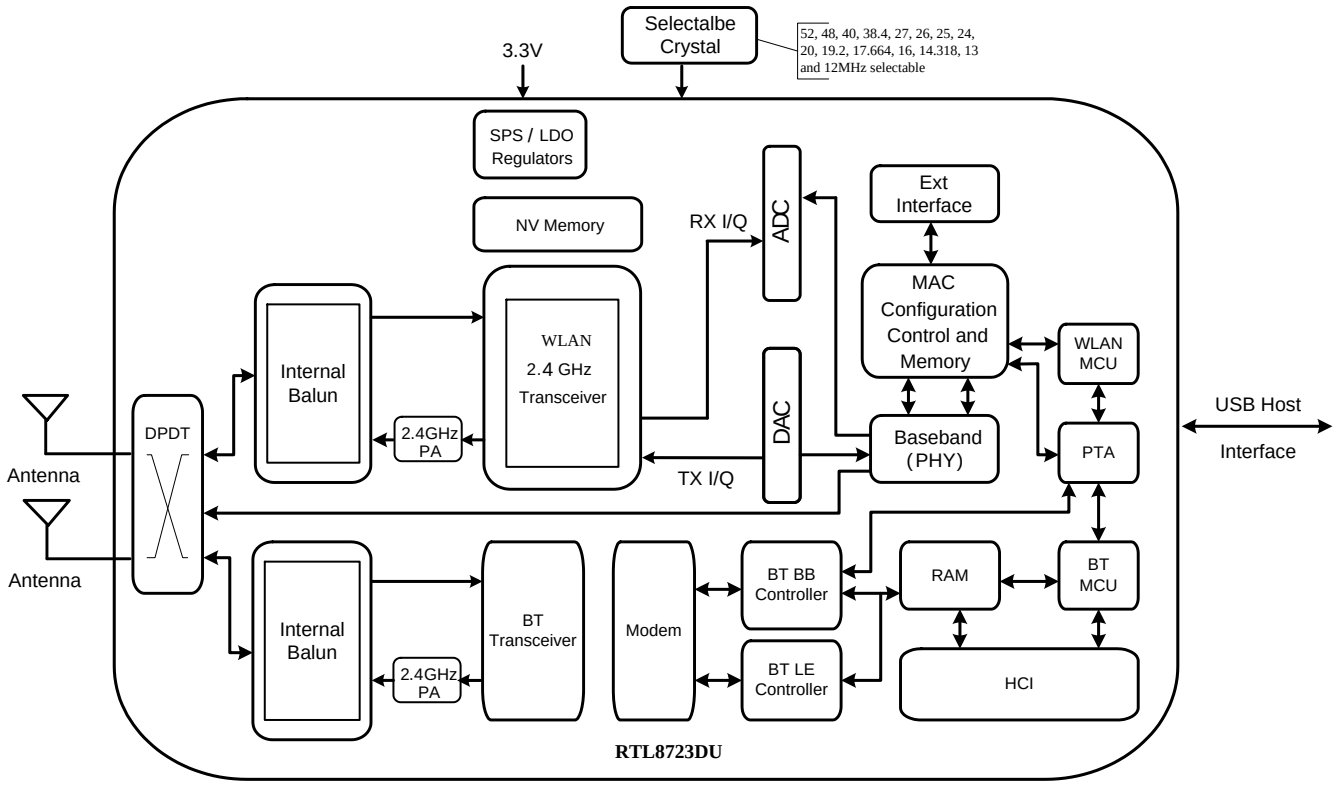


Figure 1. Single-Band 11n (1x1) and Integrated Bluetooth Controller Solution with Antenna Diversity

3.2. Single-Band 11n (1x1) Solution with Integrated Bluetooth Controller with Single Antenna

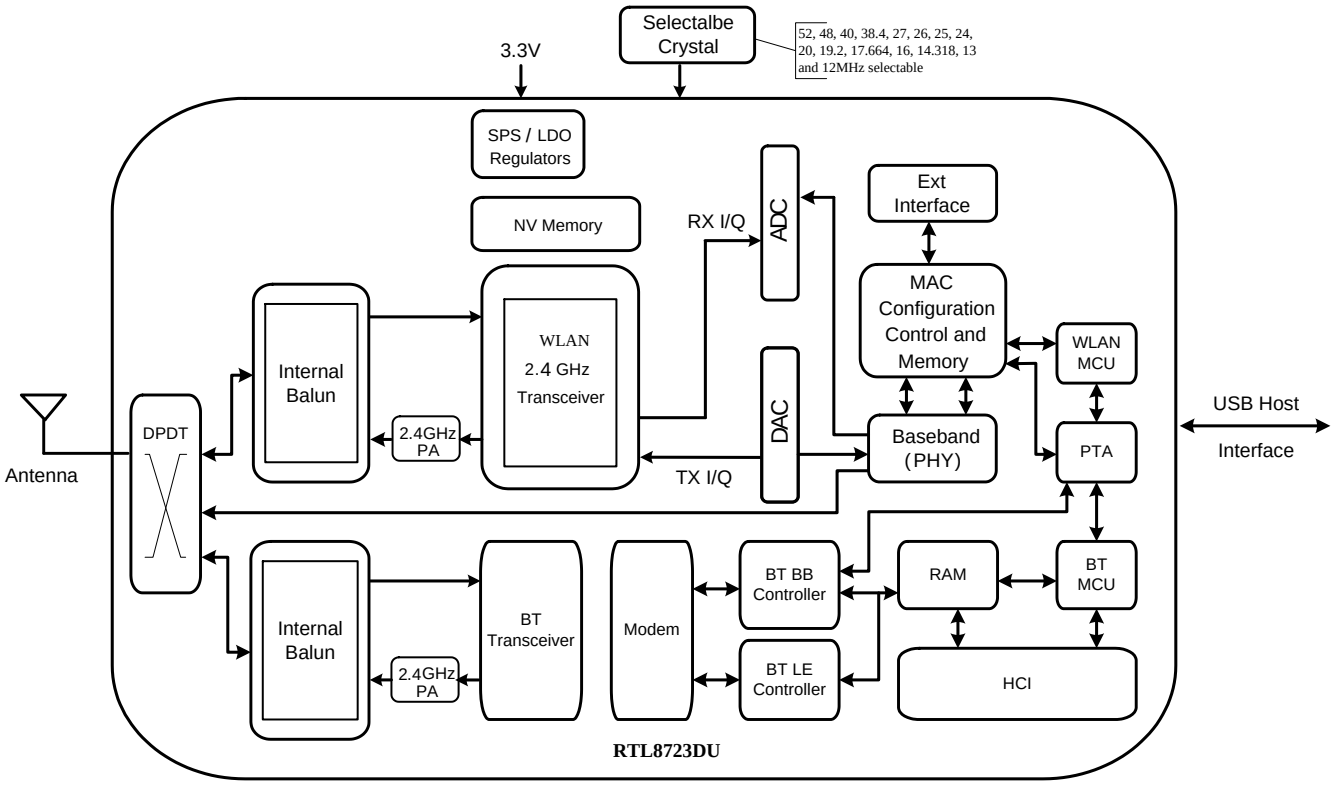


Figure 2. Single-Band 11n (1x1) and Integrated Bluetooth Controller Solution with Single Antenna

4. Pin Assignments

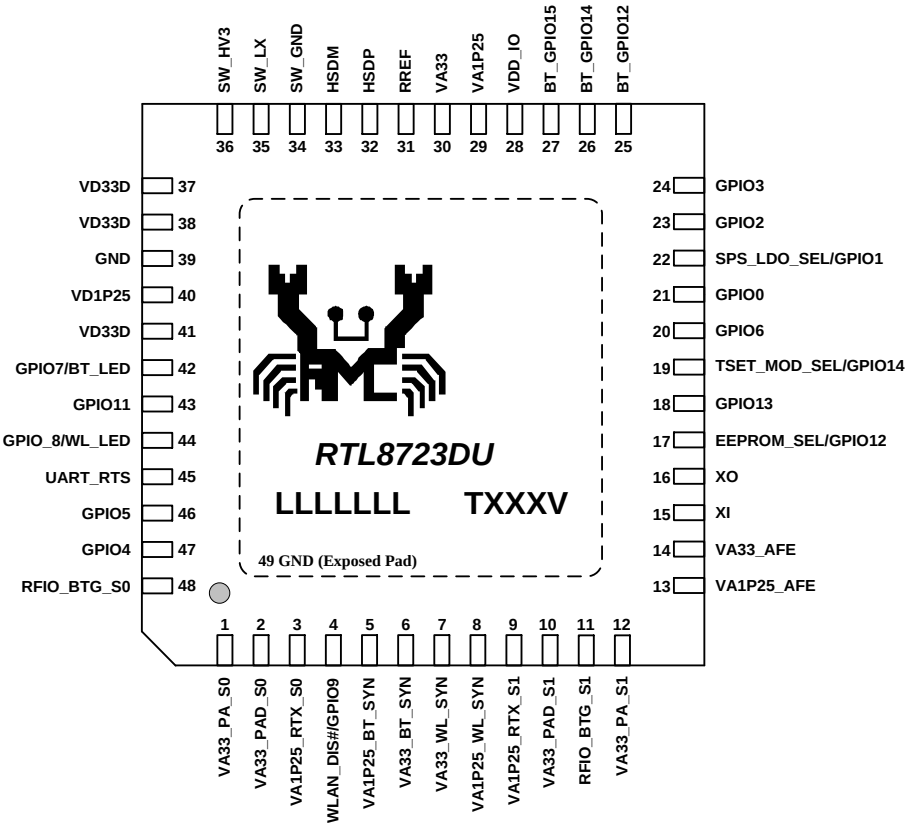


Figure 3. Pin Assignments

4.1. Package Identification

"Green" package is indicated by a 'G' in the location marked "T" in Figure 3.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input

O: Output

T/S: Tri-State bi-directional input/output pin

S/T/S: Sustained Tri-State

O/D: Open Drain

P: Power pin

5.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	19	Shared with GPIO14 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	22	Shared with GPIO1 0: Internal switching regulator select 1: Internal LDO select
EEPROM_SEL	I	17	Shared with GPIO12 0: Internal NV memory select 1: External EEPROM select

5.2. USB Transceiver Interface

Table 2. USB Transceiver Interface

Symbol	Type	Pin No	Description
HSDP	IO	32	High-Speed USB D+ Signal
HSDM	IO	33	High-Speed USB D- Signal

5.3. BT 3D Display Interface

Table 3. BT 3D Display Interface

Symbol	Type	Pin No	Description
3DD_SYNC_A	I	20	Shared with GPIO6 BT 3D Display synchronization control port A.

5.4. RF Interface

Table 4. RF Interface

Symbol	Type	Pin No	Description
RFIO_S0	IO	48	WLAN/BT RF TX/RX signal port 0
RFIO_S1	IO	11	WLAN/BT RF TX/RX signal port 1

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
BT_LED	O	42	LED Pin (Active Low)
WL_LED	O	44	LED Pin (Active Low)

5.6. Power Management Handshake Interface

Table 6. Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DIS#	I	4	Shared with GPIO9 This Pin Can Externally Shutdown the RTL8723DU-VC WLAN function when WL_DISn is Pulled Low. When this pin deasserted, USB interface will be disabled. This pin can also support the WLAN Radio-off function with host interface remaining connected.
BT_DIS#	I	43	Shared with GPIO11. This Pin Can Externally Shutdown the RTL8723DU-VC BT function when BT_DISn is Pulled Low. This pin can also support the BT Radio-off function with host interface remaining connected.
HOST_WAKE_CHIP	I	18	Shared with GPIO13. Host wakeup chip pin
CHIP_WAKE_HOST	O	19	Shared with GPIO14. Chip wakeup host pin

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	15	40MHz OSC Input 40MHz crystal reference clock input
XO	O	16	40MHz Crystal reference clock output
SUS_CLK	I	22	Shared with GPIO1. External 32K or RTC clock input.

Symbol	Type	Pin No	Description
GPIO0	IO	21	General Purpose Input/Output Pin
GPIO1	IO	22	General Purpose Input/Output Pin
GPIO2	IO	23	General Purpose Input/Output Pin
GPIO3	IO	24	General Purpose Input/Output Pin
GPIO4	IO	47	General Purpose Input/Output Pin
GPIO5	IO	46	General Purpose Input/Output Pin
GPIO6	IO	20	General Purpose Input/Output Pin
GPIO7	IO	42	General Purpose Input/Output Pin
GPIO8	IO	44	General Purpose Input/Output Pin
GPIO9	IO	4	General Purpose Input/Output Pin
GPIO11	IO	43	General Purpose Input/Output Pin
GPIO12	IO	17	General Purpose Input/Output Pin
GPIO13	IO	18	General Purpose Input/Output Pin
GPIO14	IO	19	General Purpose Input/Output Pin

5.8. Power Pins

Table 8. Power Pins

Symbol	Type	Pin No	Description
SW_LX	P	35	Switching Regulator Output
SW_HV3	P	36	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VA33	P	30	3.3V for Interface Analog Circuit
VA33_PA_S0 VA33_PAD_S0 VA33_PA_S1 VA33_PAD_S1 VA33_BT_SYN VA33_WL_SYN VA33_AFE	P	1 2 12 10 6 7 14	3.3V for RF Analog Circuit
VD33D	P	37,38,41	VDD3.3V
VDDIO	P	28	VDD for WAKE#, CLKREQ#, PERST#, GPIO0 to GPIO3 and GPIO9 to GPIO12 (3.3V)
VD1P25	P	40	VDD 1.25V Digital Circuit
VA1P25	P	29	1.25V for analog blocks
VA1P25_RTX_S0 VA1P25_RTX_S1 VA1P25_BT_SYN VA1P25_WL_SYN VA1P25_AFE	P	3 9 5 8 13	1.25V for BT and WLAN RF analog circuit
SW_GND	P	34	Switching Regulator Ground
RREF	P	31	Precision Resistor for Bandgap

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 9. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 10. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VA33 VA33_PAD_S0 VA33_PA_S0 VA33_PAD_S1 VA33_PA_S1 VA33_BT_SYN VA33_WL_SYN VA33_AFE VD33D	3.3V Supply Voltage	3.0	3.3	3.6	V
VA1P25 VA1P25_RTX_S0 VA1P25_BT_SYN VA1P25_WL_SYN VA1P25_RTX_S1 VA1P25_AFE	1.25V Core Supply Voltage	1.15	1.25	1.37	V
IDD33	3.3V Rating Current	-	-	600	mA

6.2.2. Digital IO Pin DC Characteristics

Table 11. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 12. 2.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	2.5	--	3.1	V
V_{OL}	Output low voltage	0	--	0.28	V

Table 13. 1.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

7. Interface Timing Specification

7.1. USB Bus during Power On Sequence

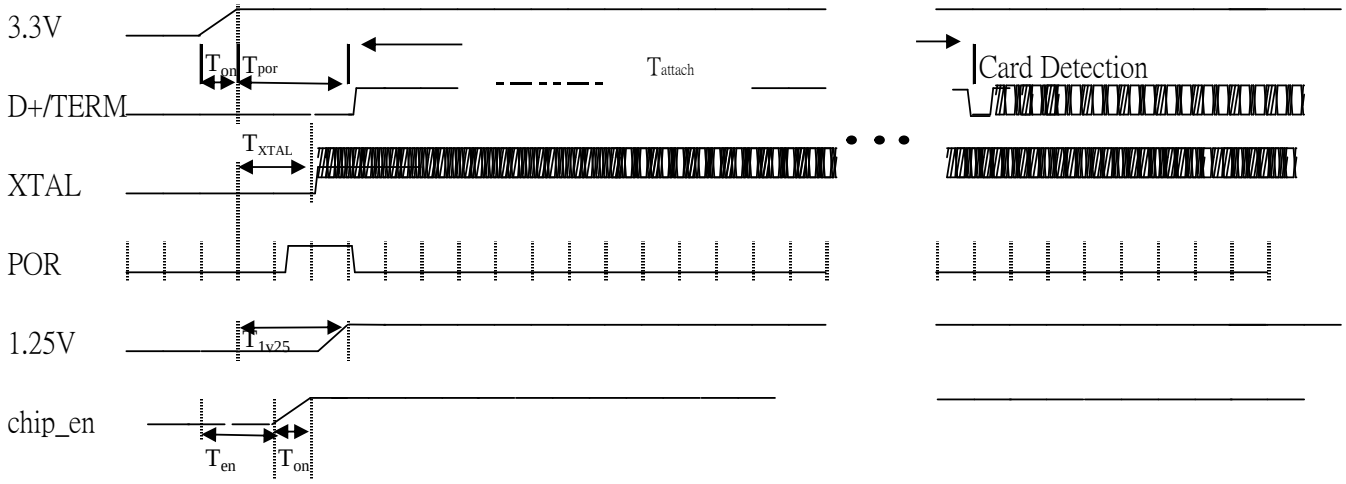


Figure 4. RTL8723DU USB Bus Power On Sequence

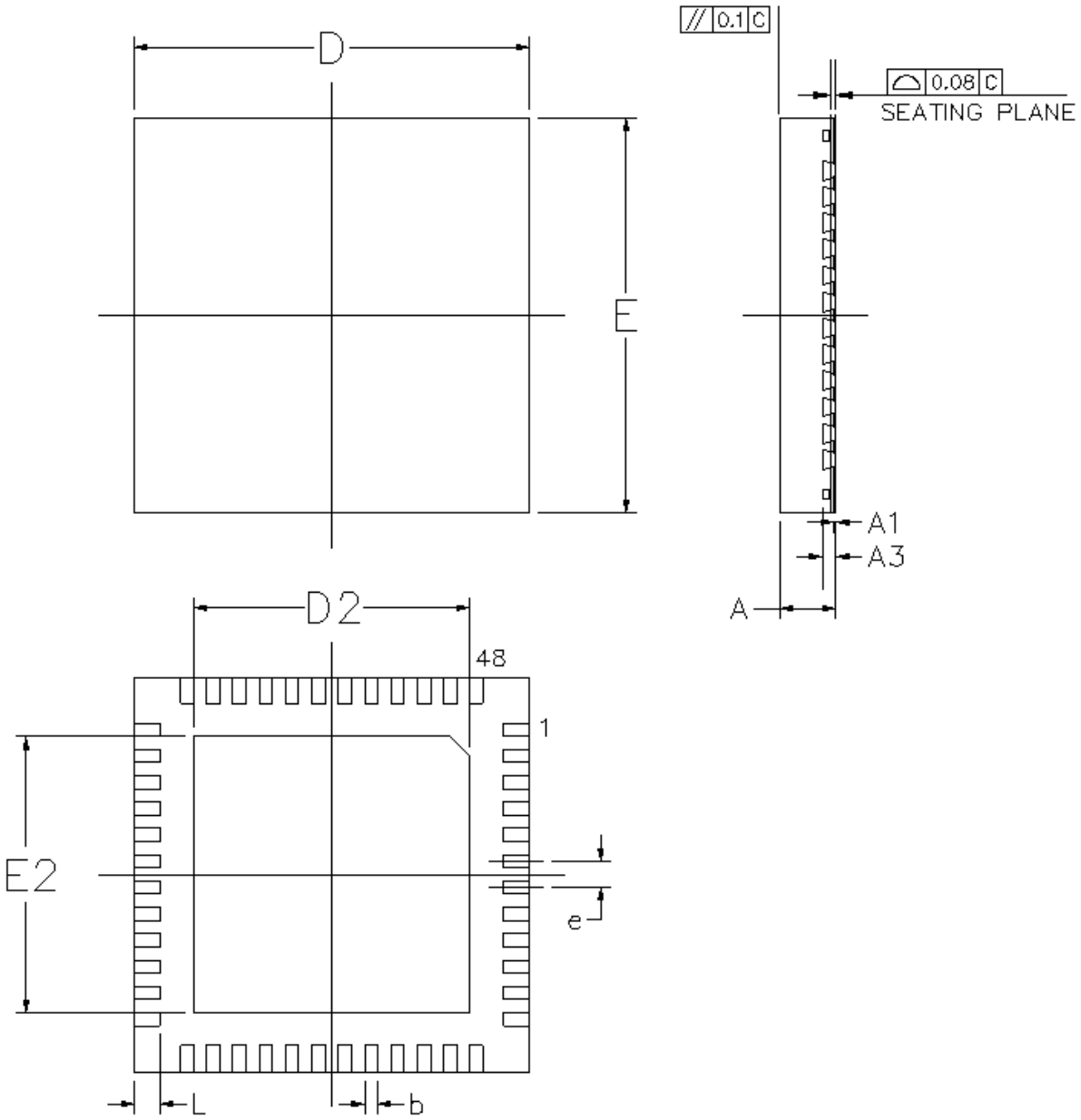
T_{on}: The main power ramp up duration
T_{por}: The power on reset releases and power management unit executes power on tasks
T_{attach}: USB attach state
$T_{k\text{-}state}$: the duration from resister attached to USB host starting card detection procedure

The power on flow description:
After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.
The power management unit also enables the USB circuits.
USB analog circuits attach resisters to indicate the insertion of the USB device

Table 14. The typical timing range

	Unit	Min	Typical	Max
T_{on}	ms	0.2	1.5	5
T_{por}	ms	--	2	10
T_{xtal}	ms	--	1.5	8
T_{attach}	ms	100	250	--
T_{1v25}	ms	-	2	5
T_{en}	ms	0	0	5

Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note1: CONTROLLING DIMENSION：MILLIMETER(mm)
Note2: REFERENCE DOCUMENTL：JEDEC MO-220

9. Ordering Information

Table 15. Ordering Information

Part Number	Package	Status
RTL8723DU-CG	QFN-48, 'Green' Package	Mass Production

Note: See page 8 for package identification.

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