NB25Q32A

Ultra Low Power, 32M-bit
Serial Multi I/O Flash Memory Datasheet

Performance Highlight

- Wide supply range from 2.65V to 3.6V for Read, Erase and Program
- Ultra-Low Power consumption for Read, Erase and Program
- x1, x2 and x4 Multi I/O Support
- High reliability with 100K cycling endurance and 20-year data retention

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1. FEATURES

- **SPI Flash Memories**
  - Standard SPI: SCLK, CS#, SI, SO
  - Dual SPI: SCLK, CS#, IO0, IO1
  - Quad SPI： SCLK, CS#, IO0, IO1, IO2, IO3

- **Highest Performance Serial Flash**
  - 1 I/O 133MHz for fast read
  - 2 I/O Dual I/O Data transfer up to 266Mbits/s
  - 4 I/O Quad I/O Data transfer up to 532Mbits/s

- **Power Supply and Low Power Consumption**
  - Single 2.65V to 3.6V supply
  - 8μA standby current,3μA deep power down current
  - 3.0mA active read current at 50MHz, 9mA active program or erase current

- **Flexible Architecture for Code and Data Storage**
  - Uniform 32/64K-byte Block Erase,Program 1 to 256 byte per programmable page
  - Minimum 100,000 Program/Erase Cycles, More than 20-year data retention
  - Latch-up protected to 100mA from -1V to Vcc +1V

- **Fast Program and Erase Speed**
  - 0.33ms page program time
  - 25ms 4K-byte sector erase time,0.25s 64K-byte block erase time

- **Advanced Security Features**
  - Additional 4K bits secured OTP
  - Features unique identifier
  - Discoverable parameters (SFDP) register

- **Package Information**
  - SOP8(150MIL/208MIL),TSSOP-8(173MIL)
  - Contact ZETTA for KGD and other options

2. OVERVIEW

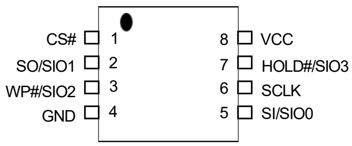
The NB25Q32A (32M-Bit) serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI : Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#).

The Dual I/O & Dual output data is transferred with speed of 266Mbits/s and the Quad I/O & Quad output data is transferred with speed of 532Mbits/s.

Specifically designed for use in many different systems, the device supports read, program, and erase operations with a wide supply voltage range of 2.65V to 3.6V. No separate voltage is required for programming and erasing.

2-1.Pin Definition

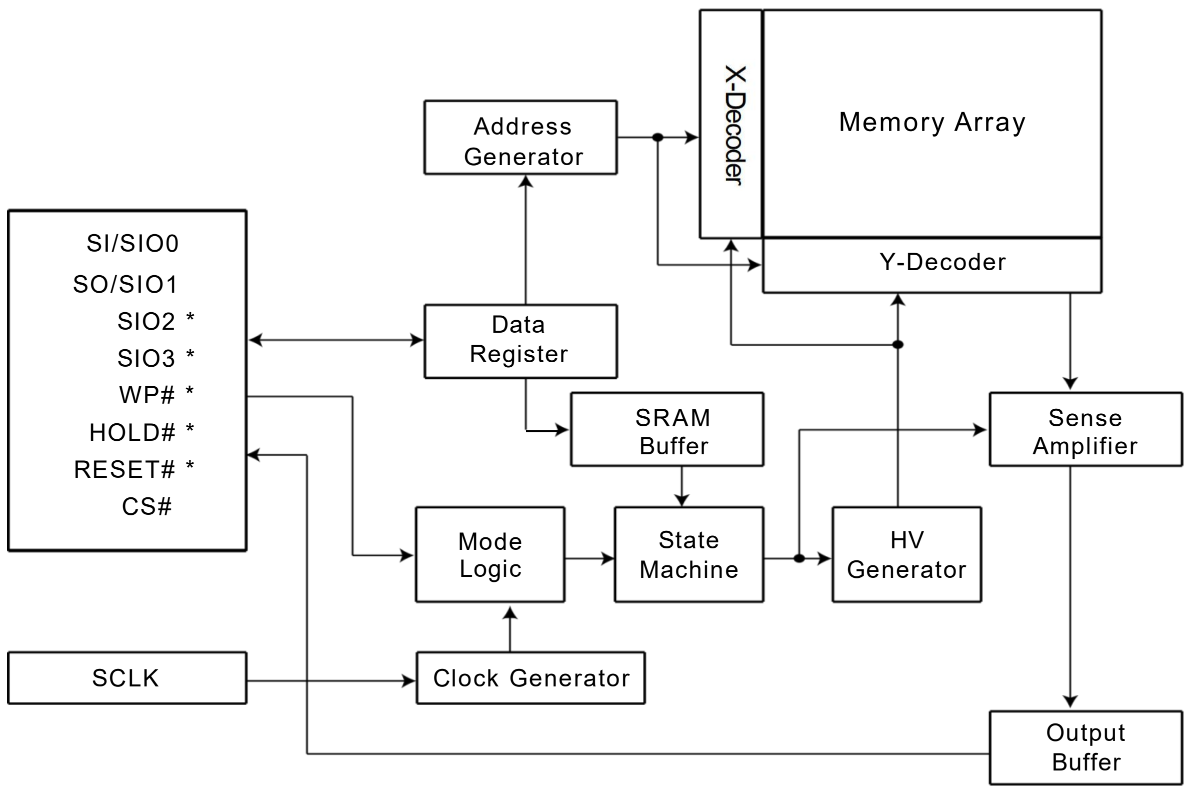
8-PIN SOP (150mil)/8-PIN SOP (200mil)



SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O mode and 4xI/ O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection Active Low or Serial Data Input & Output (for 4xI/O mode)
HOLD#/ SIO3	To pause the device without deselecting the device or Serial data Input/Output for 4 x I/O mode
VCC	+ 3.0V Power Supply
GND	Ground

Note:
The pin of HOLD#/SIO3 or WP#/SIO2 will remain
internal pull up function while this pin is not physically connected in system configuration.
However, the internal pull up function will be disabled if the system has physical connection to HOLD#/SIO3 or WP#/SIO2 pin.

2-2. BLOCK DIAGRAM



* Depends on part number options.

3. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

I. Block lock protection

- The Software Protected Mode (SPM) uses (TB, BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of *"Table 1. Protected Area Sizes"*, the protected areas are more flexible which may protect various areas by setting value of TB, BP0-BP3 bits.

- The Hardware Protected Mode (HPM) uses WP#/SIO2 to protect the (BP3, BP2, BP1, BP0, TB) bits and SRWD bit.

Table 1. Protected Area Sizes

Protected Area Sizes (TB bit = 0)

Status bit				Protect Level
BP3	**BP2**	**BP1**	**BP0**	**32Mb**
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 63rd)
0	0	1	0	2 (2blocks, block 62nd-63rd)
0	0	1	1	3 (4blocks, block 60th-63rd)
0	1	0	0	4 (8blocks, block 56th-63rd)
0	1	0	1	5 (16blocks, block 48th-63rd)
0	1	1	0	6 (32blocks, block 32nd-63rd)
0	1	1	1	7 (64blocks, protect all)
1	0	0	0	8 (64blocks, protect all)
1	0	0	1	9 (64blocks, protect all)
1	0	1	0	10 (64blocks, protect all)
1	0	1	1	11 (64blocks, protect all)
1	1	0	0	12 (64blocks, protect all)
1	1	0	1	13 (64blocks, protect all)
1	1	1	0	14 (64blocks, protect all)
1	1	1	1	15 (64blocks, protect all)

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	**BP2**	**BP1**	**BP0**	**32Mb**
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, block 0th-3rd)
0	1	0	0	4 (8blocks, block 0th-7th)
0	1	0	1	5 (16blocks, block 0th-15th)
0	1	1	0	6 (32blocks, block 0th-31st)
0	1	1	1	7 (64blocks, protect all)
1	0	0	0	8 (64blocks, protect all)
1	0	0	1	9 (64blocks, protect all)
1	0	1	0	10 (64blocks, protect all)
1	0	1	1	11 (64blocks, protect all)
1	1	0	0	12 (64blocks, protect all)
1	1	0	1	13 (64blocks, protect all)
1	1	1	0	14 (64blocks, protect all)
1	1	1	1	15 (64blocks, protect all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 7. Security Register Definition"* for security register bit definition and *"Table 2. 4K-bit Secured OTP Definition"* for address range definition.

Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 2. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx1FF	4096-bit	Determined by Factory	Determined by customer

4. MEMORY ORGANIZATION

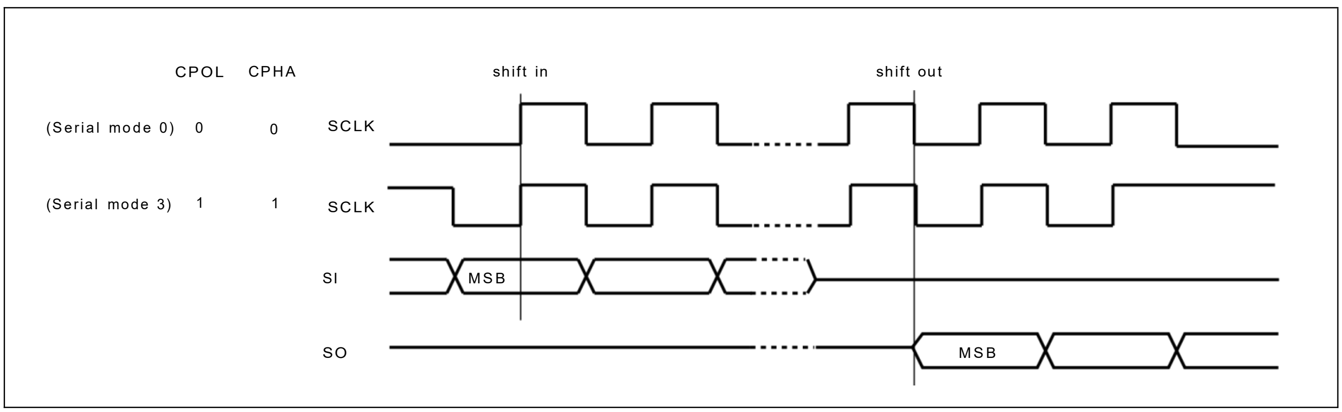
Table 3. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
63	127	1023	3FF000h	3FFFFFh
		⋮		
		1016	3F8000h	3F8FFFh
	126	1015	3F7000h	3F7FFFh
		⋮		
		1008	3F0000h	3F0FFFh
62	125	1007	3EF000h	3EFFFFh
		⋮		
		1000	3E8000h	3E8FFFh
	124	999	3E7000h	3E7FFFh
		⋮		
		992	3E0000h	3E0FFFh
61	123	991	3DF000h	3DFFFFh
		⋮		
		984	3D8000h	3D8FFFh
	122	983	3D7000h	3D7FFFh
		⋮		
		976	3D0000h	3D0FFFh
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

5. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.
4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock(SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported (for Normal Serial mode)"*.
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 4READ, QREAD, 2READ, DREAD, RDCR, RES, and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, CE, PP, 4PP, Suspend, Resume, NOP, RSTEN, RST, ENSO, EXSO, WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. While a Write Status Register, Program, or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



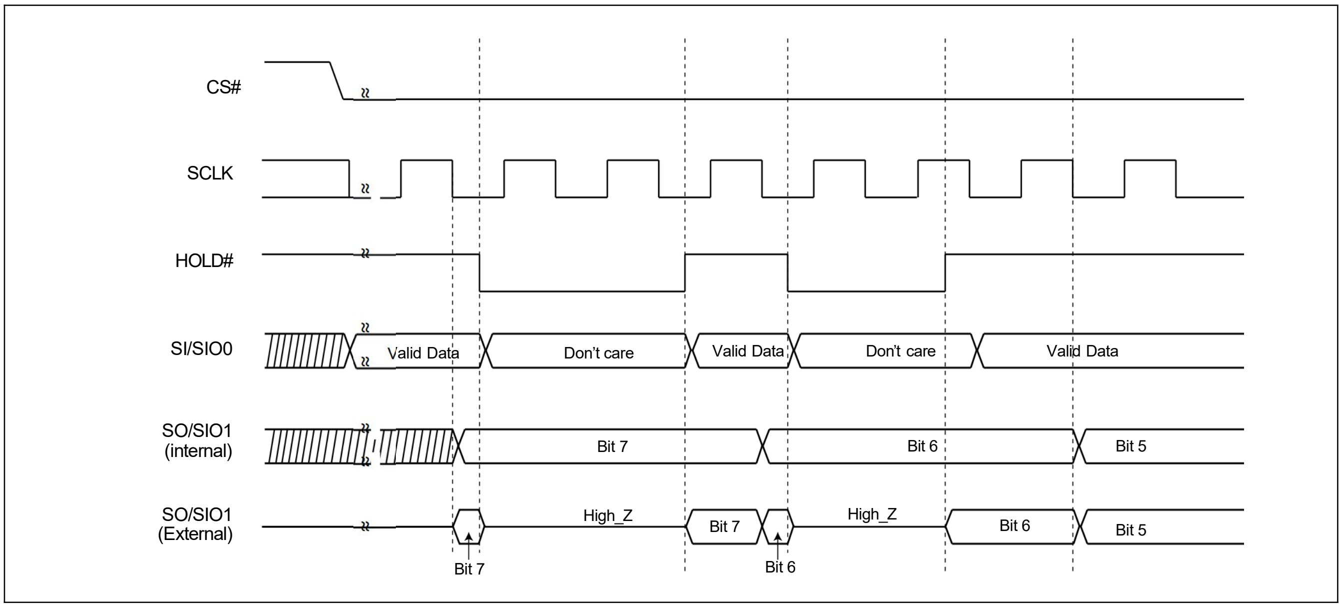
Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

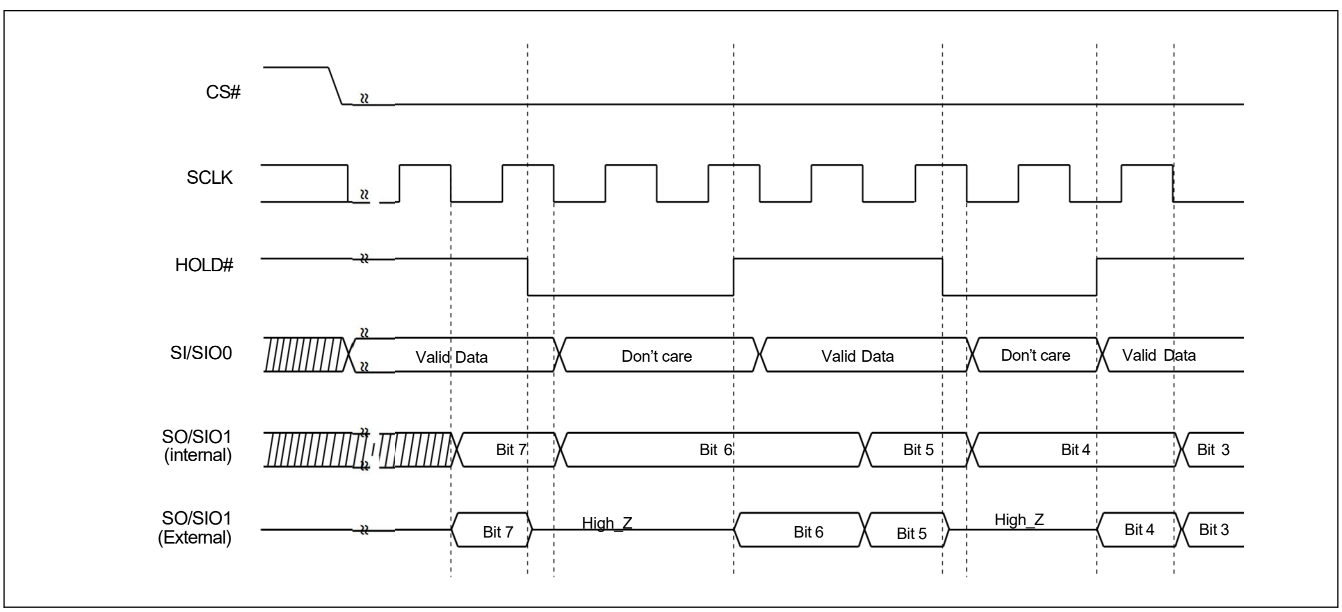
6. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 2. Hold Condition Operation





During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

7. COMMAND DESCRIPTION

Table 4. Command Sets

Read Commands

I/O	1	1	2	2	4	4
Command	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	4READ (4 x I/O read command)	QREAD (1I/4O read command)
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	ADD1(8)	ADD1(8)	ADD1(4)	ADD1(8)	ADD1(2)	ADD1(8)
3rd byte	ADD2(8)	ADD2(8)	ADD2(4)	ADD2(8)	ADD2(2)	ADD2(8)
4th byte	ADD3(8)	ADD3(8)	ADD3(4)	ADD3(8)	ADD3(2)	ADD3(8)
5th byte		Dummy(8)	Dummy*	Dummy(8)	Dummy*	Dummy(8)
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual Output until CS# goes high	Quad I/O read with configurable dummy cycles	

Note: *Dummy cycle number will be different, depending on the bit6 (DC) setting of Configuration Register. Please refer to *"Configuration Register"* Table.

Other Commands

Command	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	4PP (quad page program)	SE (sector erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	38 (hex)	20 (hex)
2nd byte					Values	ADD1	ADD1
3rd byte					Values	ADD2	ADD2
4th byte						ADD3	ADD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the configuration/ status register	quad input to program the selected page	to erase the selected sector

Command	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)	PP (page program)	DP (Deep power down)	RDP (Release from deep power down)	PGM/ERS Suspend (Suspends Program/ Erase)
1st byte	52 (hex)	D8 (hex)	60 or C7 (hex)	02 (hex)	B9 (hex)	AB (hex)	75/B0 (hex)
2nd byte	ADD1	ADD1		ADD1			
3rd byte	ADD2	ADD2		ADD2			
4th byte	ADD3	ADD3		ADD3			
Action	to erase the selected 32KB block	to erase the selected 64KB block	to erase whole chip	to program the selected page	enters deep power down mode	release from deep power down mode	program/erase operation is interrupted by suspend command

Command	PGM/ERS Resume (Resumes Program/ Erase)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO (enter secured OTP)
1st byte	7A/30 (hex)	9F (hex)	AB (hex)	90 (hex)	B1 (hex)
2nd byte			x	x	
3rd byte			x	x	
4th byte			x	ADD	
Action	to continue performing the suspended program/erase sequence	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 4K-bit secured OTP mode

Command (byte)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	RSTEN (Reset Enable)	RST (Reset Memory)	RDSFDP	SBL (Set Burst Length)
1st byte	C1 (hex)	2B (hex)	2F (hex)	66 (hex)	99 (hex)	5A (hex)	C0/77 (hex)
2nd byte						ADD1(8)	
3rd byte						ADD2(8)	Value
4th byte						ADD3(8)	
5th byte						Dummy(8)	
Action	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)			n bytes read out until CS# goes high	to set Burst length

Command (byte)	NOP (No Operation)
1st byte	00 (hex)
2nd byte	
3rd byte	
4th byte	
5th byte	
Action	

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 2: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

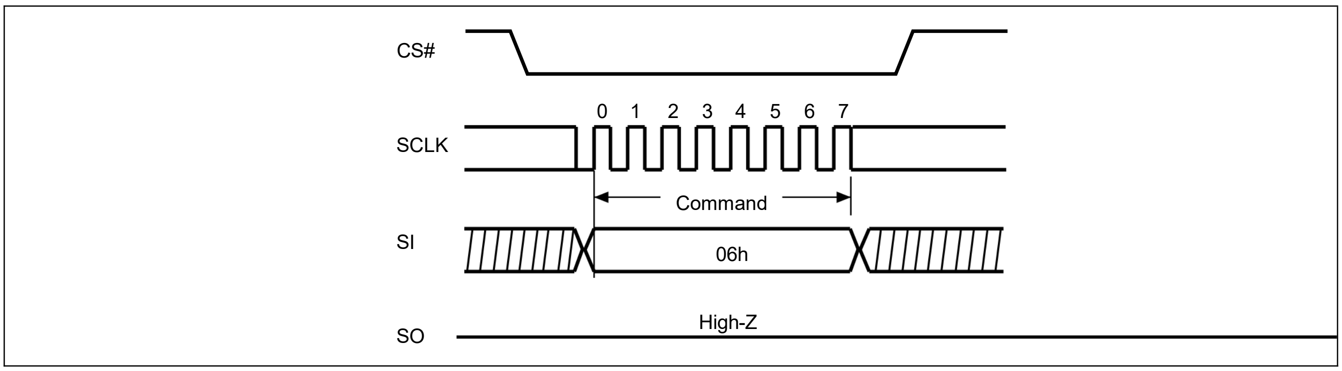
7-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE, BE32K, CE, and WRSR which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

The SIO[3:1] are don't care.

Figure 3. Write Enable (WREN) Sequence (Command 06)



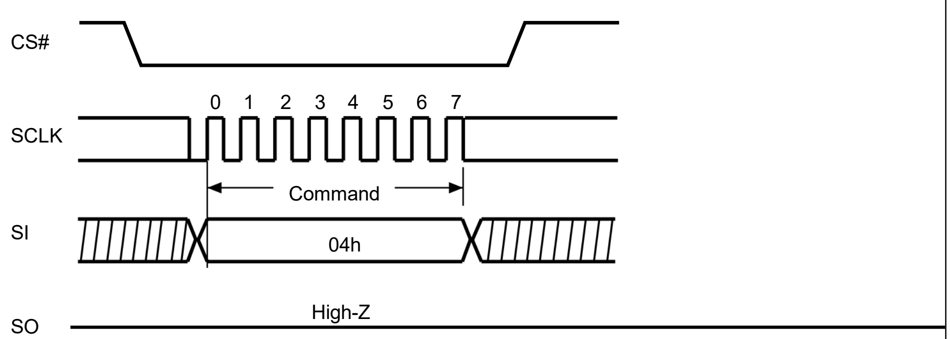
7-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion

Figure 4. Write Disable (WRDI) Sequence (Command 04)



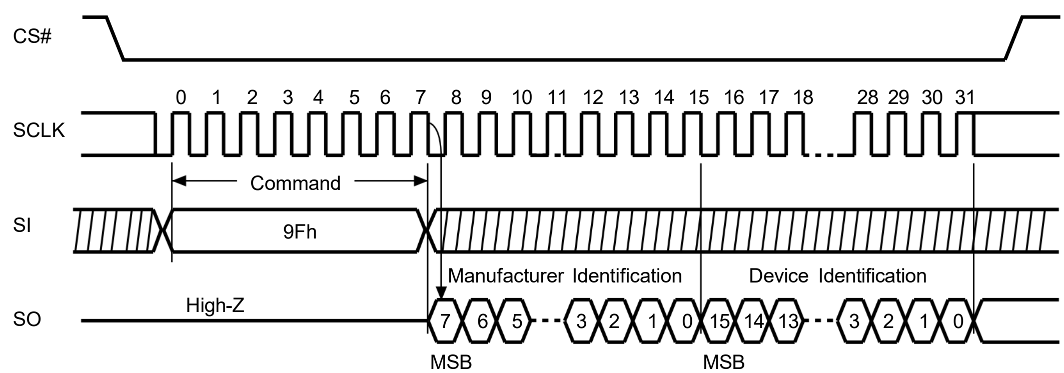
7-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Manufacturer ID and Device ID are listed as table of *"Table 6. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 5. Read Identification (RDID) Sequence (Command 9F)



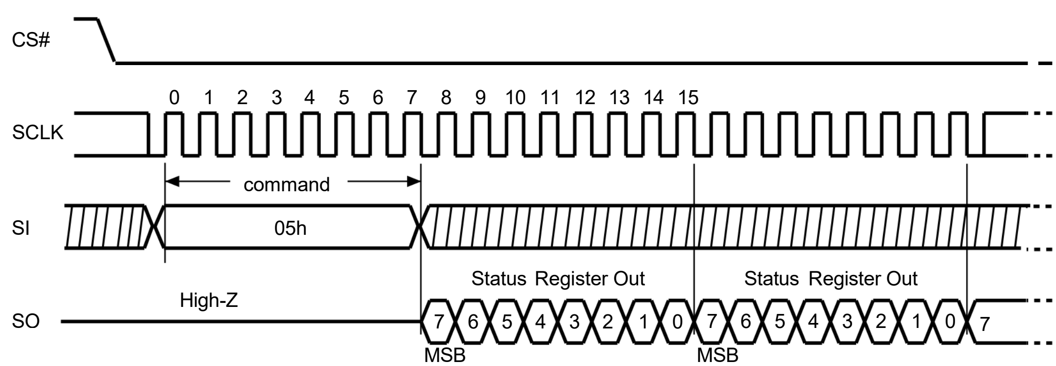
7-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

The SIO[3:1] are don't care.

Figure 6. Read Status Register (RDSR) Sequence (Command 05)



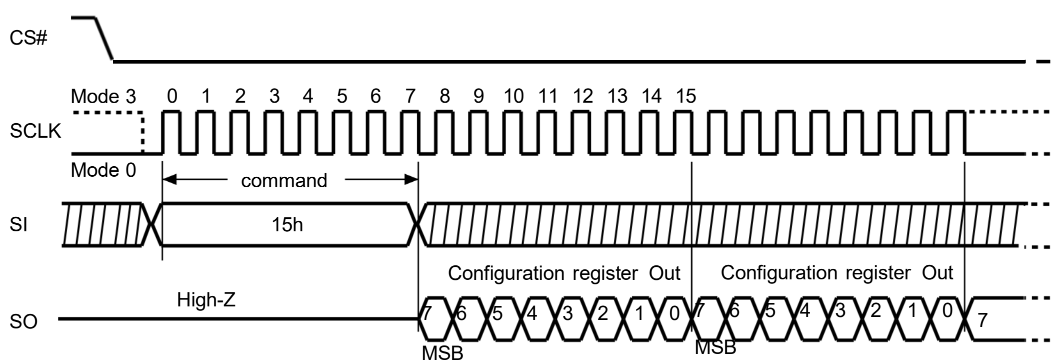
7-5. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

The SIO[3:1] are don't care.

Figure 7. Read Configuration Register (RDCR) Sequence



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 1. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1= Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the *"Table 1. Protected Area Sizes"*.

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit

The output driver strength ODS bit are volatile bits, which indicate the output driver level of the device. The Output Driver Strength is defaulted=1 when delivered from factory. To write the ODS bit requires the Write Status Register (WRSR) instruction to be executed.

TB bit

The Top/Bottom (TB) bit is a OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bit requires the Write Status Register (WRSR) instruction to be executed.

Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	DC (Dummy Cycle)	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	ODS
x	2READ/ 4READ Dummy Cycle	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	0,Output driver strength=1 1,Output driver strength=1/4 (Default=0)
x	volatile	x	x	OTP	x	x	volatile

Note: Refer to *"Dummy Cycle and Frequency Table"*, with "Don't Care" on other Reserved Configuration Registers.

Dummy Cycle and Frequency Table

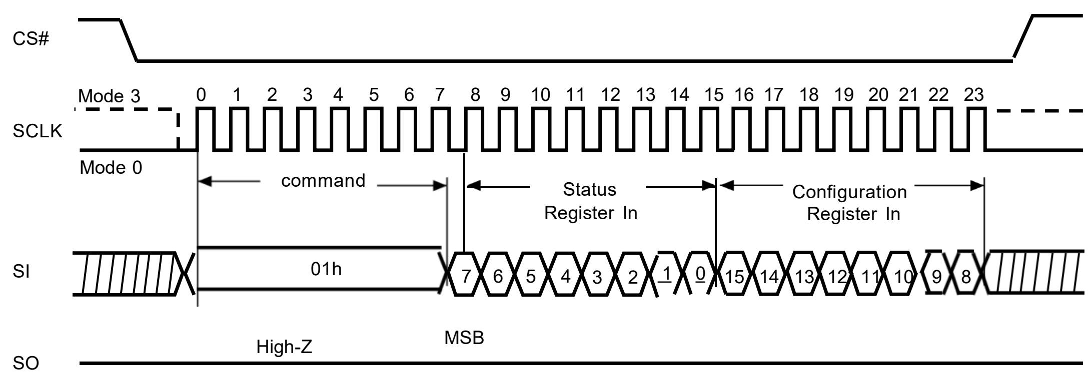
	DC	Numbers of Dummy Cycles	Freq. (MHz)
2READ	0 (default)	4	104
	1	8	133
4READ	0 (default)	6	104
	1	10	133

7-6. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 1. Protected Area Sizes"*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high.

Figure 8. Write Status Register (WRSR) Sequence (Command 01)



The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 5. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be programmed or erased.
Hardware protection mode (HPM)	The SRWD, BP0-BP3, TB of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be programmed or erased.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0, TB) bits of the Status Register, as shown in *"Table 1. Protected Area Sizes"*.

As the table above showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM):

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

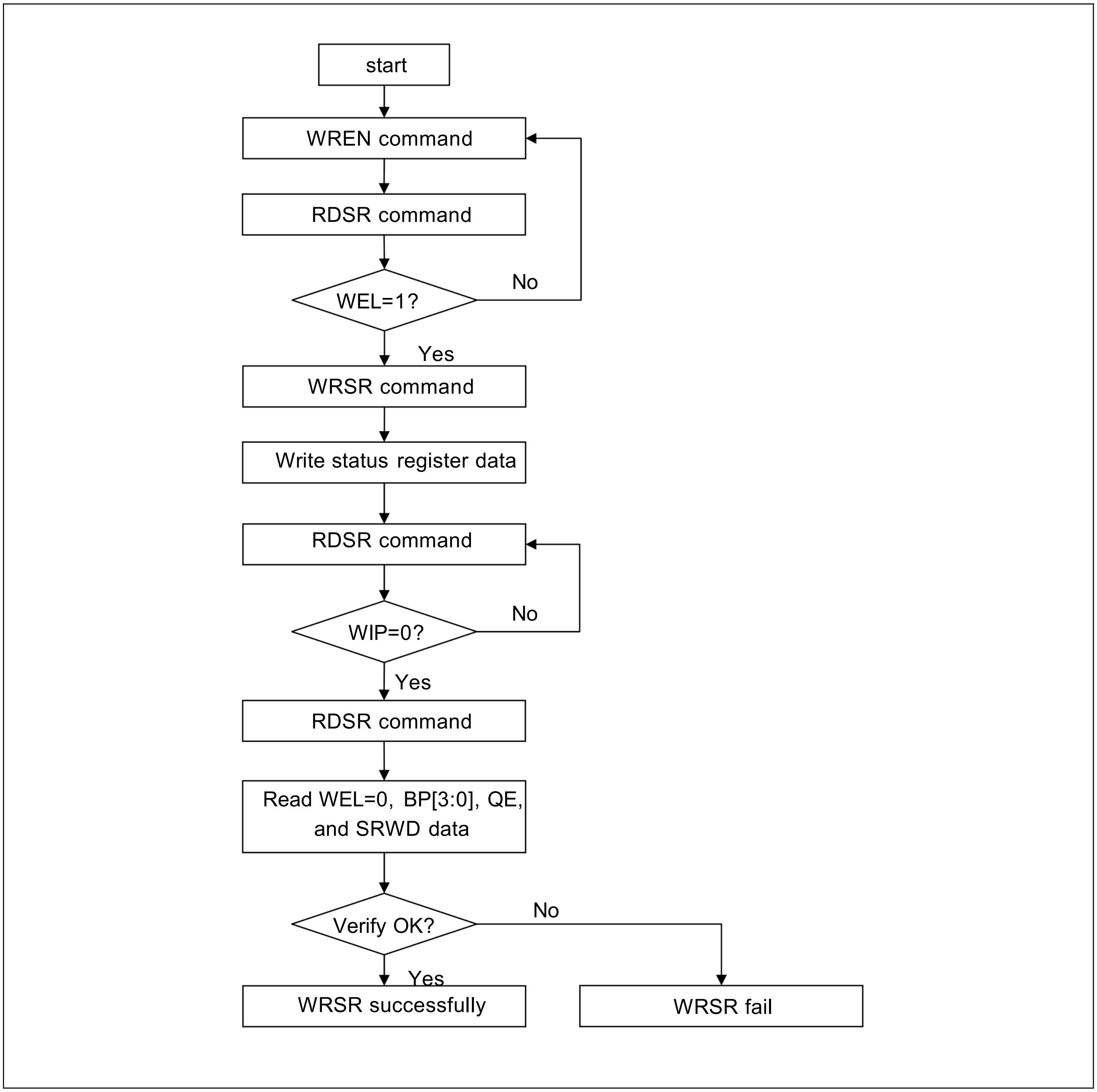
Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0, TB and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0, TB.
If the system goes into four I/O mode, the feature of HPM will be disabled.

Figure 9. WRSR flow

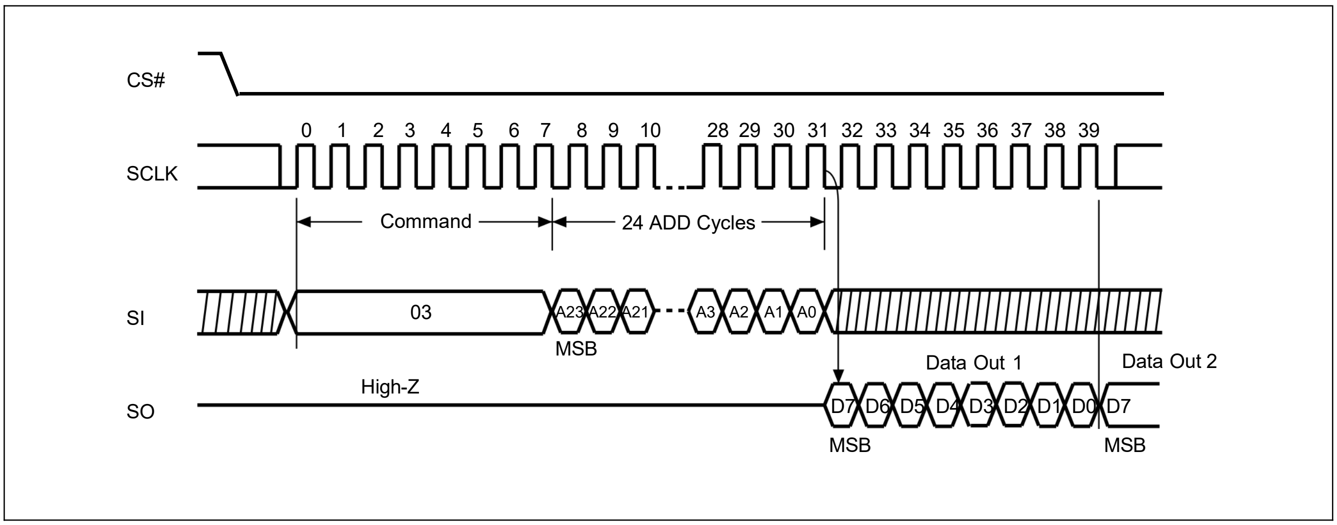


7-7. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→3-byte address on SI →data out on SO→ to end READ operation can use CS# to high at any time during data out.

Figure 10. Read Data Bytes (READ) Sequence (Command 03)



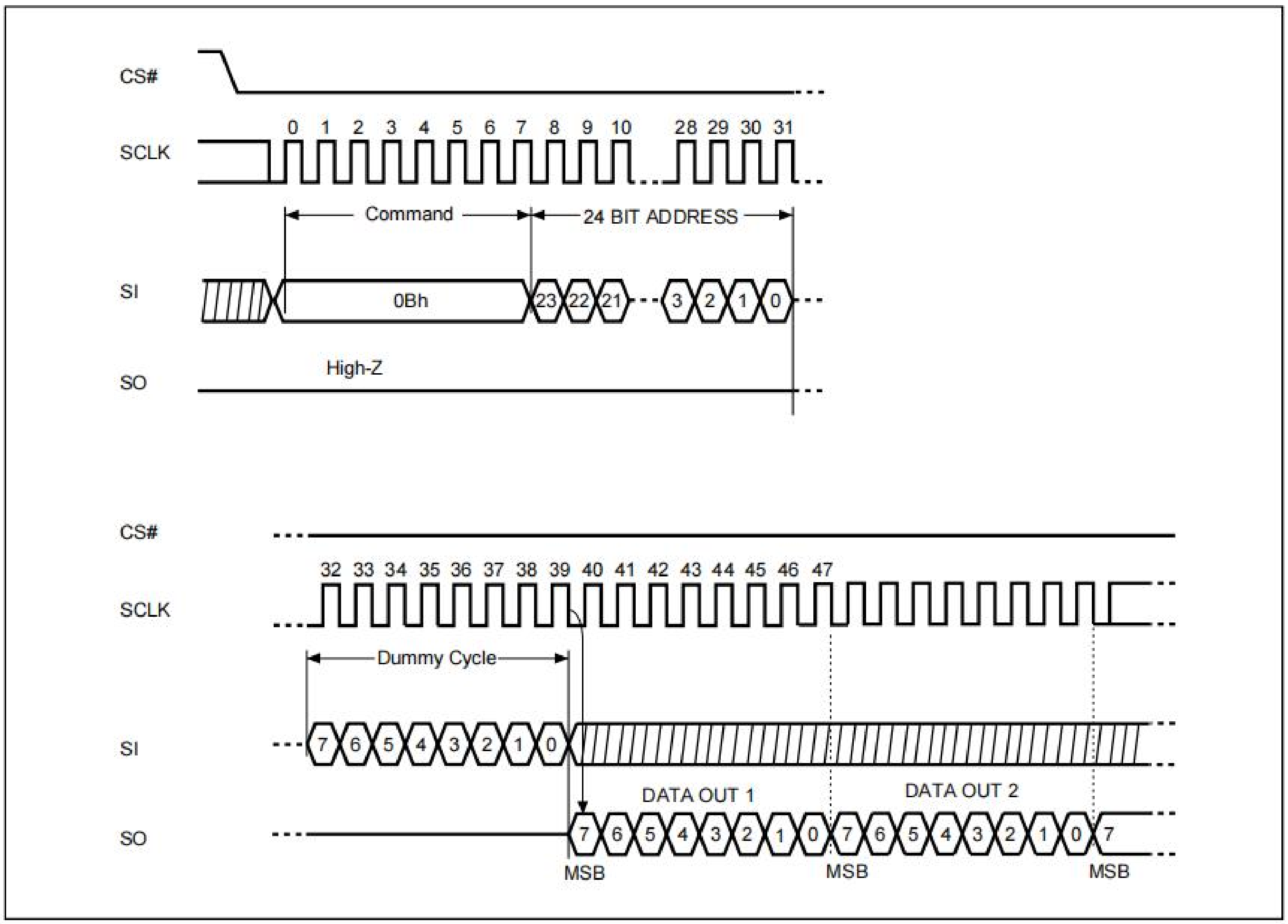
7-8. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *"Figure 11. Read at Higher Speed (FAST_READ) Sequence (Command 0B)"*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 11. Read at Higher Speed (FAST_READ) Sequence (Command 0B)



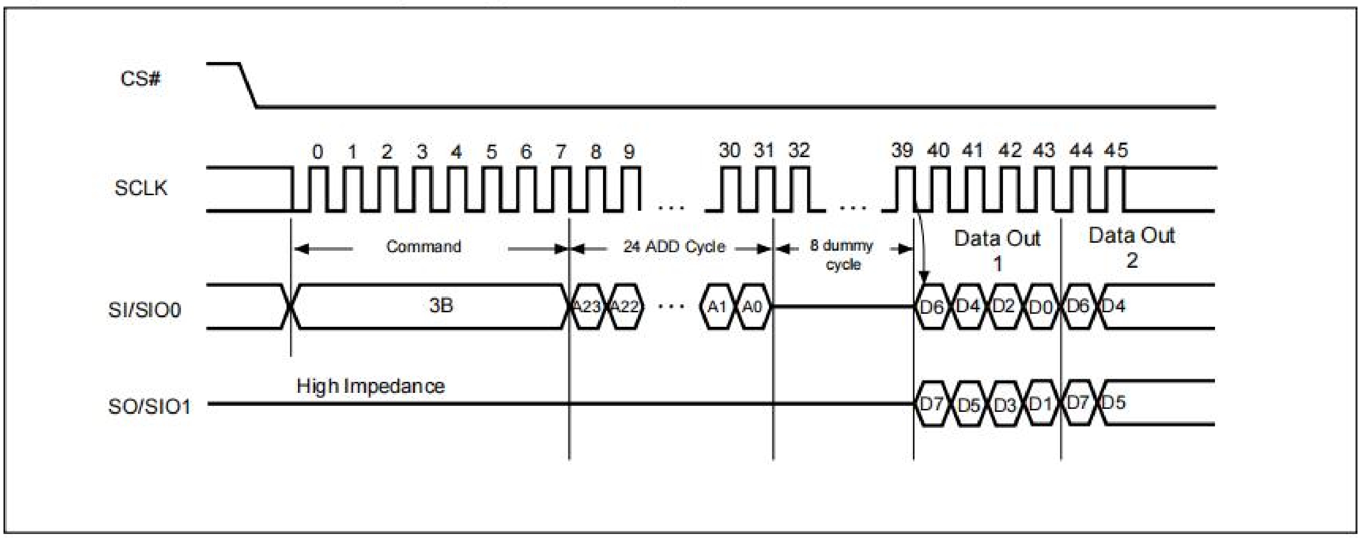
7-9. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 12. Dual Read Mode Sequence (Command 3B)



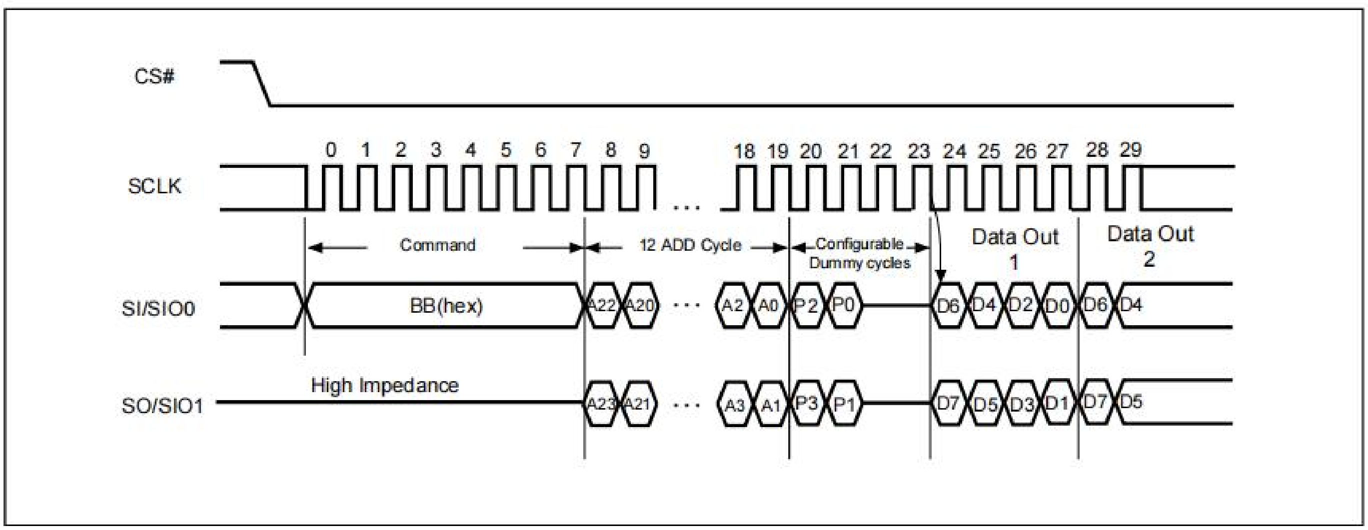
7-10. 2 x I/O Read Mode (2READ)

The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4 dummy cycles(default) on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 13. 2 x I/O Read Mode Sequence (Command BB)



Note: SI/SIO0 or SO/SIO1 should be kept "0h" or "Fh" in the first two dummy cycles. In other words, P2=P0 or P3=P1 is necessary.

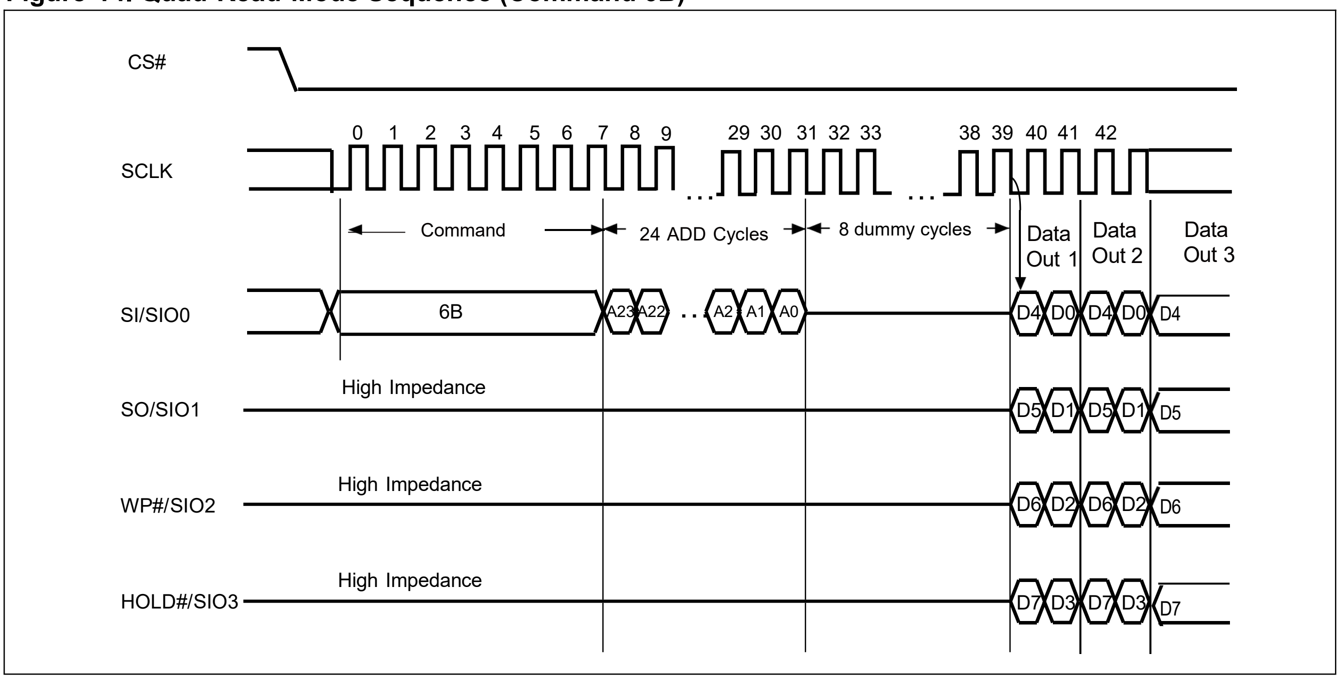
7-11. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 14. Quad Read Mode Sequence (Command 6B)

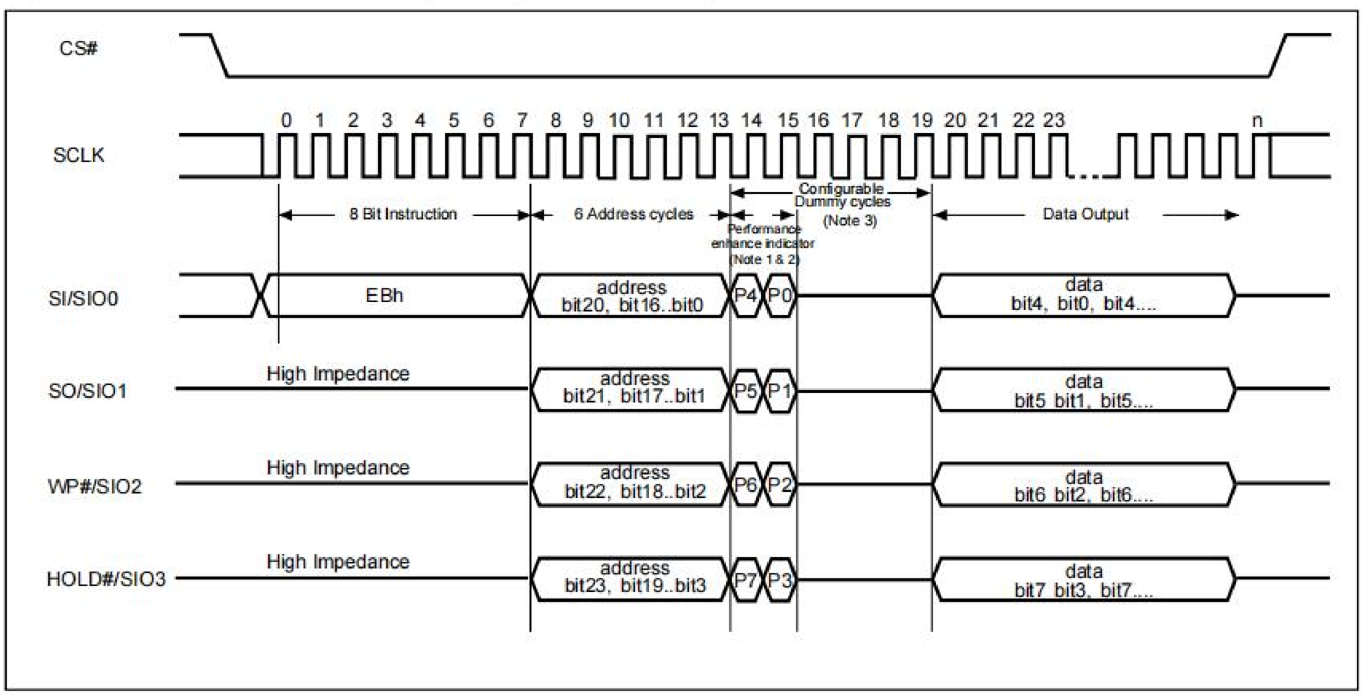


7-12. 4 x I/O Read Mode (4READ)

The 4READ instruction enables quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles (default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out. (Please refer to figure below)

Figure 15. 4 x I/O Read Mode Sequence (Command EB)



Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. The Configurable Dummy Cycle is set by Configuration Register Bit. Please see *"Dummy Cycle and Frequency Table"*

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→ sending 4READ instruction→ 3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles → data out until CS# goes high → CS# goes low (reduce 4READ instruction) → 24-bit random access address (Please refer to *"Figure 16. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode)"*).

In the performance-enhancing mode (Notes of *"Figure 16. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode)"*), P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h. These commands will reset the performance enhance mode. And afterwards CS# is raised and then lowered, the system then will return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

7-13. Performance Enhance Mode

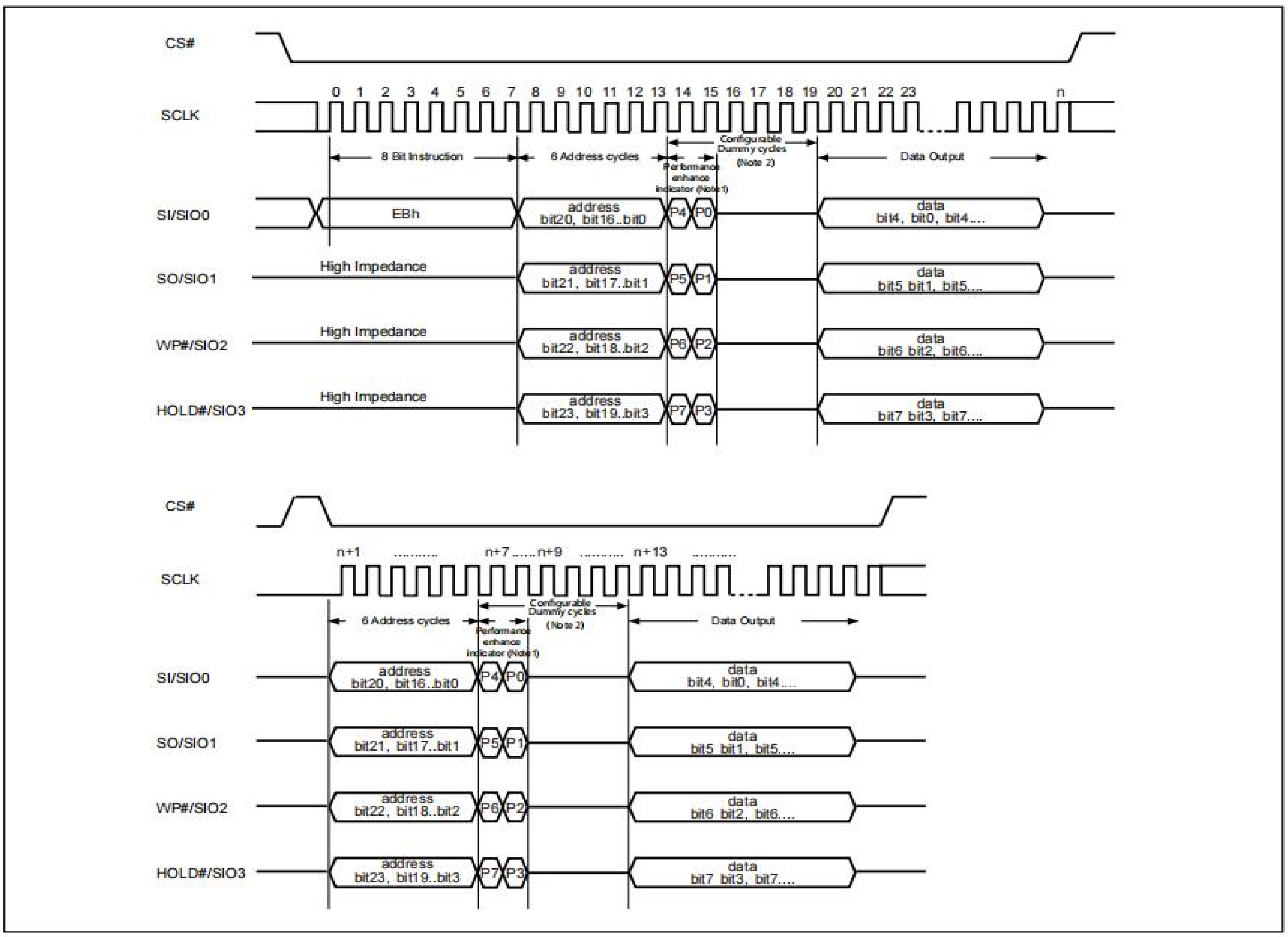
The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please note *"Figure 16. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode)"*)

Performance enhance mode is supported for 4READ mode.
"EBh" commands support enhance mode.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue "FFh" data cycles to exit enhance mode.

Figure 16. 4 x I/O Read enhance performance Mode Sequence (Command EB) (SPI Mode)



Note:

1. Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
   Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF
2. The Configurable Dummy Cycle is set by Configuration Register Bit. Please see *"Dummy Cycle and Frequency Table"*

7-14. Burst Read

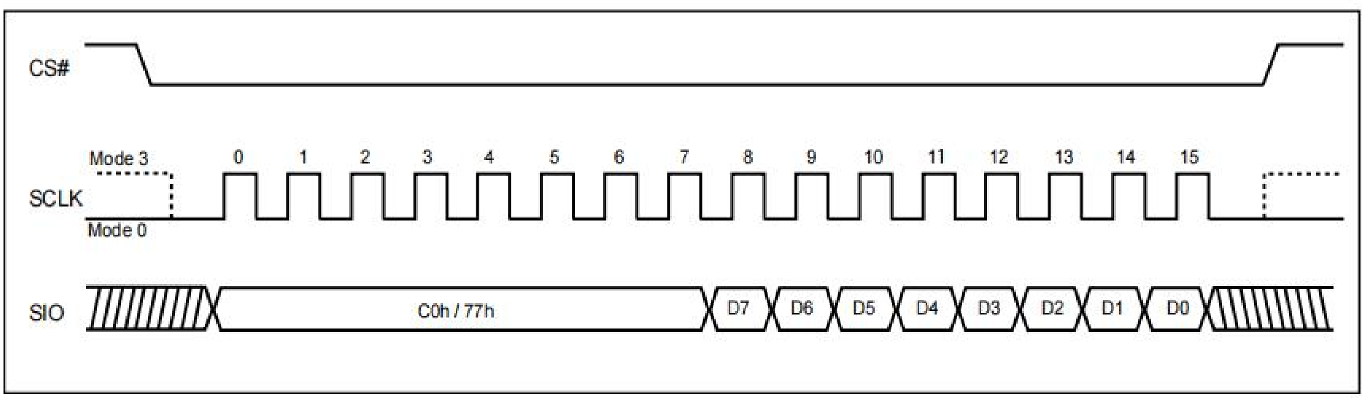
The Burst Read feature allows applications to fill a cache line with a fixed length of data without using multiple read commands. Burst Read is disabled by default at power-up or reset. Burst Read is enabled by setting the Burst Length. When the Burst Length is set, reads will wrap on the selected boundary (8/16/32/64-bytes) containing the initial target address. For example if an 8-byte Wrap Depth is selected, reads will wrap on the 8-byte-page-aligned boundary containing the initial read address.

To set the Burst Length, drive CS# low → send SET BURST LENGTH instruction code → send WRAP CODE → drive CS# high. Refer to the table below for valid 8-bit Wrap Codes and their corresponding Wrap Depth.

Data	WrapAround	Wrap Depth
00h	Yes	8-byte
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

Once Burst Read is enabled, it will remain enabled until the device is power-cycled or reset. The 4READ read command supports the wrap around feature after Burst Read is enabled. To change the wrap depth, resend the Burst Read instruction with the appropriate Wrap Code. To disable Burst Read, send the Burst Read instruction with Wrap Code 1xh. “EBh" supports wrap around feature after wrap around is enabled.

Figure 17. Burst Read



7-15. Sector Erase (SE)

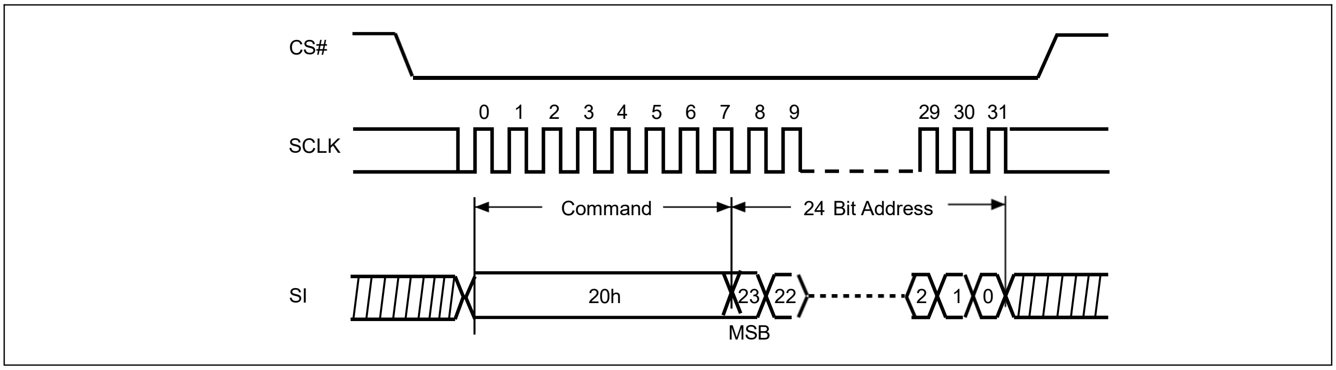
The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 3. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI →CS# goes high.

The SIO[3:1] are don't care.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP3~0, the array data will be protected (no change) and the WEL bit still be reset.

Figure 18. Sector Erase (SE) Sequence (Command 20)



7-16. Block Erase (BE)

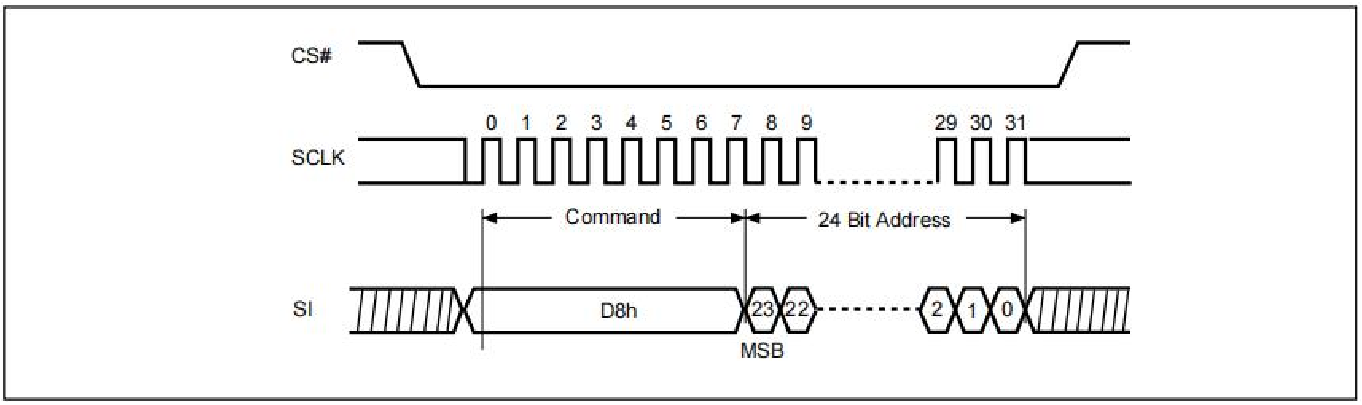
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0, the array data will be protected (no change) and the WEL bit still be reset.

Figure 19. Block Erase (BE) Sequence (Command D8)



7-17. Block Erase (BE32K)

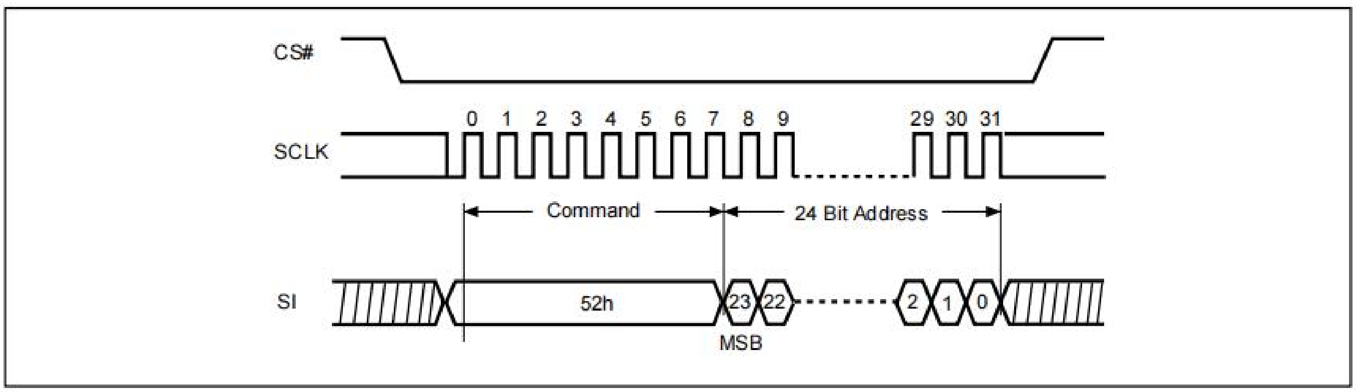
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0, the array data will be protected (no change) and the WEL bit still be reset.

Figure 20. Block Erase 32KB (BE32K) Sequence (Command 52)



7-18. Chip Erase (CE)

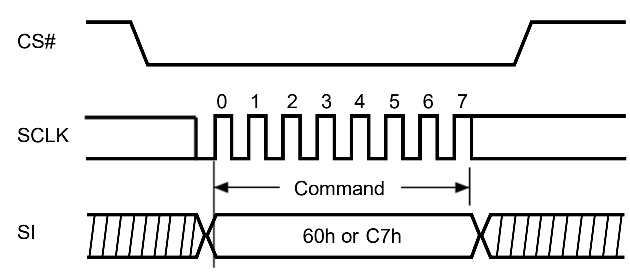
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected the Chip Erase (CE) instruction will not be executed, but WEL will be reset.

Figure 21. Chip Erase (CE) Sequence (Command 60 or C7)



7-19. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the eight least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the requested page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

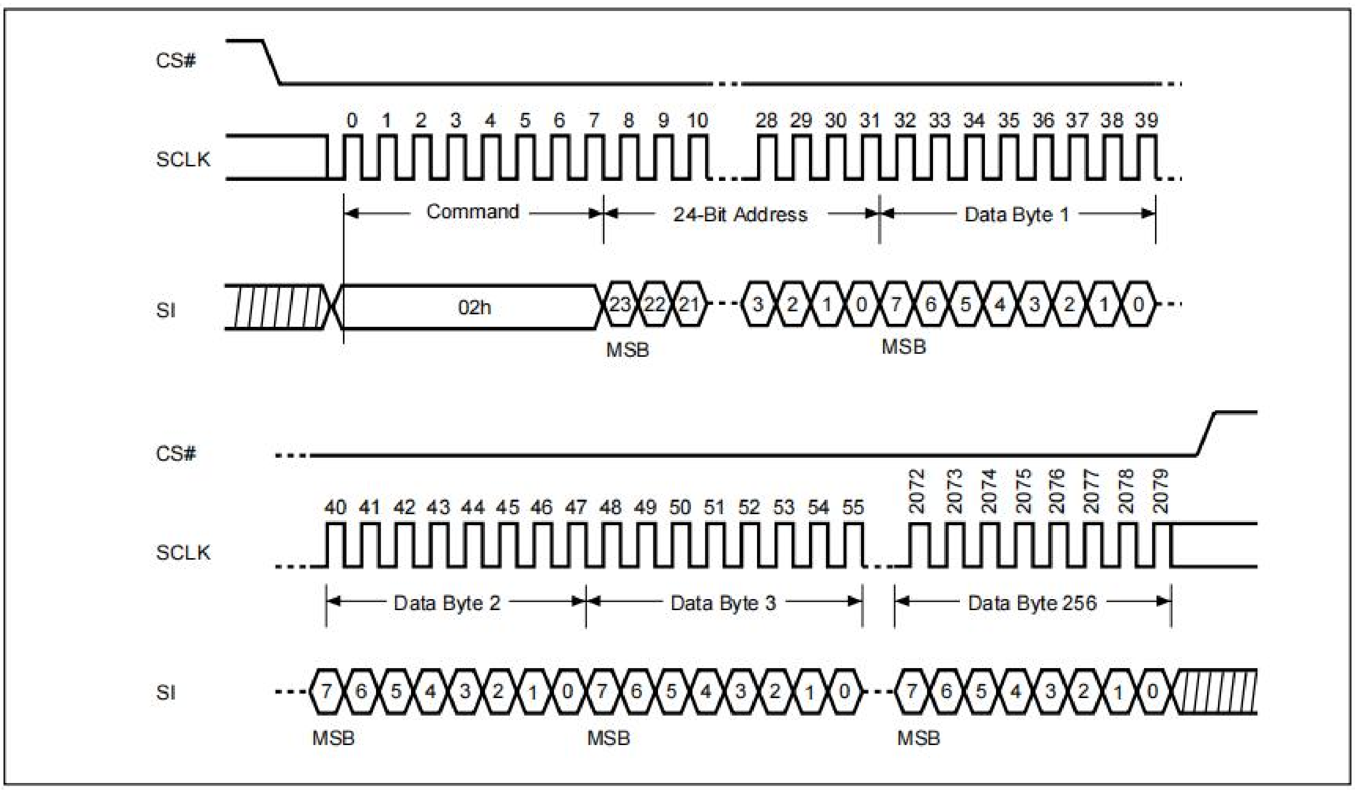
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise, the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP3~0, the array data will be protected (no change) and the WEL bit will still be reset.

The SIO[3:1] are don't care.

Figure 22. Page Program (PP) Sequence (Command 02)



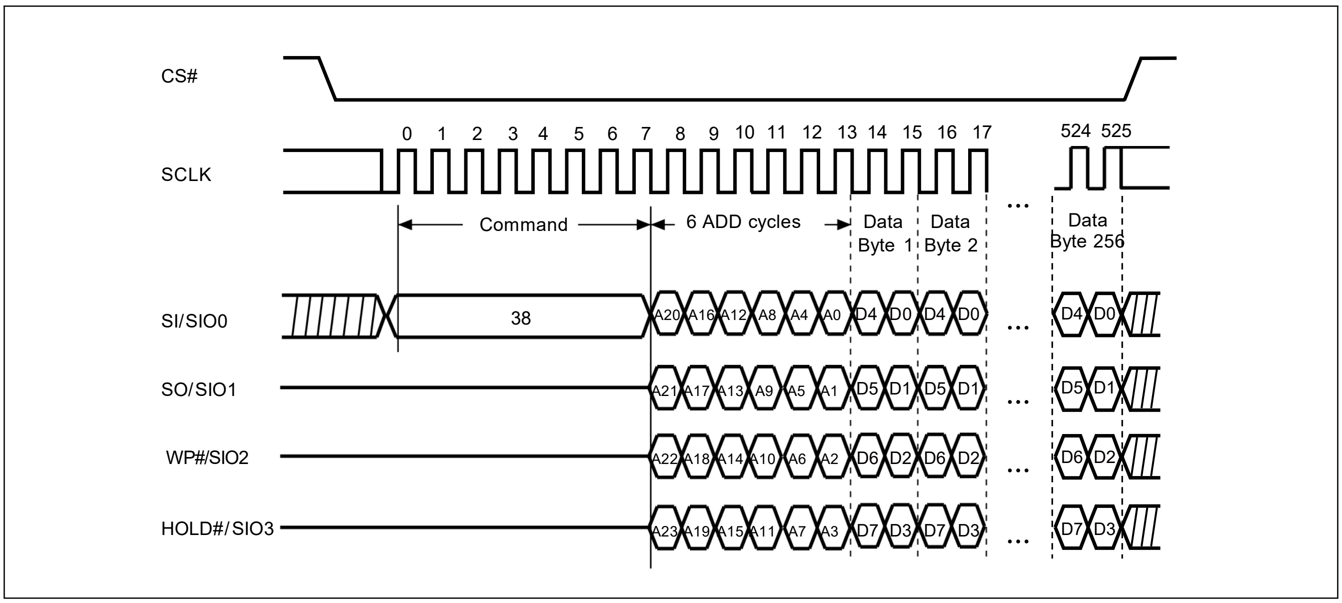
7-20. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3, which can raise programmer performance and the effectiveness of application of lower clock less than 133MHz. For system with faster clock, the Quad page program cannot provide more performance, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 133MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high.

If the page is protected by BP3~0, the array data will be protected (no change) and the WEL bit will still be reset.

Figure 23. 4 x I/O Page Program (4PP) Sequence (Command 38)



The Program/Erase function instruction function flow is as follows:

Figure 24. Program/Erase Flow(1) with read array data

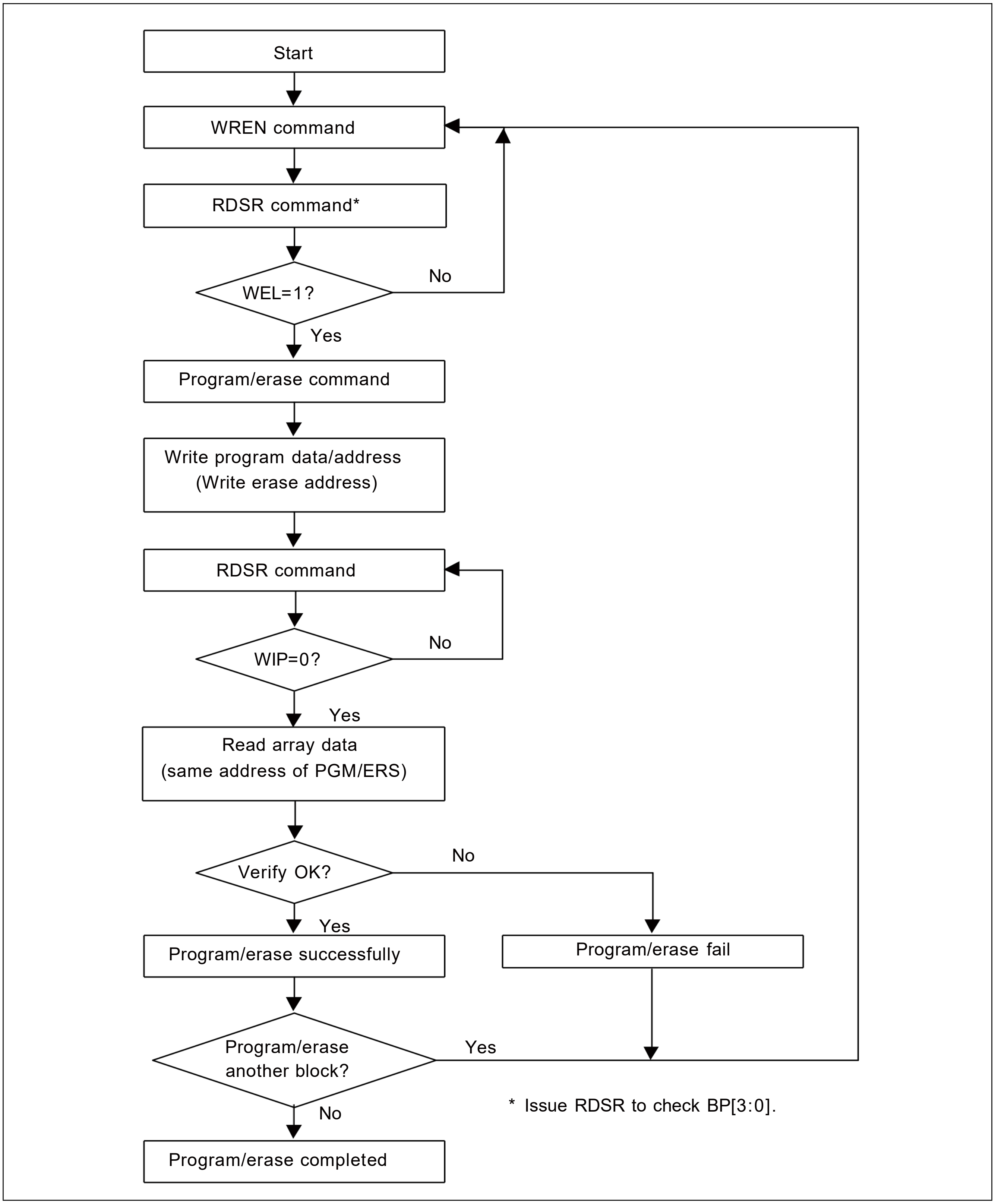
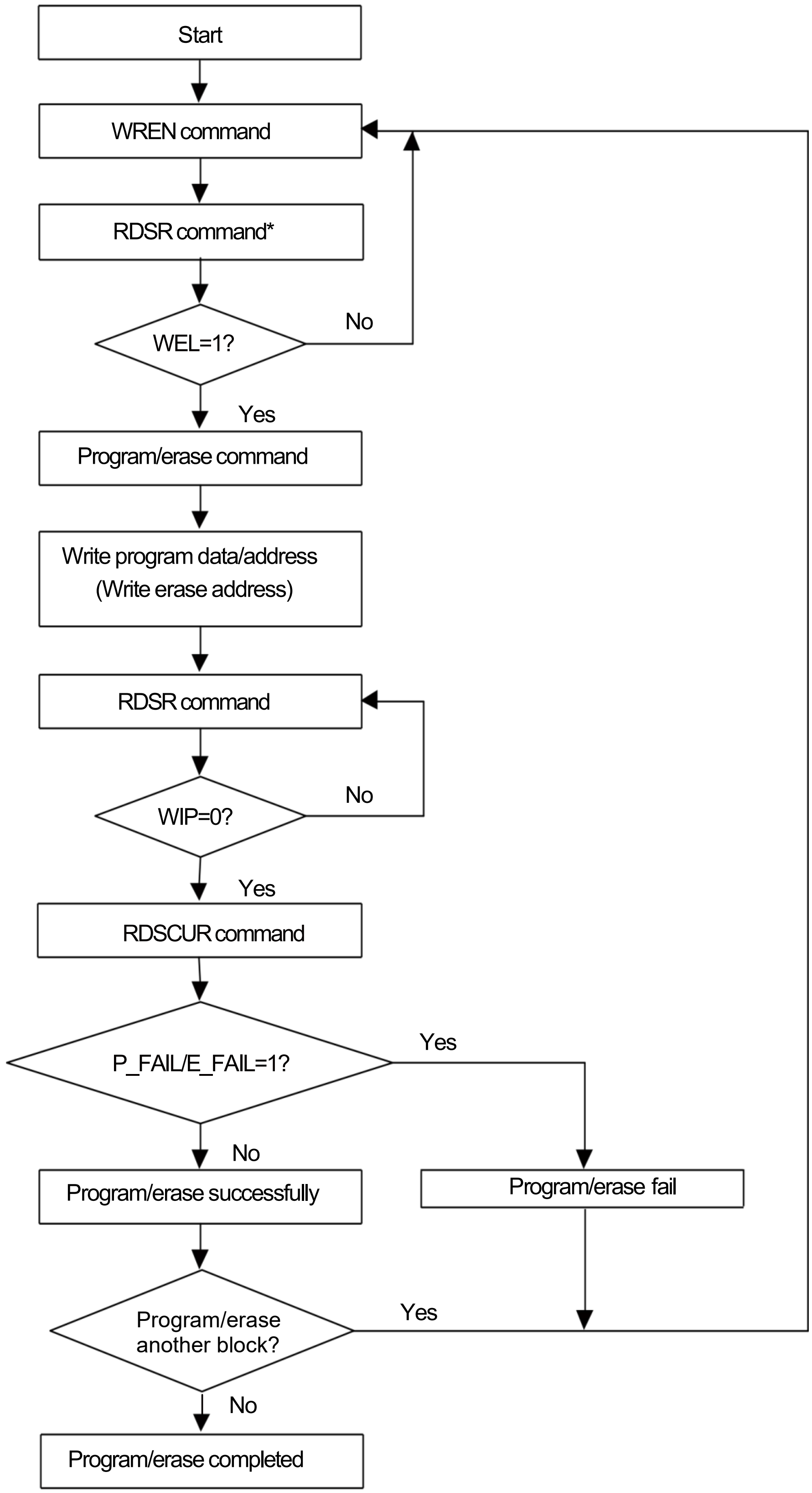


Figure 25. Program/Erase Flow(2) without read array data



7-21. Deep Power-down (DP)

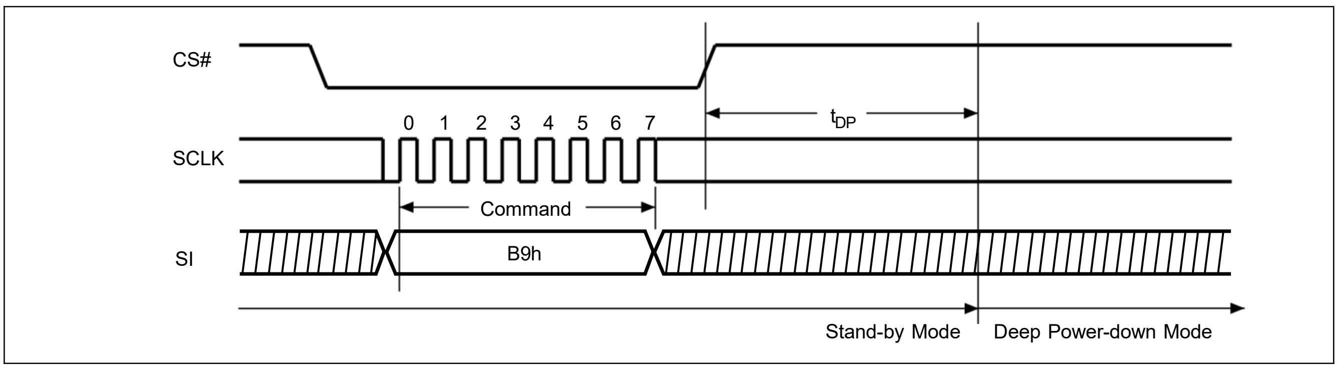
The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instructions are ignored. When CS# goes high, the device is in standby mode not deep power-down mode.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high.

The SIO[3:1] are don't care when during this mode.

Once the DP instruction is set, all instructions will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code has been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

Figure 26. Deep Power-down (DP) Sequence (Command B9)



7-22. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 12. AC Characteristics"*. Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 6. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress.

The SIO[3:1] are don't care when during this mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

Figure 27. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

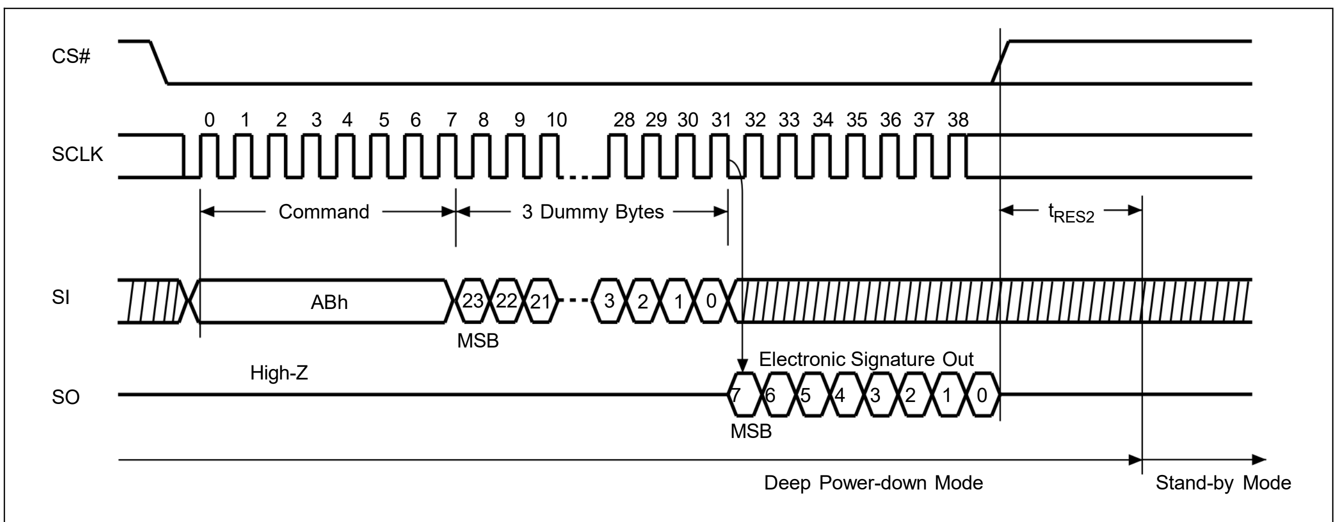
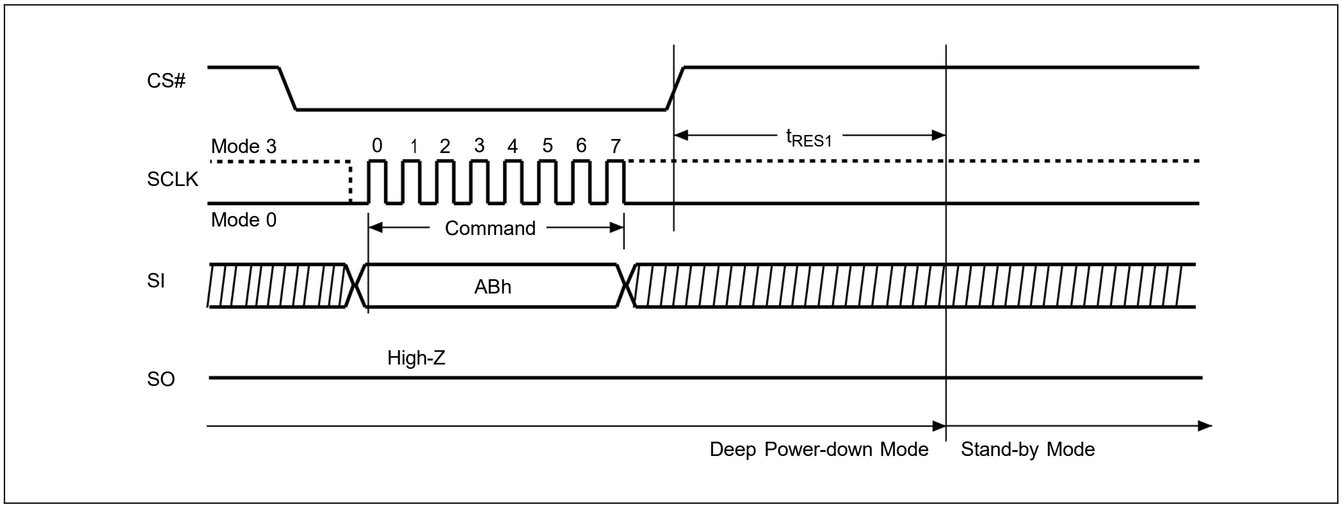


Figure 28. Release from Deep Power-down (RDP) Sequence

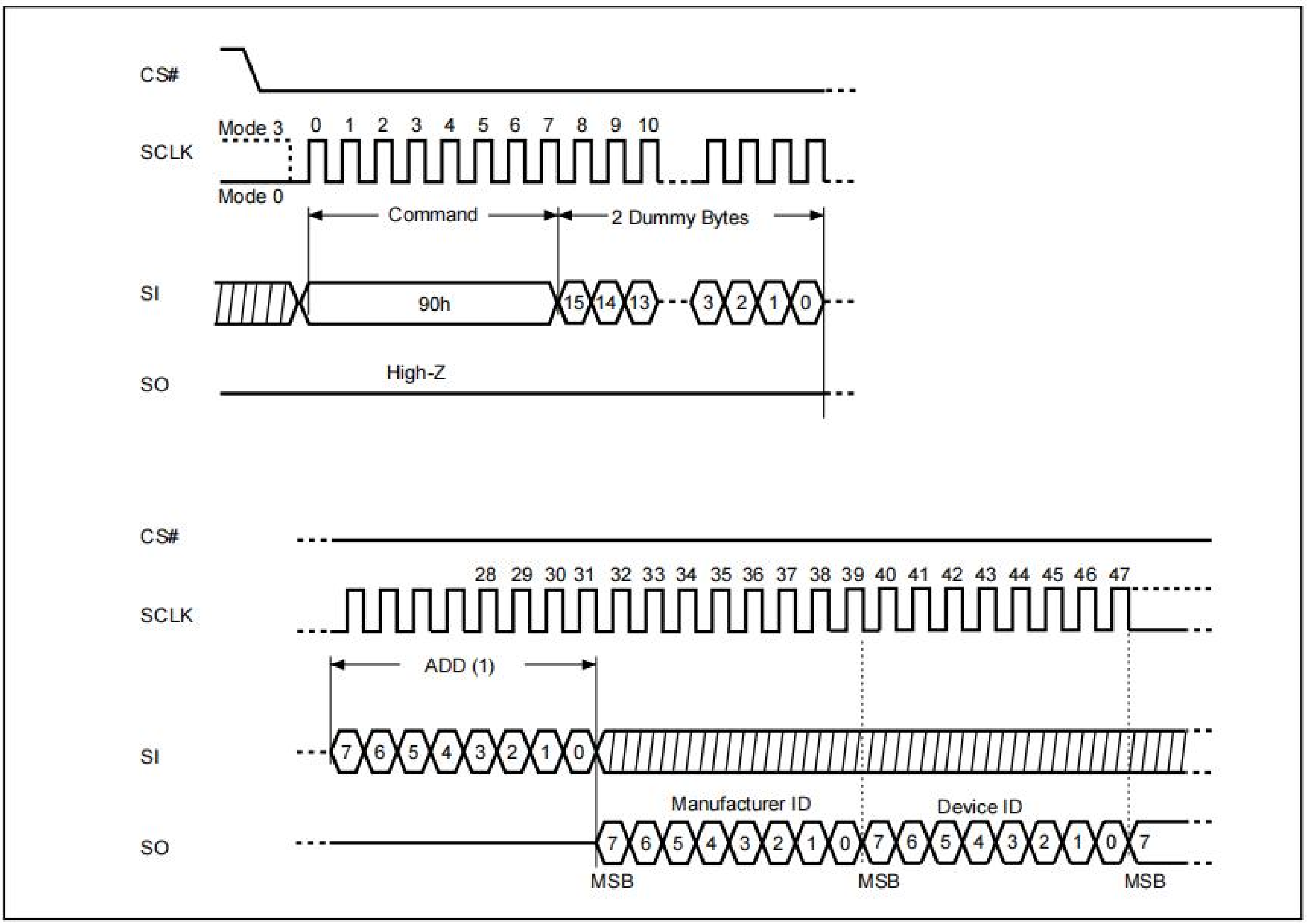


7-23. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for ZETTA and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID values are listed in *"Table 6. ID Definitions"*. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 29. Read Electronic Manufacturer & Device ID (REMS) Sequence



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

Table 6. ID Definitions

Command Type	NB25Q32A		
RDID	Manufactory ID	Memory type	Memory density
		20	16
RES	Electronic ID		
	15		
REMS	Manufactory ID	Device ID	
		15	

7-24. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit Secured OTP mode. While the device is in 4K-bit Secured OTP mode, array access is not available. The additional 4K-bit Secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

The SIO[3:1] are don't care.

Please note that WRSR/WRSCUR/CE/BE/SE/BE32K commands are not acceptable during the access of secure OTP region, once Security OTP is locked down, only read related commands are valid.

7-25. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit Secured OTP mode.
The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

The SIO[3:1] are don't care.

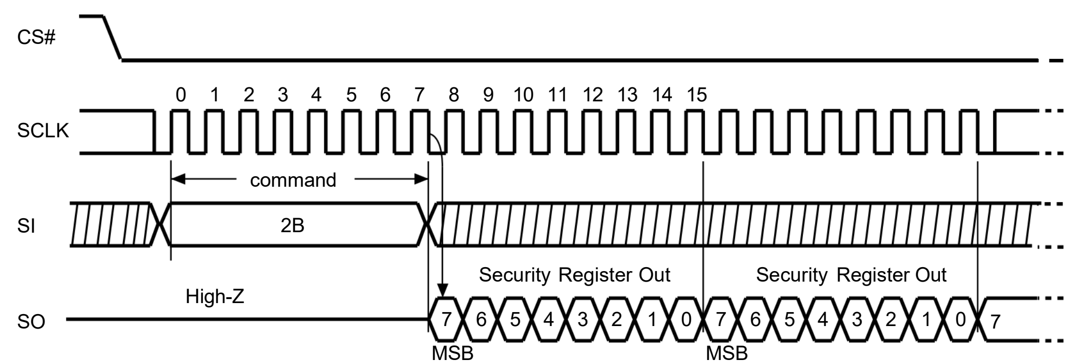
7-26. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→ sending RDSCUR instruction → Security Register data out on SO→ CS# goes high.

The SIO[3:1] are don't care.

Figure 30. Read Security Register (RDSCUR) Sequence (Command 2B)



The definition of the Security Register is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more.

Program Suspend Status bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Erase Suspend Status bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Fail Flag bit. While a program failure happened, the Program Fail Flag bit would be set. If the program operation fails on a protected memory region or locked OTP region, this bit will also be set. This bit can be the failure indication of one or more program operations. This fail flag bit will be cleared automatically after the next successful program operation.

Erase Fail Flag bit. While an erase failure happened, the Erase Fail Flag bit would be set. If the erase operation fails on a protected memory region or locked OTP region, this bit will also be set. This bit can be the failure indication of one or more erase operations. This fail flag bit will be cleared automatically after the next successful erase operation.

Table 7. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend status)	PSB (Program Suspend status)	LDSO (lock-down 4K-bit Secured OTP)	Secured OTP Indicator bit (4K-bit Secured OTP)
Reserved	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	Reserved	0=Erase is not suspended 1=Erase is suspended (default=0)	0=Program is not suspended 1=Program is suspended (default=0)	0 = not lockdown 1 = lock-down (cannot program/erase OTP)	0 = nonfactory lock 1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit
Reserved	Read Only	Read Only		Read Only	Read Only	OTP	Read Only

7-27. Write Security Register (WRSCUR)

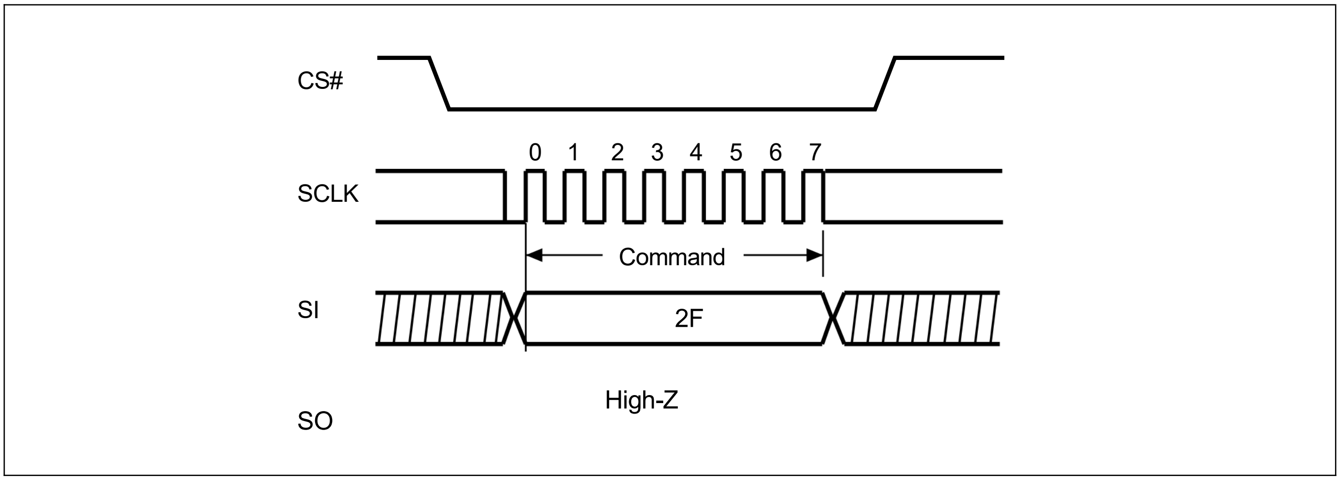
The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The SIO[3:1] are don't care.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Figure 31. Write Security Register (WRSCUR) Sequence (Command 2F) (SPI mode)



7-28. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased (*"Table 8. Readable Area of Memory While a Program or Erase Operation is Suspended"*).

Table 8. Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Sector Erase (4KB)	All but the 4KB Sector being erased
Block Erase (32KB)	All but the 32KB Block being erased
Block Erase (64KB)	All but the 64KB Block being erased

When the serial flash receives the Suspend instruction, there is a latency of tPSL or tESL (*"Figure 32. Suspend to Read Latency"*) before the Write Enable Latch (WEL) bit clears to “0” and the PSB or ESB sets to “1”, after which the device is ready to accept one of the commands listed in *"Table 9. Acceptable Commands During Program/Erase Suspend after tPSL/tESL"* (e.g. FAST READ). Refer to *"Table 12. AC Characteristics"* for tPSL and tESL timings. *"Table 10. Acceptable Commands During Suspend (tPSL/tESL not required)"* lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status. The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

Figure 32. Suspend to Read Latency

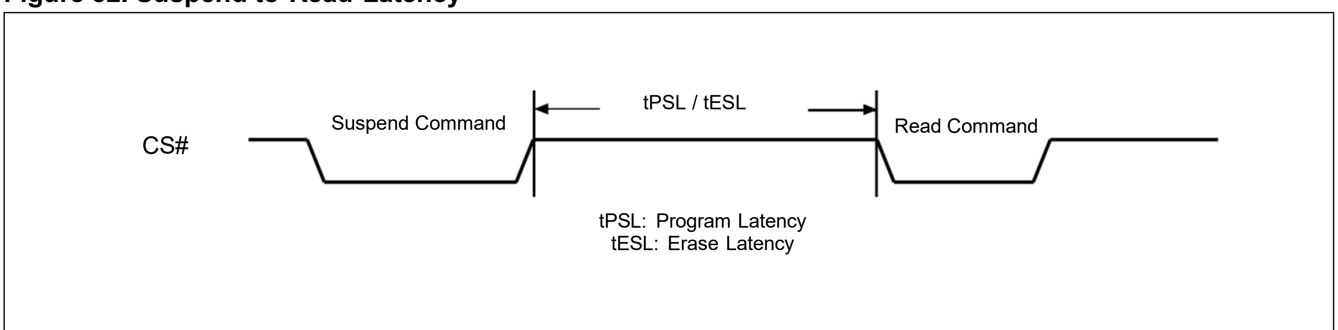


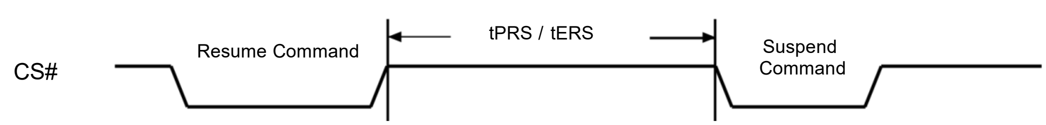
Table 9. Acceptable Commands During Program/Erase Suspend after tPSL/tESL

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03h	•	•
FAST READ	0Bh	•	•
DREAD	3Bh	•	•
QREAD	6Bh	•	•
2READ	BBh	•	•
4READ	EBh	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
REMS	90h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
SBL	C0h or 77h	•	•
WREN	06h		•
RESUME	7Ah or 30h	•	•
PP	02h		•
4PP	38h		•

Table 10. Acceptable Commands During Suspend (tPSL/tESL not required)

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDSCUR	2Bh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

Figure 33. Resume to Suspend Latency



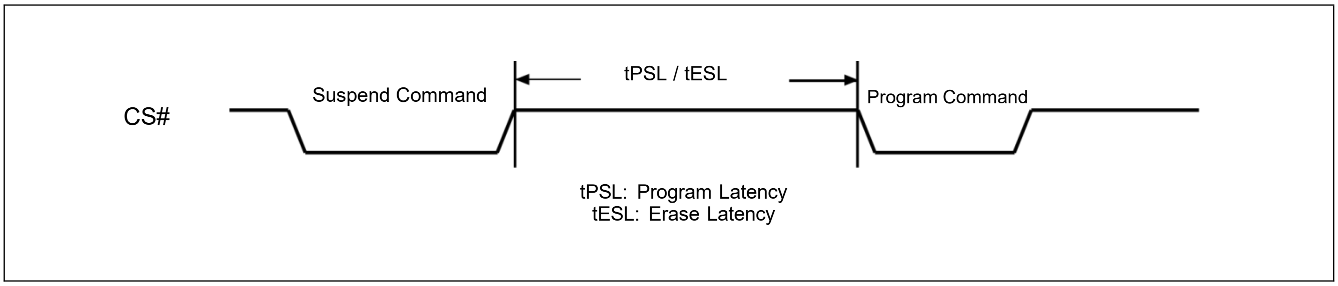
tPRS: Program Resume to another Suspend
tERS: Erase Resume to another Suspend

7-28-1. Program Suspend

The “Erase Suspend to Program” feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (WREN) instruction must be issued before any Page Program instruction.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The WEL and WIP bits of the Status Register will remain “1” while the Page Program operation is in progress and will both clear to “0” when the Page Program operation completes.

Figure 34. Suspend to Program Latency



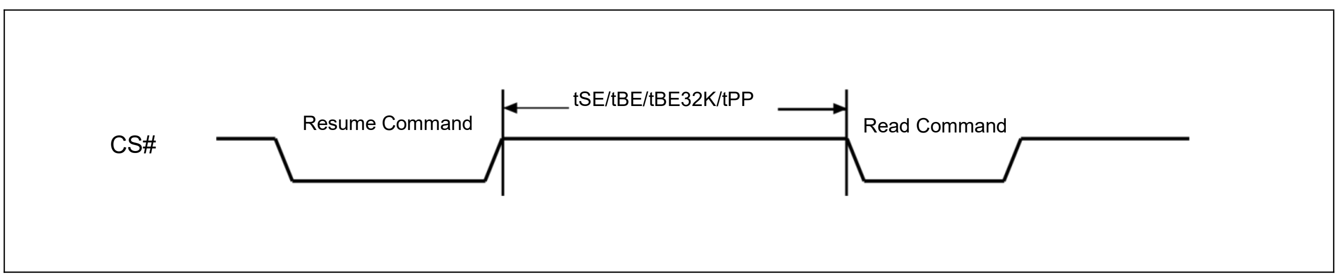
7-29. Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the serial flash receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”. The program or erase operation will continue until finished (*"Figure 35. Resume to Read Latency"*) or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction (*"Figure 33. Resume to Suspend Latency"*).

Please note that the Resume instruction will be ignored if the serial flash is in “Performance Enhance Mode”. Make sure the serial flash is not in “Performance Enhance Mode” before issuing the Resume instruction.

Figure 35. Resume to Read Latency



7-30. No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

7-31. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

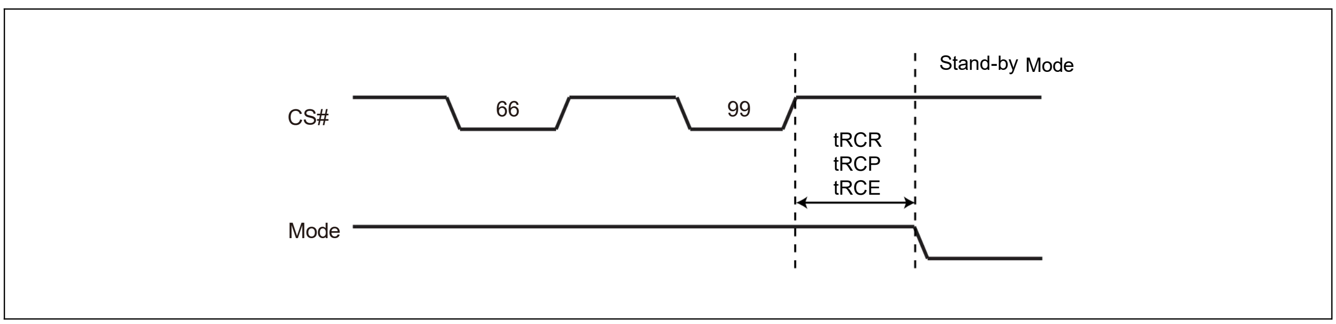
The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

Figure 36. Software Reset Recovery



7-32. Read SFDP Mode (RDSFDP)

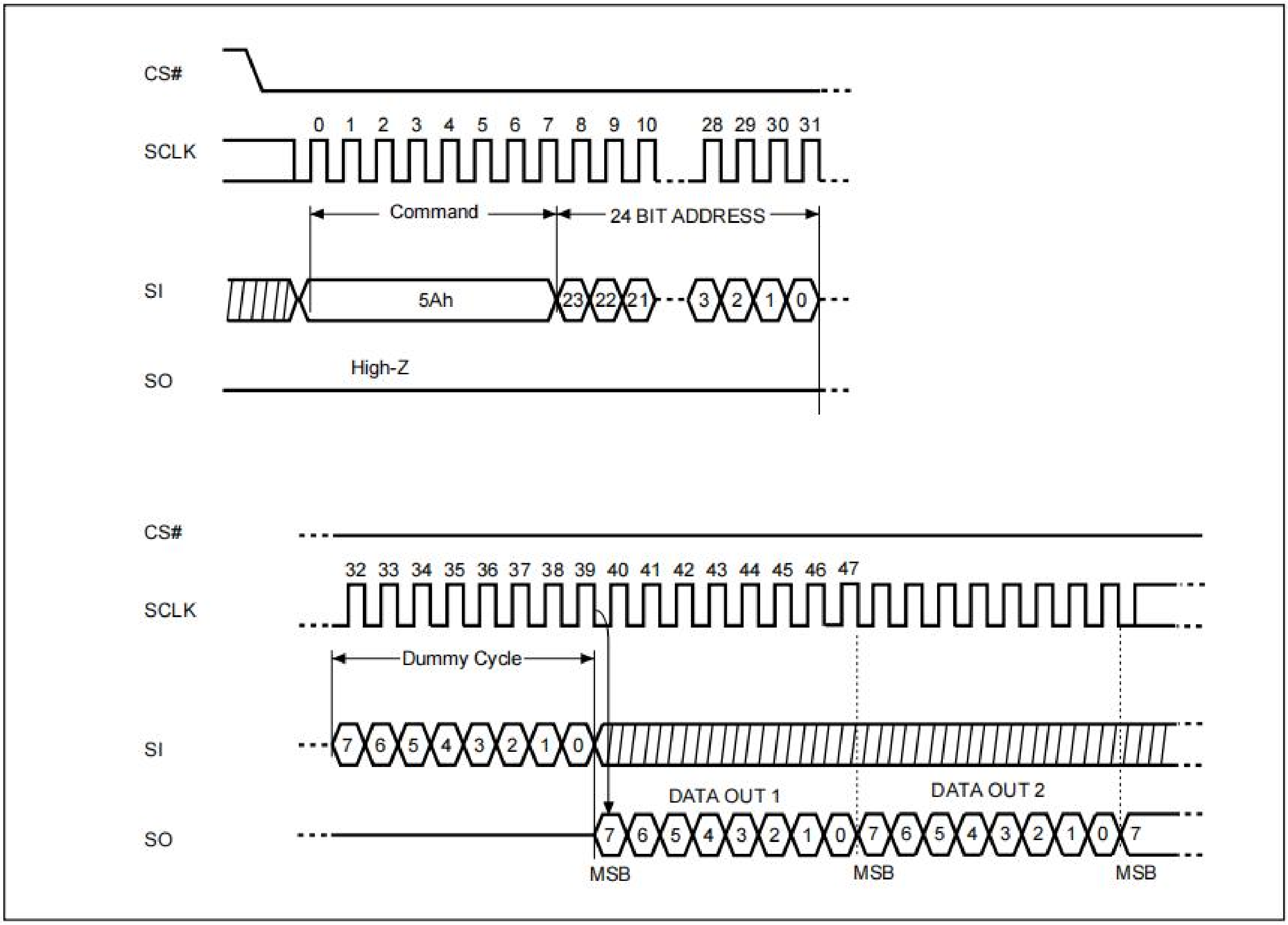
The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

For SFDP register values detail, please contact local ZETTA sales channel for Application Note.

Figure 37. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



8. POWER-ON STATE

The device is at the following states after power-up:

- Standby mode
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal Power-on Reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

9. Electrical Specifications

9-1. Absolute Maximum Ratings

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to 4.6V
Applied Output Voltage		-0.5V to 4.6V
VCC to Ground Potential		-0.5V to 4.6V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see the figures below.

Figure 38. Maximum Negative Overshoot Waveform

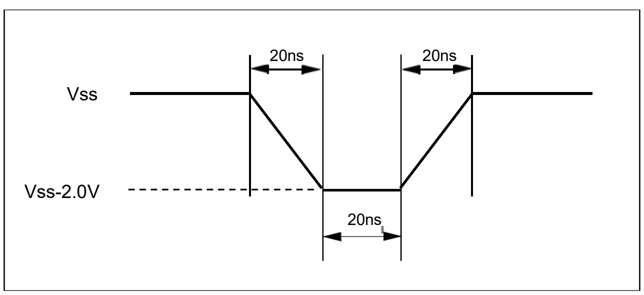
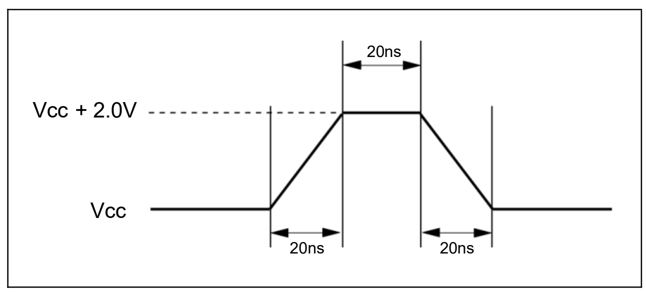


Figure 39. Maximum Positive Overshoot Waveform



9-2. Capacitance TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 40. Data Input Test Waveforms and Measurement Level

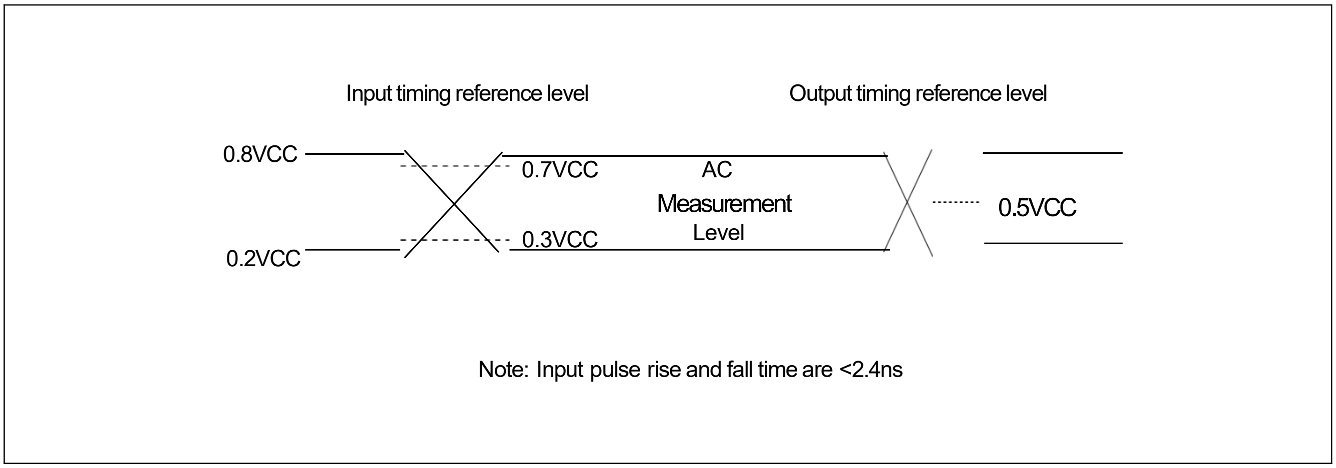


Figure 41. Output Loading

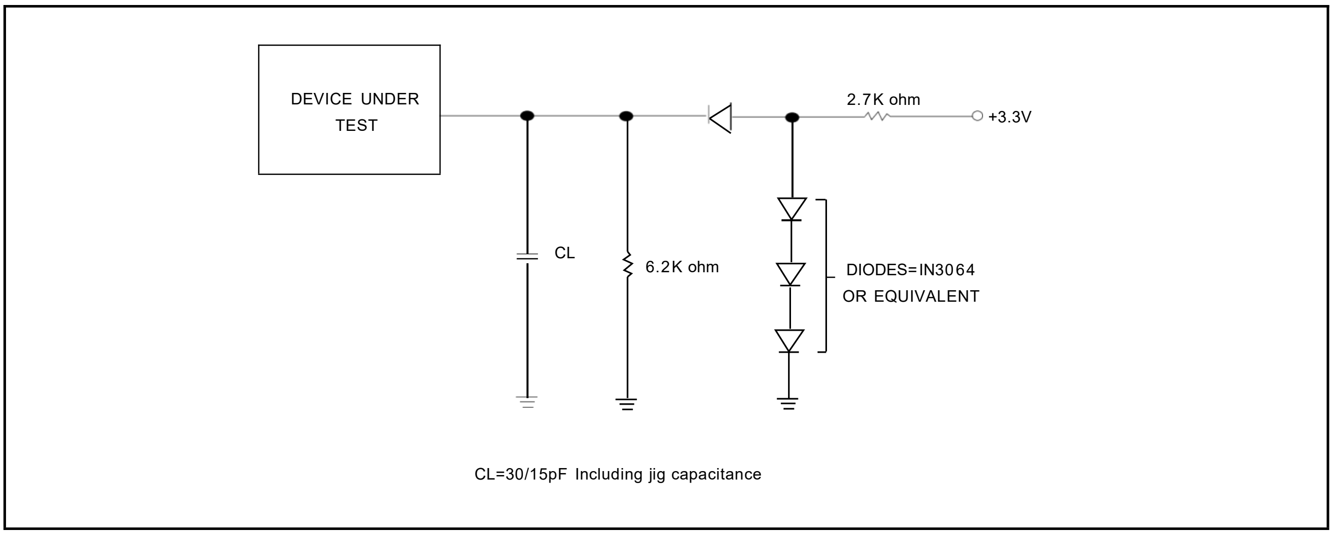


Figure 42. SCLK TIMING DEFINITION

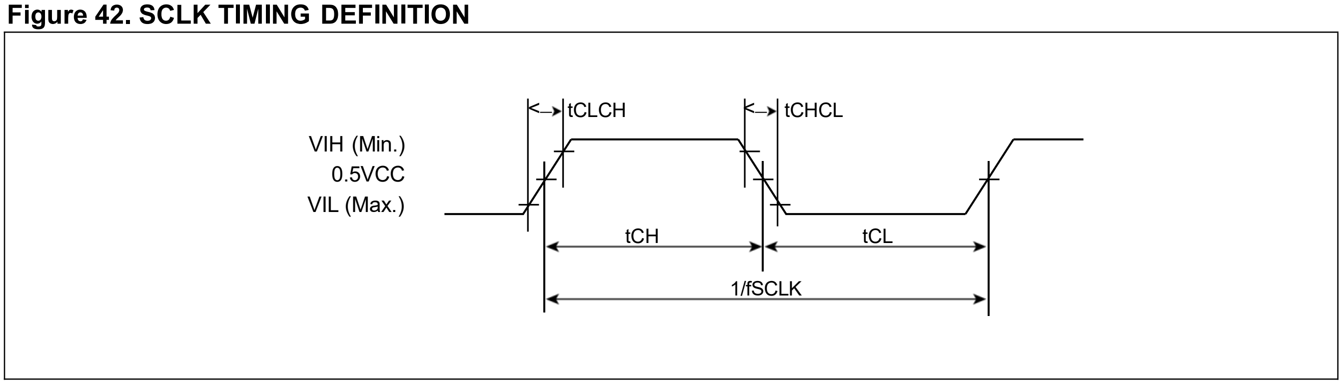


Table 11. DC Characteristics

Temperature = -40°C to 85°C for Industrial grade

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		11	45	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			5	25	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		2.5	5	mA	f=50MHz, SCLK=0.1VCC/0.9VCC, SO=Open
				8	17	mA	fQ=133MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		8	15	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			8	15	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		8	15	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		8	15	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.8	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. The value guaranteed by characterization, not 100% tested in production.

Table 12. AC Characteristics

Temperature = -40°C to 85°C for Industrial grade

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE32K, BE, CE, RES, WREN, WRDI, RDID, RDSR, WRSR		D.C.		133	MHz
fRSCLK	fR	Clock Frequency for READ instructions				50	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions				133	MHz
fTSCLK	fQ	Clock Frequency for 4READ/QREAD instructions				133	MHz
f4PP		Clock Frequency for 4PP (Quad page program)				133	MHz
tCH[(1)]	tCLH	Clock High Time	Others (fSCLK)	45% x (1/fSCLK)			ns
tCH[(1)]	tCLH	Clock High Time	Normal Read (fRSCLK)	9			ns
tCL[(1)]	tCLL	Clock Low Time	Others (fSCLK)	45% x (1/fSCLK)			ns
tCL[(1)]	tCLL	Clock Low Time	Normal Read (fRSCLK)	9			ns
tCLCH [(2)]		Clock Rise Time (peak to peak)		0.1			V/ns
tCHCL [(2)]		Clock Fall Time (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		4			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		4			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		4			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		4			ns
tSHSL	tCSH	CS# Deselect Time	Read	15			ns
tSHSL	tCSH	CS# Deselect Time	Write/Erase/Program	50			ns
tSHQZ [(2)]	tDIS	Output Disable Time	2.65V-3.6V			10	ns
tSHQZ [(2)]	tDIS	Output Disable Time	3.0V-3.6V			8	ns
tHLCH		HOLD# Setup Time (relative to SCLK)		5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)		5			ns
tHHCH		HOLD Setup Time (relative to SCLK)		5			ns
tCHHL		HOLD Hold Time (relative to SCLK)		5			ns
tHHQX	tLZ	HOLD to Output Low-Z Loading=30pF	2.65V-3.6V			10	ns
tHHQX	tLZ	HOLD to Output Low-Z Loading=30pF	3.0V-3.6V			8	ns
tHLQZ	tHZ	HOLD# to Output High-Z Loading=30pF	2.65V-3.6V			10	ns
tHLQZ	tHZ	HOLD# to Output High-Z Loading=30pF	3.0V-3.6V			8	ns
tCLQV	tV	Clock Low to Output Valid VCC=2.65V~3.6V	Loading: 15pF			6	ns
tCLQV	tV	Clock Low to Output Valid VCC=2.65V~3.6V	Loading: 30pF			8	ns
tCLQX	tHO	Output Hold Time		1			ns
tWHSL [(3)]		Write Protect Setup Time		20			ns
tSHWL [(3)]		Write Protect Hold Time		100			ns
tESL[(4)]		Erase Suspend Latency				20	us
tPSL[(4)]		Program Suspend Latency				20	us
tPRS [(5)]		Latency between Program Resume and next Suspend		0.3	100		us
tERS [(6)]		Latency between Erase Resume and next Suspend		0.3	200		us

Table 13. AC Characteristics - continued

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tRCR		Recovery Time from Read	15			us
tRCP		Recovery Time from Program	22			us
tRCE		Recovery Time from Erase	15			ms
tDP		CS# High to Deep Power-down Mode			10	us
tRES1		CS# High to Standby Mode without Electronic Signature Read			95	us
tRES2		CS# High to Standby Mode with Electronic Signature Read			95	us
tW		Write Status Register Cycle Time			40	ms
tBP		Byte-Program		10	50	us
tPP		Page Program Cycle Time		0.33	1.2	ms
tSE		Sector Erase Cycle Time (4KB)		24	200	ms
tBE32K		Block Erase Cycle Time (32KB)		0.15	0.6	s
tBE		Block Erase Cycle Time (64KB)		0.25	1	s
tCE		Chip Erase Cycle Time		12	28	s
tWSR		Write Security Register Time			1	ms

Notes:

1. *tCH + tCL must be greater than or equal to 1/fC.*
2. *The value guaranteed by characterization, not 100% tested in production.*
3. *Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.*
4. *Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".*
5. *For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.*
6. *For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.*

10. TIMING ANALYSIS

Figure 43. Serial Input Timing

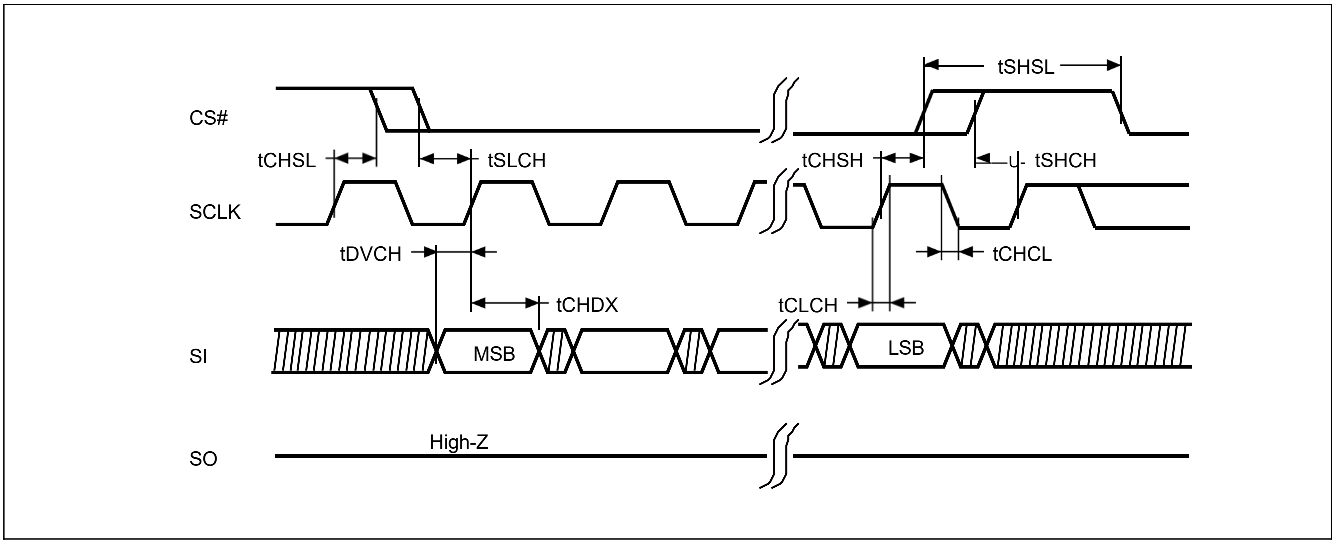


Figure 44. Output Timing

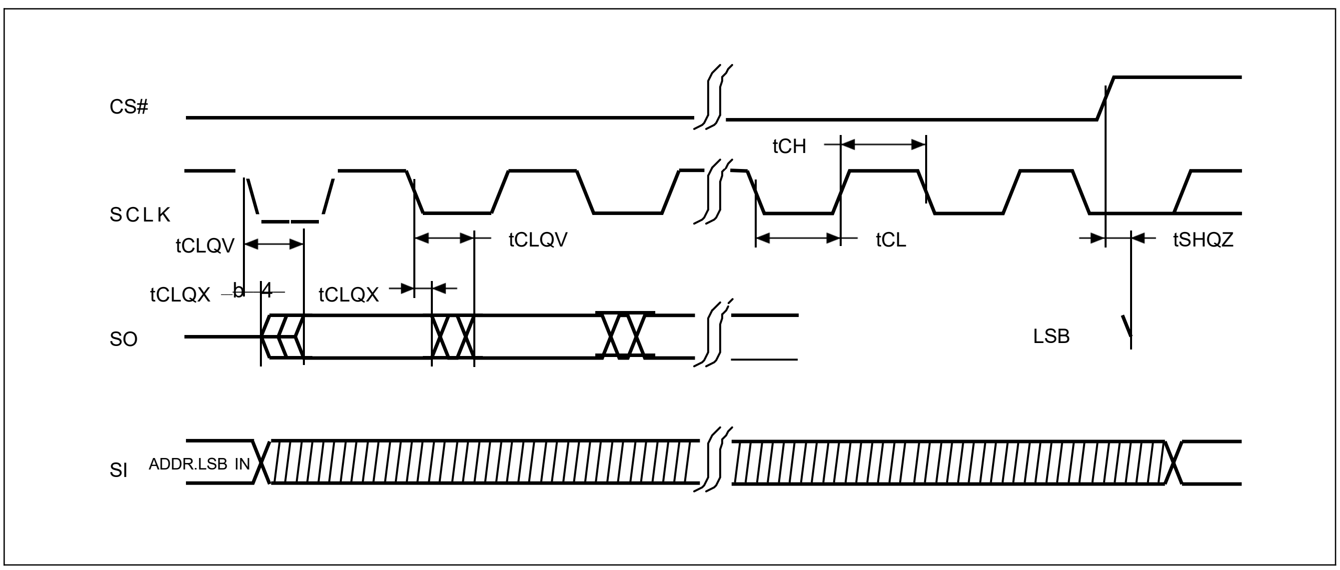


Figure 45. Hold Timing

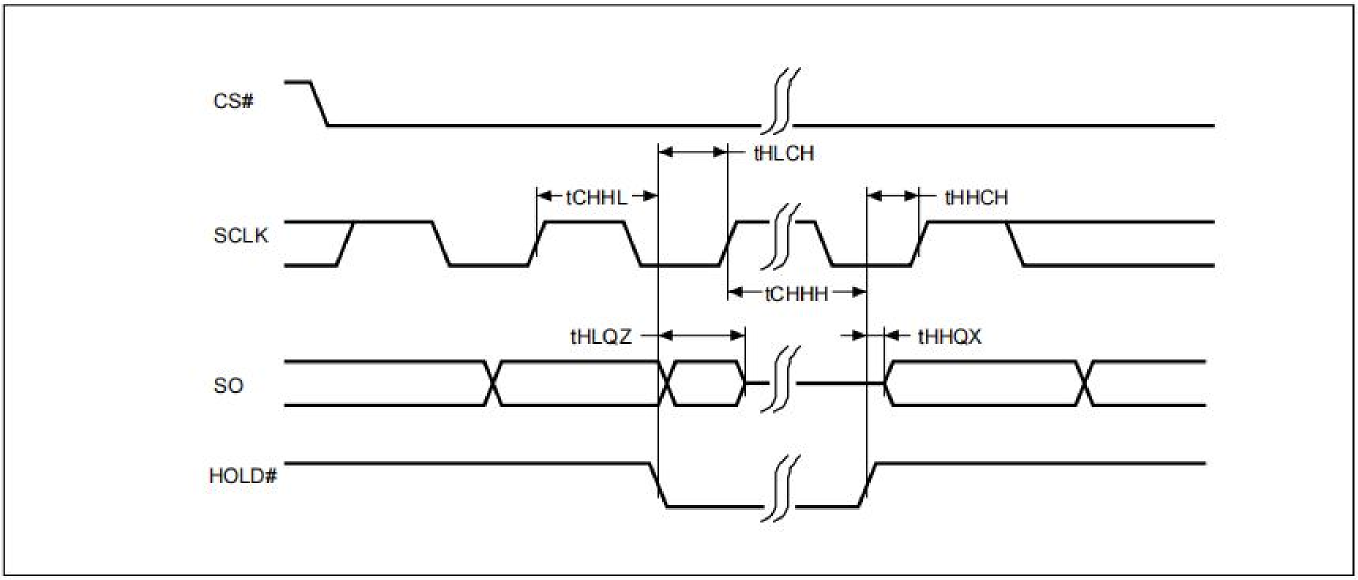
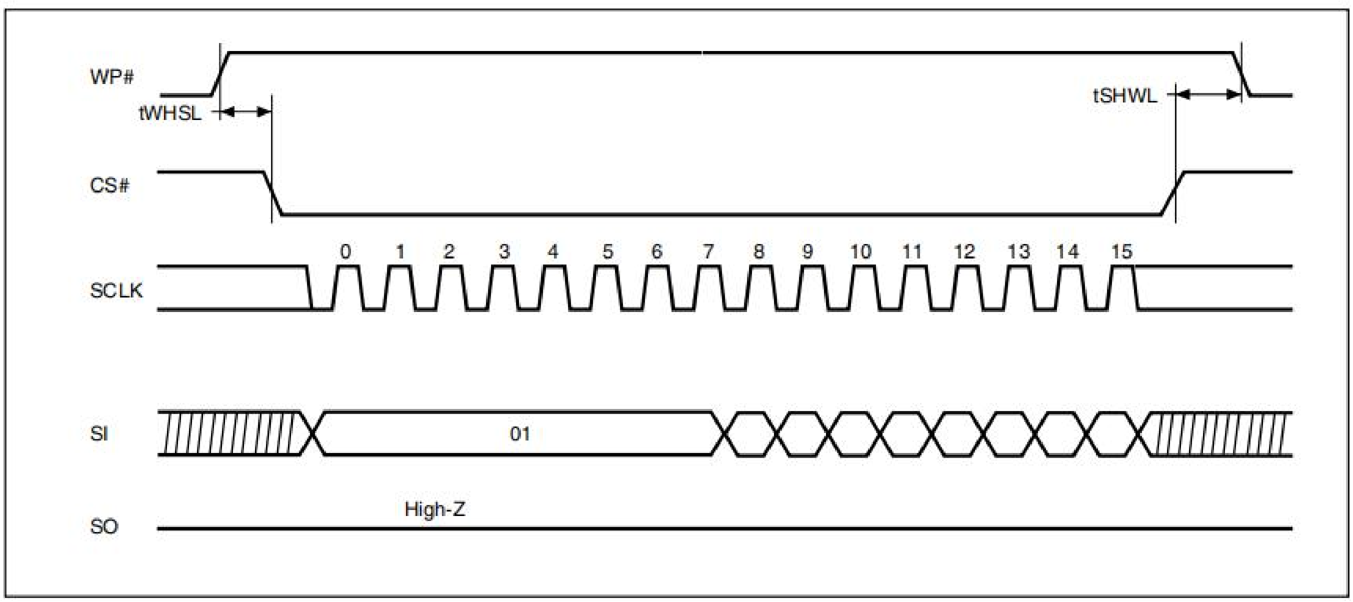


Figure 46. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



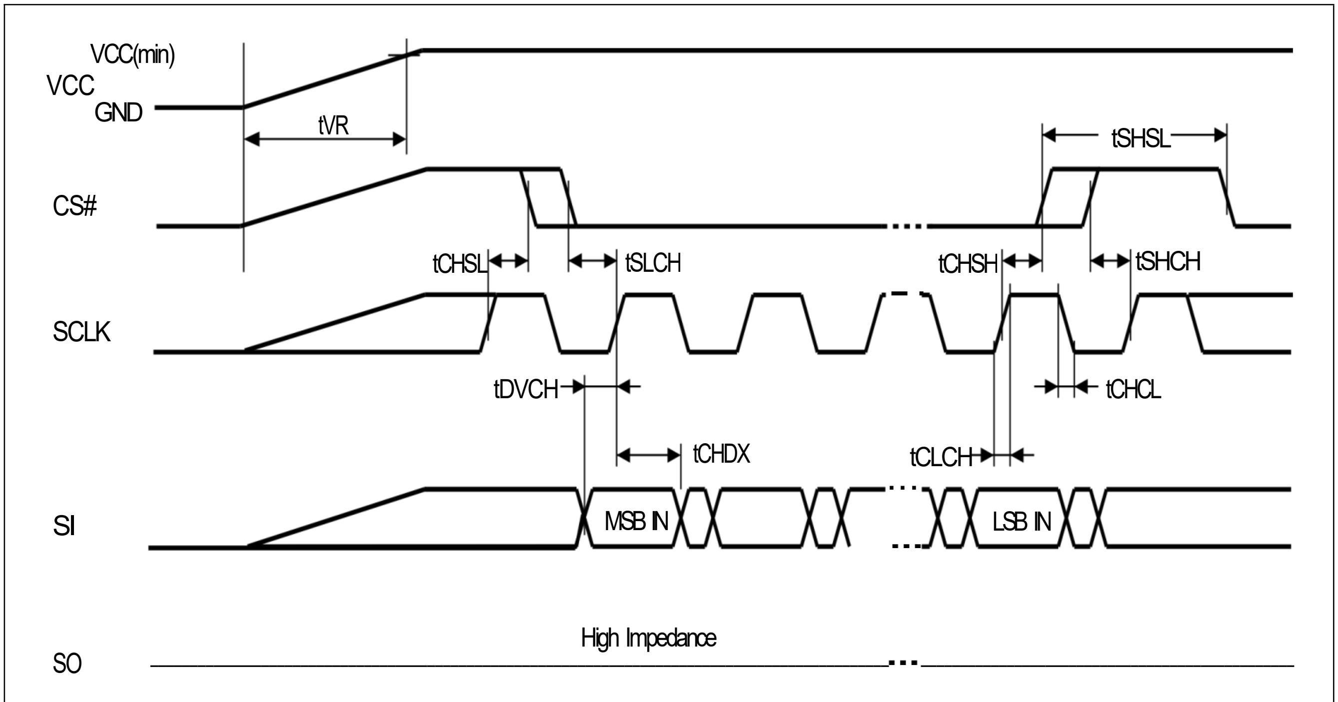
11. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in "Figure 47. AC Timing at Device Power-Up" and "Figure 48. Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 47. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "Table 12. AC Characteristics".

Figure 48. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

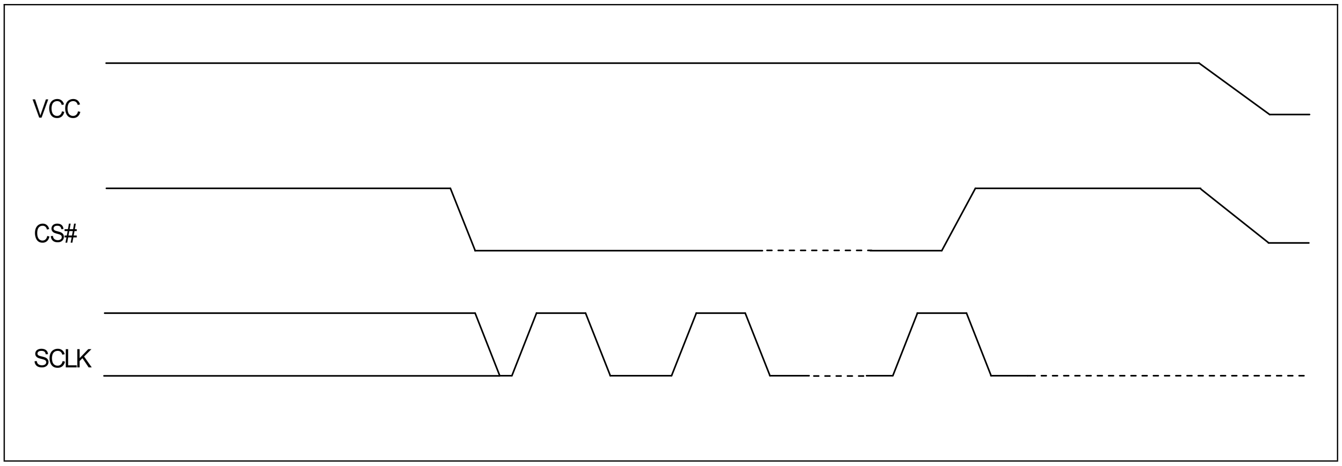


Figure 49. Power-up Timing

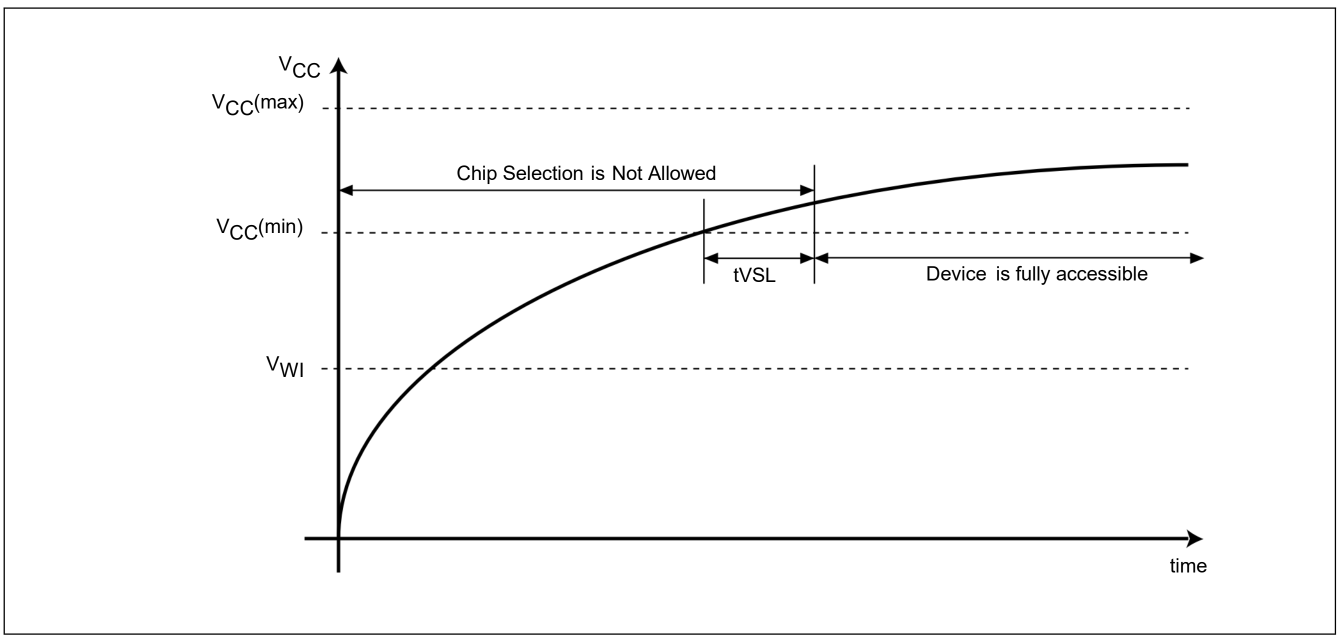


Figure 50. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below V_{PWD} for at least tPWD timing. Please check the table below for more detail.

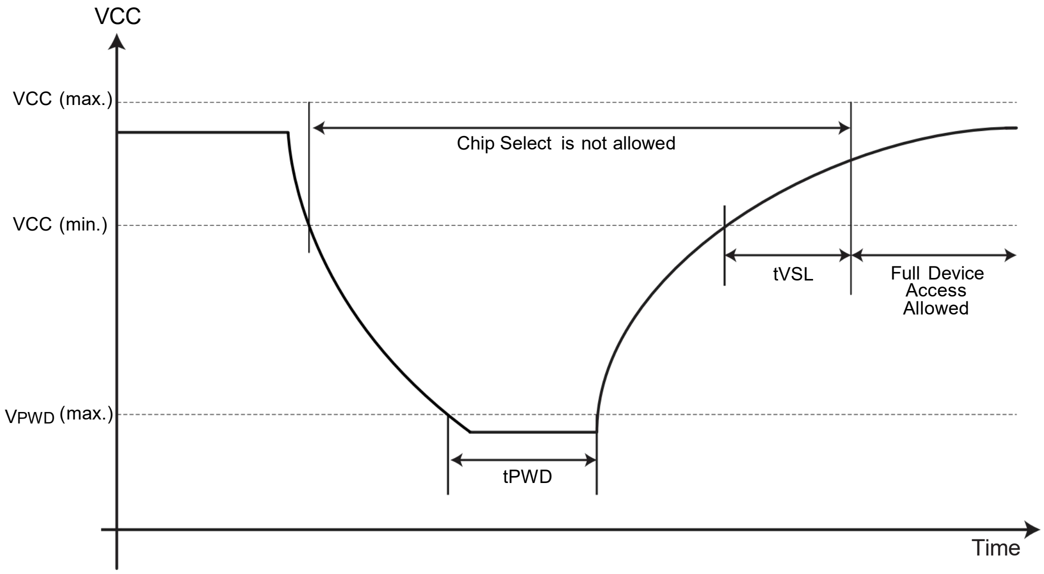


Table 14. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	800		us
VWI	Write Inhibit Voltage	1.5	2.5	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
VCC	VCC Power Supply	2.65	3.6	V

Note: These parameters are characterized only.

Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

12. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ.[(1)]	Max.[(2)]	Unit
Write Status Register Cycle Time		45	ms
Sector Erase Time (4KB)	23	180	ms
Block Erase Time (64KB)	0.25	1	s
Block Erase Time (32KB)	0.14	0.6	s
Chip Erase Time	9	25	s
Byte Program Time (via page program command)	9	45	us
Page Program Time	0.30	1.2	ms
Erase/Program Cycle	100,000		cycles

Notes:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checkerboard pattern.
2. Under worst conditions of 85°C and 2.65V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

13. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

14. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

15.PART NAME DESCRIPTION

NB 25X X X X X X X

Packaging Type
T:Tube
R:Tape & Reel
Y:Tray

Green Code
G: Low-halogen, Lead(Pb)-free
P: Lead (Pb) - free

Temperature Range
E: Extended (-25℃~85℃)
I: Industrial(-40℃~85℃)
J:Industrial Plus (-40℃~105℃)

Package Type
S: 208mil SOP8
T: 150mil SOP8

Version
D: D Version

Device Density
32: 32Mbit

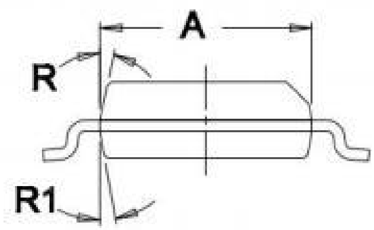
Base Part Number
25Q: Quad SPI Nor Flash

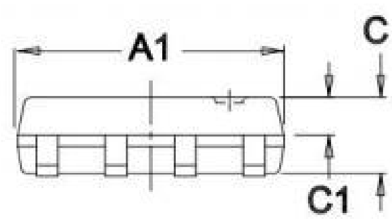
Zetta
Memory

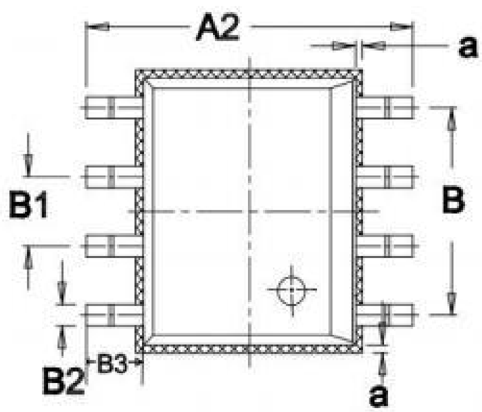
16. PACKAGE INFORMATION

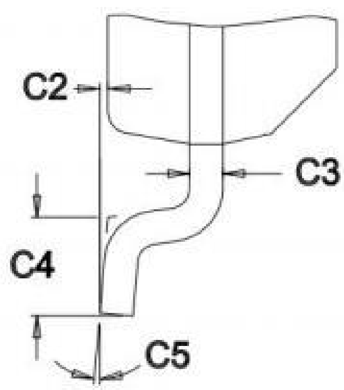
1). 8-pin SOP (150mil)

SYMBOL	min(mm)	nom(mm)	max(mm)	SYMBOL	min(mm)	nom(mm)	max(mm)
A	3.80	3.90	4.00	C	1.35	1.40	1.45
A1	4.80	4.90	5.00	C1	0.67	0.70	0.73
A2	5.80	6.00	6.20	C2	0.00	0.05	0.10
a			0.20	C3	0.17	0.20	0.23
B		3.81		C4	0.40	0.60	0.80
B1		1.27		C5	2°	5°	8°
B2	0.35	0.40	0.48	R		12°	
B3	0.90	1.00	1.20	R1		10°	

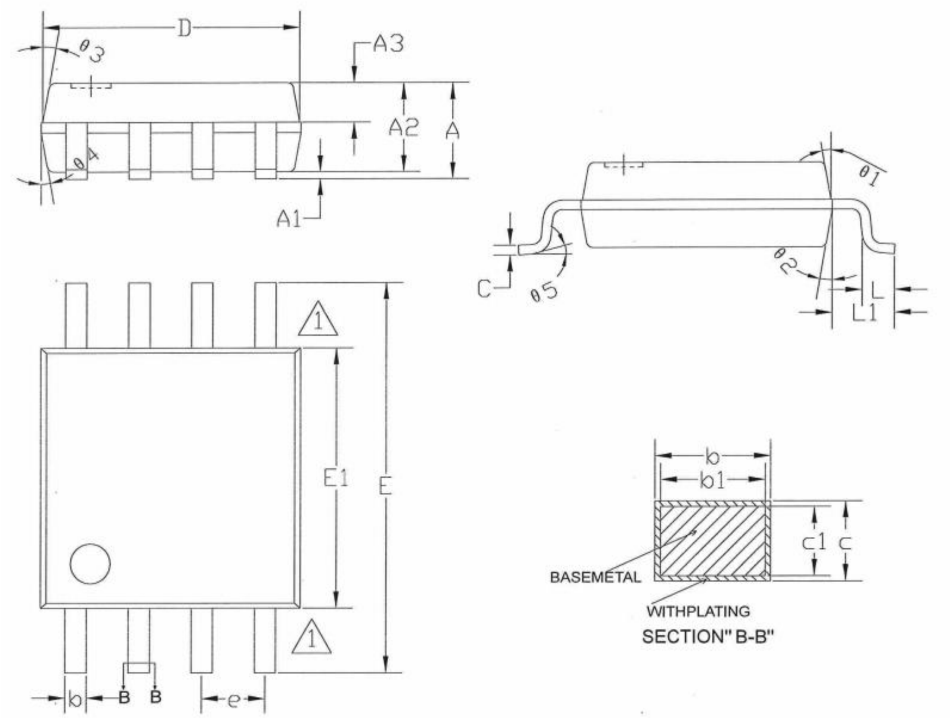








2). 8-pin SOP (208mil)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.95
A1	0.10	0.15	0.18
A2	1.75	1.80	1.90
A3	0.78	0.80	0.82
b	0.33	--	0.47
b1	0.32	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	5.07	5.17	5.27
E	7.70	7.90	8.10
E1	5.17	5.22	5.27
e	1.27(BSC)		
L	0.60	0.65	0.70
L1	1.31(BSC)		
θ1	8°	~	12°
θ2	8°	~	12°
θ3	8°	~	12°
θ4	8°	~	12°
θ5	0°	~	6°

17. REVISION HISTORY

Version No	Description	Date
1.0	Initial Release	2024-12-17
1.1	Add package information	2025-01-11