



# XZP821 Datasheet

10/100/1000M/2.5G ETHERNET TRANSCEIVER

VERSION V1.01

DATE 2023-08-08

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## Revision History

| Revision | Release Date | Summary                                                                                                  |
|----------|--------------|----------------------------------------------------------------------------------------------------------|
| V1.00    | 2023/03/08   | First version.                                                                                           |
| V1.01    | 2023/08/08   | Description Modification in Register 4.1.5,4.2.7,4.2.9,4.2.17,4.2.19;<br>Update power consumption table. |

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# 1. Overview

The XZP821 is a 10BASE-Te, 100BASE-TX, 1000BASE-T and 2.5GBASE-T transceiver highly integrated into a single monolithic CMOS chip, and is compatible with both the IEEE 802.3 standard and the NBASE-T Alliance PHY . It performs all the necessary physical layer functions for 10BASE-Te, 100BASE-TX, 1000BASE-T and 2.5GBASE-T ethernet over CAT.5e UTP cable.

The XZP821 uses advanced DSP technology and an Analog Front End to enable high-speed data transmission and reception over UTP cable. It is a highly integrated solution combining digital adaptive equalizers, ADCs, line driver, echo cancellers, crosstalk cancellers, phase-locked loops and so on. Functions such as Crossover Detection & Auto-Correction, polarity correction are also supported.

Data transfer between MAC and XZP821 is by the SERDES interface which can be configured as SGMII and 2500BASE-X. XZP821 operates at multiple digital I/O voltages, including 3.3V and 1.8V.

## 1.1. Features

- Compatible with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.3az (Energy Efficient Ethernet)
- Supports IEEE 802.3bz(2.5GBASE-T)
- Supports Full Duplex flow control (IEEE 802.3x)
- Supports IEEE 802.3 optional ability(Fast Retrain)
- Integrated 10BASE-Te, 100BASE-TX, 1000BASE-T and 2.5GBASE-T IEEE 802.3 Compliant transceiver
- Auto-Negotiation with extended next page capability(XNP)
- Compatible with NBASE-T Alliance PHY Specification
- Supports pair swap/polarity/skew correction
- Crossover detection and auto-correction
- Configurable MDI port ordering(MDI swap) for easy PCB layout
- Supports power down/link down power saving mode
- Supports clause 22 and clause 45 MDC/MDIO management interface
- Supports rate adaptor for SERDES
- Selectable SERDES interface to MAC control(SGMII /2500BASE-X)
- Built-in Wake-on-LAN(WOL) over UTP
- Supports Interrupt function over UTP
- Supports parallel detection
- Baseline Wander Correction
- Supports 3.3/1.8V signaling for MDIO access
- Supports 25MHz crystal or external OSC

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- Provides 25MHz clock source for MAC
- Provides 3 network customized LEDs with controllable LED Blinking Frequency and Duty Cycle
- Self-Loopback diagnostic capability
- Supports SPI Flash

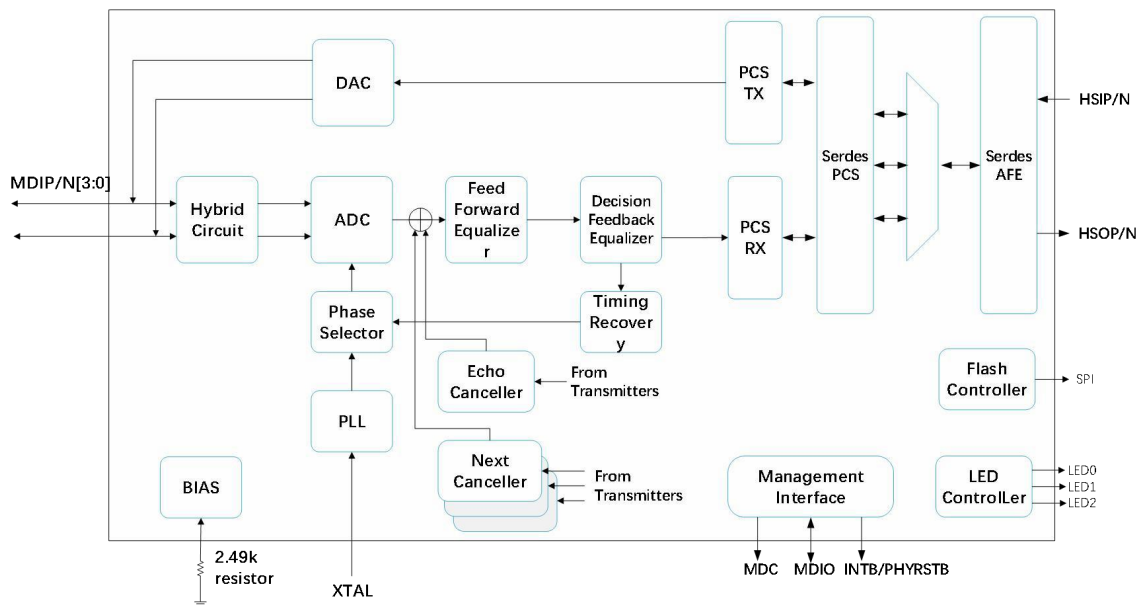


Figure 1. Block Diagram

## 1.2. Target Applications

- Ethernet Switch
- DTV (Digital TV)
- Communication and Network Riser
- Routers, PON Equipment
- Printer and Office Machine
- MAU(Media Access Unit)

## 2. Pin Assignment

### 2.1. XZP821 QFN48

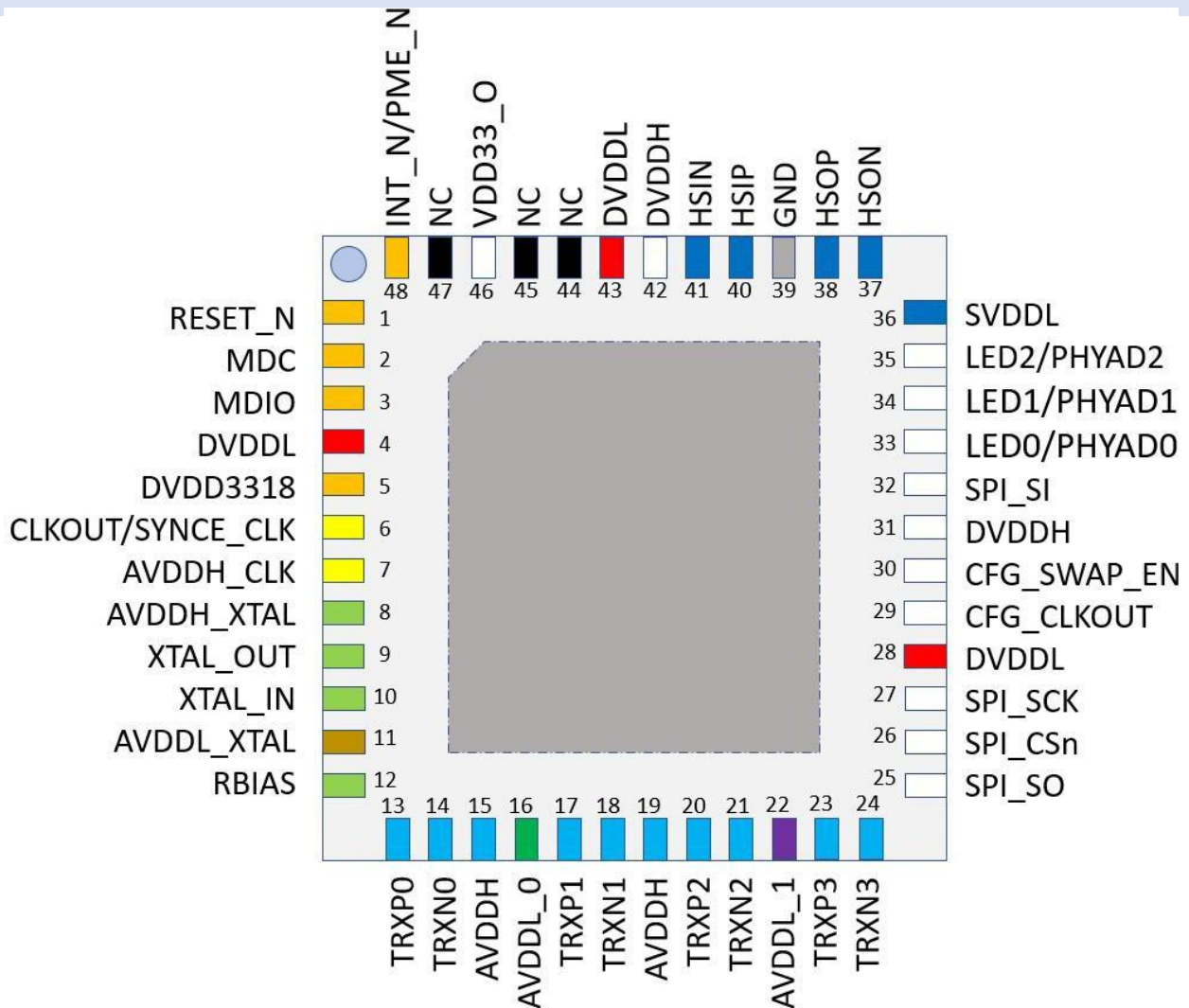


Figure 2. Pin Map

### 2.2. Pin Descriptions

- I: Input Pin
- AI: Analog Input Pin
- O: Output Pin
- AO: Analog Output Pin
- IO: Bidirectional Input/Output Pin
- AIO: Analog Bidirectional Input/Output Pin
- LI: Latched Input During Power UP or Hardware Reset

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- P: Digital Power Pin
- AP: Analog Power Pin
- G: Digital Ground Pin
- AG: Analog Ground Pin
- PD: Internal Pull-Down
- PU: Internal Pull-UP
- SP: SerDes Power Pin
- SG: SerDes Ground Pin
- OD: Open Drain
- XT: Crystal Related

## XZP821 Datasheet

- 2.2.1. ALL pins

Table 1. All Pins Assignment

| No. | Pin Name         | Type  | No. | Pin Name            | Type    |
|-----|------------------|-------|-----|---------------------|---------|
| 1   | RESET_N          | I/PU  | 26  | SPI_CS <sub>n</sub> | O       |
| 2   | MDC              | I/PD  | 27  | SPI_SCK             | O       |
| 3   | MDIO             | IO/PU | 28  | DVDDL               | P       |
| 4   | DVDDL            | P     | 29  | CFG_CLKOUT          | LI/PD   |
| 5   | DVDD3318         | P     | 30  | CFG_SWAP_EN         | LI/PD   |
| 6   | CLKOUT/SYNCE_CLK | O     | 31  | DVDDH               | P       |
| 7   | AVDDH_CLK        | AP    | 32  | SPI_SI              | O       |
| 8   | AVDDH_XTAL       | AP    | 33  | LED0/PHYAD0         | O/LI/PU |
| 9   | XTAL_OUT         | XT    | 34  | LED1/PHYAD1         | O/LI/PD |
| 10  | XTAL_IN          | XT    | 35  | LED2/PHYAD2         | O/LI/PD |
| 11  | AVDDL_XTAL       | AP    | 36  | SVDDL               | AP      |
| 12  | RBIAS            | AO    | 37  | HS <sub>ON</sub>    | AO      |
| 13  | TRXP0            | AIO   | 38  | HS <sub>OP</sub>    | AO      |
| 14  | TRXN0            | AIO   | 39  | GND                 | G       |
| 15  | AVDDH            | AP    | 40  | HS <sub>IP</sub>    | AI      |
| 16  | AVDDL_0          | AP    | 41  | HS <sub>IN</sub>    | AI      |
| 17  | TRXP1            | AIO   | 42  | DVDDH               | P       |
| 18  | TRXN1            | AIO   | 43  | DVDDL               | P       |
| 19  | AVDDH            | AP    | 44  | NC                  |         |
| 20  | TRXP2            | AIO   | 45  | NC                  |         |
| 21  | TRXN2            | AIO   | 46  | VDD33_O             | O/P     |
| 22  | AVDDL_1          | AP    | 47  | NC                  |         |
| 23  | TRXP3            | AIO   | 48  | INT_N/PME_N         | O       |
| 24  | TRXN3            | AIO   | 49  | GND                 | G       |
| 25  | SPI_SO           | I     |     |                     |         |

## XZP821 Datasheet

- 2.2.2. Transceiver Interface Pins

Table 2. Transceiver Interface

| Pin Name | Pin No. | Type | Description                                    |
|----------|---------|------|------------------------------------------------|
| TRXP0    | 13      | AIO  | Media-dependent pair 0, 100Ω transmission line |
| TRXN0    | 14      | AIO  |                                                |
| TRXP1    | 17      | AIO  | Media-dependent pair 1, 100Ω transmission line |
| TRXN1    | 18      | AIO  |                                                |
| TRXP2    | 20      | AIO  | Media-dependent pair 2, 100Ω transmission line |
| TRXN2    | 21      | AIO  |                                                |
| TRXP3    | 23      | AIO  | Media-dependent pair 3, 100Ω transmission line |
| TRXN3    | 24      | AIO  |                                                |

---

- 2.2.3. SERDES Interface Pins

Table 3. SERDES Interface Pins

| Pin Name | Pin No. | Type | Description                                                                                                                                                                                                                                                                                           |
|----------|---------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HSOP     | 38      | AO   | SERDES Differential Output, transfer data to an external device. The SERDES baud rate should be set by MAC via register before usage.<br>SGMII : supports 10M/100M/1G ethernet speed<br>2500BASE-X: supports 2.5G ethernet speed<br>Differential pairs have an internal 100ohm termination resistor.  |
| HSOIN    | 37      | AO   |                                                                                                                                                                                                                                                                                                       |
| HSIP     | 40      | AI   | SERDES Differential Input, receiver data from an external device. The SERDES baud rate should be set by MAC via register before usage.<br>SGMII : supports 10M/100M/1G ethernet speed<br>2500BASE-X: supports 2.5G ethernet speed<br>Differential pairs have an internal 100ohm termination resistor. |
| HSIN     | 41      | AI   |                                                                                                                                                                                                                                                                                                       |

---

- 2.2.4. Configuration Pins

Table 4. Configuration Pins

| Pin Name          | Pin No. | Type    | Description                                                                                                                                        |
|-------------------|---------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| LED0/<br>PHYADDR0 | 33      | LI/O/PU | PHYADDR0, PHY Address Select. After power-up or reset its function is LED0 indicator.<br>Note: This pin must be pulled high or low via an external |

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|                   |    |         |                                                                                                                                                                                              |
|-------------------|----|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                   |    |         | 4.7k ohm resistor upon power on or reset.                                                                                                                                                    |
| LED1/<br>PHYADDR1 | 34 | LI/O/PD | PHYADDR1, PHY Address Select. After power-up or reset its function is LED1 indicator.<br>Note: This pin must be pulled high or low via an external 4.7k ohm resistor upon power on or reset. |
| LED2/<br>PHYADDR2 | 35 | LI/O/PD | PHYADDR2, PHY Address Select. After power-up or reset its function is LED2 indicator.<br>Note: This pin must be pulled high or low via an external 4.7k ohm resistor upon power on or reset. |
| CFG_SWAP_EN       | 30 | LI//PD  | MDI swap Pullup:<br>MDI pair3-pair0 mapping to RJ45_pair0~RJ45_pair3<br>Pulldown:<br>MDI pair0-pair3 mapping to RJ45_pair0~RJ45_pair3                                                        |
| CFG_CLKOUT        | 29 | LI/PD   | Clock out<br>Pullup: 25MHz clock out in CLKOUT pin<br>Pulldown: clock out disable                                                                                                            |

### • 2.2.5. Miscellaneous Pins

Table 5. Miscellaneous Pins

| Pin Name    | Pin No. | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------|---------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDC         | 2       | I/PD  | MII Management Interface Clock Input.<br>The clock reference for the MII management interface.<br>The maximum frequency support is 12.5MHz.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| MDIO        | 3       | IO/PU | MII Management Interface Data Input/Output.<br>MDIO transfer management data in and out of the device synchronous to the rising edge of MDC.                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| INT_N/PME_N | 48      | OD/PU | This pin is shared by two functions, the default pin setting is INT_N. Keep this pin floating if either of the functions is not used. The pin type depends on function selected:<br>1. Interrupt (should be DVDD3318 pulled up).<br>Set low if the specified events occurred; active low.<br>2. Power Management Event (should be DVDD3318 pulled up). Set low if received a magic packet; active low.<br>Note 1: The behavior of INT_N is level-triggered, the behavior of PME_N is level-triggered or pulse-triggered which is controlled by register.<br>Note 2: The function of INT_N/PME_N can be assigned |

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|                      |    |      |                                                                                                                                                                                                                                                                                                                                                  |
|----------------------|----|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                      |    |      | by register.                                                                                                                                                                                                                                                                                                                                     |
| RESET_N              | 1  | I/PU | Hardware Reset (Active Low Reset Signal).<br>To complete the reset function, this pin must be asserted for at least 10ms. It must be pulled high for normal operation.                                                                                                                                                                           |
| RBIAS                | 12 | AO   | Bias Resistor.<br>An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND                                                                                                                                                                                                                                                |
| XTAL_IN              | 10 | XT   | 25MHz Crystal Clock Input.<br>25MHz ± 50ppm tolerance crystal reference or oscillator input.<br>When using a crystal, connect a loading capacitor from each pad to ground.<br>When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating.<br>The maximum XTALI input voltage is 3.3V. |
| XTAL_OUT             | 9  | XT   | 25Mhz Crystal Clock Output.<br>25MHz±50ppm tolerance crystal output. Refer to XTALI.                                                                                                                                                                                                                                                             |
| CLKOUT/<br>SYNCE_CLK | 6  | O    | 25MHz clock output or SYNCE clock output<br>Keep this pin floating if do not use this clock                                                                                                                                                                                                                                                      |
| VDD33_O              | 46 | O/P  | Always output 3.3 power.<br>Keep this pin floating if do not use<br>Driving current <1mA, only use to external 0.95V SWR enable                                                                                                                                                                                                                  |

### • 2.2.6. SPI Interface Pins

Table 6. SPI Pins

| Pin Name | Pin No. | Type | Description                                 |
|----------|---------|------|---------------------------------------------|
| SPI_CSn  | 26      | O    | SPI Flash Chip Select                       |
| SPI_SCK  | 27      | O    | SPI Flash serial data clock                 |
| SPI_SO   | 25      | I    | Input from SPI Flash serial data output pin |
| SPI_SI   | 32      | O    | Output to SPI Flash serial data input pin   |

## XZP821 Datasheet

- 2.2.7. Power and GND Pins

Table 7. Power and GND Pins

| Pin Name   | Pin No.      | Type | Description                                |
|------------|--------------|------|--------------------------------------------|
| AVDDH      | 15,19        | AP   | Analog High Voltage Input Power            |
| AVDDL_XTAL | 11           | AP   | Xtal Low Voltage Input Power               |
| AVDDL_0    | 16           | AP   | Analog Low Voltage Input Power 0           |
| AVDDL_1    | 22           | AP   | Analog Low Voltage Input Power 1           |
| SVDDL      | 36           | SP   | SerDes Low Voltage Input Power             |
| DVDDH      | 31,42        | P    | Digital High Voltage Input Power           |
| DVDDL      | 4,28,43      | P    | Digital Low Voltage Input Power            |
| DVDD3318   | 5            | P    | Input Power, IO Power for RESET_N/MDC/MDIO |
| AVDDH_XTAL | 8            | AP   | Xtal High Voltage Input Power              |
| AVDDH_CLK  | 7            | AP   | SYNCE clock Input Power                    |
| GND        | 39,<br>EPAD  | G    | Ground                                     |
| NC         | 44,45,4<br>7 |      | Keep this pin floating                     |

## 3. Operational Description

### 3.1. Reset

XZP821 have a hardware reset pin(RESET\_N) which is low active. RESET\_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET\_N is also used for power on strapping. During RESET\_N is active, XZP821 latches input value on strapping. Strapping is used as configuration information which provides flexibility in application without mdio access.

Table 8. Reset Timing Characteristics

| Symbol | Description                                                         | Min | Typ | Max | Units |
|--------|---------------------------------------------------------------------|-----|-----|-----|-------|
| T1     | The duration from all powers steady to reset signal release to high | 10  | –   | –   | ms    |
| T2     | The duration of reset signal remain low timing                      | 10  | –   | –   | ms    |

\*\* NOTE: If the T2 meets the requirement, the T1 is not required.

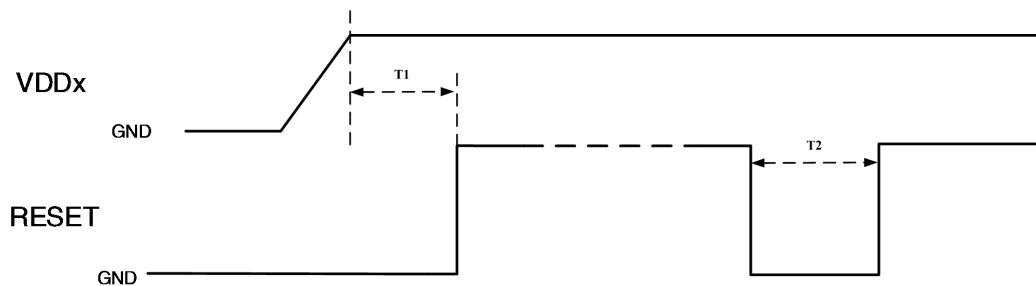


Figure 3. Reset Timing Diagram

### 3.2. PHY Address

For XZP821, Strapping PHYADDR[2:0] is used to generate phy address.

XZP821 always responses to phy address 0. It can be disabled by configure bit[6] to 1'b0 of common register EXT\_0xA005. It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of common register EXT\_0xA005 is broadcast phy address and its default value is 5  $\Rightarrow$  b11111. Bit[5] of common register EXT\_0xA005 is enable control for broadcast phy address and its default value is 1  $\Rightarrow$  b0.

### 3.3. Mode Configuration

The chip mode of XZP821 can be configed by registers 0xa001[2:0].

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| Operating Mode                                | Serdes Mode | UTP Speed  |
|-----------------------------------------------|-------------|------------|
| AUTO_BX2500_SG<br>MII 0xa001[2:0] = 3<br>b000 | 2500BASE-X  | 2500BASE-T |
|                                               | SG<br>MII   | 1000BAST-T |
|                                               |             | 100BASE-T  |
|                                               |             | 10BASE-Te  |
| FORCE_BX250<br>0 0xa001[2:0] = 3<br>b001      | 2500BASE-X  | 2500BASE-T |
|                                               |             | 1000BAST-T |
|                                               |             | 100BASE-T  |
|                                               |             | 10BASE-Te  |
| UTP_TO_FIBER_FORCE<br>0xa001[2:0] = 3 b101**  | 2500BASE-X  | 2500BASE-T |
|                                               | 1000BASE-X  | 1000BASE-T |
|                                               | 100BASE-FX  | 100BASE-T  |

**Table 9. Mode selection**

\*\* UTP\_TO\_FIBER\_FORCE Mode should manually set other registers at different fiber speed, reference to application note.

### 3.4. Sync-E Clock Output

XZP821 provides Synchronous Ethernet (Sync-E) clock output. Sync-E clock can output from CLKOUT/ SYNCE\_CLK (pin 6). The Sync-E clock sources can be configured to recovery from Serdes or UTP respectively.

### 3.5. Interrupt

XZP821 has a interrupt pin. INT\_N/PME\_N is shared by two functions, the default pin setting is INT\_N. Keep this pin floating if neither of the functions is used.

The pin type depends on function selected:

- 1. Interrupt (should be DVDD3318 pulled up). Set low if the specified events occurred; active low.
- 2. Power Management Event (should be DVDD3318 pulled up). Set low if received a magic packet; active low.

Note 1: The behavior of INT\_N is level-triggered, the behavior of PME\_N is level-triggered or pulse-triggered which is controled by register.

Note 2: The function of INT\_N/PME\_N can be assigned by common ext register 0xa00a bit6.

### 3.6. LED

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. They can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the register interface.

### 3.7. Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22/45 and XZP821 also support MDC clock rates up to 12.5 MHz.

## 4. Register Overview

Table 10. Register Access Types

| Type | Description                                                                                                                                                                                              |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RW   | Read and write                                                                                                                                                                                           |
| SC   | Self-clear.<br>If default value is '0' ('1'), writing a '1' ('0') to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0' ('1'). |
| RO   | Read only.                                                                                                                                                                                               |
| LH   | Latch high.                                                                                                                                                                                              |
| LL   | Latch Low.                                                                                                                                                                                               |
| RC   | Read clear.                                                                                                                                                                                              |
| SWC  | Software reset to 0.                                                                                                                                                                                     |
| SWS  | Software reset to 1.                                                                                                                                                                                     |
| POS  | Default value depends on power on strapping.                                                                                                                                                             |

### 4.1. Phy MII Register

#### • 4.1.1 Basic control register (0x00)

Table 11. Basic control register (0x00)

| Bit | Symbol               | Access | Default | Description                                                                                                                                                                                                                                                  |
|-----|----------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | Reset                | RW SC  | 0x0     | PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.<br>0: Normal operation<br>1: PHY reset                                                                                  |
| 14  | Loopback             | RW SWC | 0x0     | Internal loopback control<br>1  b0: disable loopback<br>1  b1: enable loopback                                                                                                                                                                             |
| 13  | Speed_Selection(LSB) | RW     | 0x0     | LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.<br>Bit6 bit13 |

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|     |                      |                     |     |                                                                                                                                                                                                                                                                         |
|-----|----------------------|---------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                      |                     |     | <p>1 1 = speed is determined by MMD1 0x0 bits 5:2</p> <p>1 0 = 1000Mb/s</p> <p>0 1 = 100Mb/s</p> <p>0 0 = 10Mb/s</p>                                                                                                                                                    |
| 12  | Autoneg_En           | RW                  | 0x1 | <p>1: to enable auto-negotiation;</p> <p>0: auto-negotiation is disabled.</p>                                                                                                                                                                                           |
| 11  | Power_down           | RW<br>SWC           | 0x0 | <p>1 = Power down</p> <p>0 = Normal operation</p> <p>When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.</p>               |
| 10  | Isolate              | RW<br>SWC           | 0x0 | <p>Isolate phy from RGMII/SGMII/FIBER.</p> <p>1 = b0: Normal mode</p> <p>1 = b1: Isolate mode</p>                                                                                                                                                                       |
| 9   | Re_Autoneg           | RW<br><br>SC<br>SWC | 0x0 | <p>Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART.</p> <p>1 = Restart Auto-Negotiation Process</p> <p>0 = Normal operation</p>                                                                                   |
| 8   | Duplex_Mode          | RW                  | 0x1 | <p>The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.</p> <p>1 = Full Duplex</p> <p>0 = Half Duplex</p> |
| 7   | Collision_Test       | RW<br>SWC           | 0x0 | <p>Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.</p> <p>1 = Enable COL signal test</p> <p>0 = Disable COL signal test</p>                                                                                                  |
| 6   | Speed_Selection(MSB) | RW                  | 0x1 | See bit13.                                                                                                                                                                                                                                                              |
| 5:0 | Reserved             | RO                  | 0x0 | Reserved. Write as 0, ignore on read                                                                                                                                                                                                                                    |

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### • 4.1.2. Basic status register (0x01)

Table 12. Basic status register (0x01)

| Bit | Symbol                  | Access       | Default | Description                                                                                                                                                                                                                            |
|-----|-------------------------|--------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | 100Base-T4              | RO           | 0x0     | PHY doesn't support 100BASE-T4                                                                                                                                                                                                         |
| 14  | 100Base-X_Fd            | RO           | 0x1     | PHY supports 100BASE-X_FD                                                                                                                                                                                                              |
| 13  | 100Base-X_Hd            | RO           | 0x1     | PHY supports 100BASE-X_HD                                                                                                                                                                                                              |
| 12  | 10Mbps_Fd               | RO           | 0x1     | PHY supports 10Mbps_Fd                                                                                                                                                                                                                 |
| 11  | 10Mbps_Hd               | RO           | 0x1     | PHY supports 10Mbps_Hd                                                                                                                                                                                                                 |
| 10  | 100Base-T2_Fd           | RO           | 0x0     | PHY doesn't support 100Base-T2_Fd                                                                                                                                                                                                      |
| 9   | 100Base-T2_Hd           | RO           | 0x0     | PHY doesn't support 100Base-T2_Hd                                                                                                                                                                                                      |
| 8   | Extended_Status         | RO           | 0x1     | Whether support EXTended status register in 0Fh<br>0: Not supported<br>1: Supported                                                                                                                                                    |
| 7   | Unidirect_Ability       | RO           | 0x0     | 1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established<br>1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established |
| 6   | Mf_Preamble_Suppression | RO           | 0x1     | 1'b0: PHY will not accept management frames with preamble suppressed<br>1'b1: PHY will accept management frames with preamble suppressed                                                                                               |
| 5   | Autoneg_Complete        | RO SWC       | 0x0     | 1'b0: Auto-negotiation process not completed<br>1'b1: Auto-negotiation process completed                                                                                                                                               |
| 4   | Remote_Fault            | RO RC SWC LH | 0x0     | 1'b0: no remote fault condition detected<br>1'b1: remote fault condition detected                                                                                                                                                      |
| 3   | Autoneg_Ability         | RO           | 0x1     | 1'b0: PHY not able to perform Auto-negotiation<br>1'b1: PHY able to perform Auto-negotiation                                                                                                                                           |
| 2   | Link_Status             | RO SWC LL    | 0x0     | Link status<br>1'b0: Link is down<br>1'b1: Link is up                                                                                                                                                                                  |
| 1   | Jabber_Detect           | RO RC SWC LH | 0x0     | 10Baset jabber detected. It would assert if TX activity lasts longer than 42ms.<br>1'b0: no jabber condition detected                                                                                                                  |

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|   |                     |    |     |                                                                                                                                                     |
|---|---------------------|----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------|
|   |                     |    |     | 1'b1: Jabber condition detected.                                                                                                                    |
| 0 | Extended_Capability | RO | 0x1 | To indicate whether support Extended registers, to access from address register 1Eh and data register 1Fh<br>1'b0: Not supported<br>1'b1: Supported |

### • 4.1.3. PHY identification register1 (0x02)

Table 13. PHY identification register1 (0x02)

| Bit  | Symbol | Access | Default | Description |
|------|--------|--------|---------|-------------|
| 15:0 | Phy_Id | RO     | None    | None        |

### • 4.1.4. PHY identification register2 (0x03)

Table 14. PHY identification register2 (0x03)

| Bit   | Symbol      | Access | Default | Description |
|-------|-------------|--------|---------|-------------|
| 15:10 | Phy_Id      | RO     | None    | None        |
| 9:4   | Type_No     | RO     | None    | None        |
| 3:0   | Revision_No | RO     | None    | None        |

### • 4.1.5. Auto-Negotiation advertisement (0x04)

Table 15. Auto-Negotiation advertisement (0x04)

| Bit | Symbol    | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-----------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | NEXT_Page | RW     | 0x0     | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>If 1000BASE-T is advertised, the required</p> |

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|    |                    |    |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----|--------------------|----|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                    |    |     | <p>next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed.</p> <p>1 = Advertise<br/>0 = Not advertised</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 14 | Ack                | RO | 0x0 | Always 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 13 | Remote_Fault       | RW | 0x0 | <p>1 = Set Remote Fault bit<br/>0 = Do not set Remote Fault bit</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 12 | Extended_NEXT_Page | RW | 0x1 | <p>Extended next page enable control bit<br/>1 = Local device supports transmission of extended next pages<br/>0 = Local device does not support transmission of extended next pages.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 11 | Asymmetric_Pause   | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>1 = Asymmetric Pause<br/>0 = No asymmetric Pause</p>                                                                                               |
| 10 | Pause              | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> |

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|   |                                    |    |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---|------------------------------------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|   |                                    |    |     | 1 = MAC PAUSE implemented<br>0 = MAC PAUSE not implemented                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 9 | 100BASE-T4                         | RO | 0x0 | always 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 8 | 100BASE-TX_Full_Duplex             | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down 1 = Advertise<br/>0 = Not advertised</li> </ul>                                                                                                                                                       |
| 7 | 100BASE-TX_Half_Duplex             | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down 1 = Advertise<br/>0 = Not advertised</li> </ul> |
| 6 | 10BASE-T <sub>e</sub> _Full_Duplex | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> </ul>                                                                                                                                                                                                                                                                                                                          |

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|     |                           |    |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|---------------------------|----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                           |    |     | <ul style="list-style-type: none"> <li>The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>Link goes down 1 = Advertise<br/>0 = Not advertised</li> </ul>                                                                                                                                                                                                                                                                                                         |
| 5   | 10BASE-<br>Te_Half_Duplex | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>Software reset is asserted by writing register 0x0 bit[15]</li> <li>Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>Link goes down 1 = Advertise<br/>0 = Not advertised</li> </ul> |
| 4:0 | Selector_Field            | RW | 0x1 | Selector Field mode.<br>00001 = IEEE 802.3                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

### 4.1.6. Auto-Negotiation link partner ability (0x05)

Table 16. Auto-Negotiation link partner ability (0x05)

| Bit | Symbol        | Access    | Default | Description                                                                                                                                |
|-----|---------------|-----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | 1000Base-X_Fd | RO<br>SWC | 0x0     | Received Code Word Bit 15<br>1 = Link partner is capable of next page<br>0 = Link partner is not capable of next page                      |
| 14  | ACK           | RO<br>SWC | 0x0     | Acknowledge. Received Code Word Bit 14<br>1 = Link partner has received link code word<br>0 = Link partner has not received link code word |
| 13  | REMOTE_FAULT  | RO<br>SWC | 0x0     | Remote Fault. Received Code Word Bit 13<br>1 = Link partner has detected remote fault<br>0 = Link partner has not detected remote fault    |

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|    |                        |           |     |                                                                                                                                                                    |
|----|------------------------|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12 | RESERVED               | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 12                                                                                                                |
| 11 | ASYMMETRIC_PAUSE       | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 11<br>1 = Link partner requests asymmetric pause<br>0 = Link partner does not request asymmetric pause            |
| 10 | PAUSE                  | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 10<br>1 = Link partner supports pause operation<br>0 = Link partner does not support pause operation              |
| 9  | 100BASE-T4             | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 9<br>1 = Link partner supports 100BASE-T4<br>0 = Link partner does not support 100BASE-T4                         |
| 8  | 100BASE-TX_FULL_DUPLEX | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 8<br>1 = Link partner supports 100BASE-TX full-duplex<br>0 = Link partner does not support 100BASE-TX full-duplex |
| 7  | 100BASE-TX_HALF_DUPLEX | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 7<br>1 = Link partner supports 100BASE-TX half-duplex<br>0 = Link partner does not support 100BASE-TX half-duplex |
| 6  | 10BASE-Te_FULL_DUPLEX  | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 6<br>1 = Link partner supports 10BASE-Te full-duplex<br>0 = Link partner does not support 10BASE-Te full-duplex   |
| 5  | 10BASE-Te_HALF_DUPLEX  | RO<br>SWC | 0x0 | Technology Ability Field. Received Code Word Bit 5<br>1 = Link partner supports 10BASE-Te half-duplex<br>0 = Link partner does not support                         |

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|     |                |           |     |                                           |
|-----|----------------|-----------|-----|-------------------------------------------|
|     |                |           |     | 10BASE-Tc half-duplex                     |
| 4:0 | SELECTOR_FIELD | RO<br>SWC | 0x0 | Selector Field Received Code Word Bit 4:0 |

### • 4.1.7. Auto-Negotiation expansion register (0x06)

Table 17. Auto-Negotiation expansion register (0x06)

| Bit  | Symbol                             | Access          | Default | Description                                                                                      |
|------|------------------------------------|-----------------|---------|--------------------------------------------------------------------------------------------------|
| 15:5 | Reserved                           | RO              | 0x0     | Reserved                                                                                         |
| 4    | Parallel Detection fault           | RO RC<br>SWC LH | 0x0     | 1 = Fault is detected<br>0 = No fault is detected                                                |
| 3    | Link partner nEXT page able        | RO SWC<br>LH    | 0x0     | 1 = Link partner supports NEXT page<br>0 = Link partner does not support next page               |
| 2    | Local NEXT Page able               | RO              | 0x1     | 1 = Local Device supports NEXT Page<br>0 = Local Device does not Next Page                       |
| 1    | Page received                      | RO RC<br>LH     | 0x0     | 1 = A new page is received<br>0 = No new page is received                                        |
| 0    | Link Partner Auto negotiation able | RO              | 0x0     | 1 = Link partner supports auto-negotiation<br>0 = Link partner does not support auto-negotiation |

### • 4.1.8. Auto-Negotiation NEXT Page register (0x07)

Table 18. Auto-Negotiation NEXT Page register (0x07)

| Bit  | Symbol             | Access | Default | Description                                                                                                                                                       |
|------|--------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | NEXT Page          | RW     | 0x0     | Transmit Code Word Bit 15<br>1 = The page is not the last page<br>0 = The page is the last page                                                                   |
| 14   | Reserved           | RO     | 0x0     | Transmit Code Word Bit 14                                                                                                                                         |
| 13   | Message page mode  | RW     | 0x1     | Transmit Code Word Bit 13<br>1 = Message Page<br>0 = Unformatted Page                                                                                             |
| 12   | Ack2               | RW     | 0x0     | Transmit Code Word Bit 12<br>1 = Comply with message<br>0 = Cannot comply with message                                                                            |
| 11   | Toggle             | RO     | 0x0     | Transmit Code Word Bit 11<br>1 = This bit in the previously exchanged Code Word is logic 0<br>0 = The Toggle bit in the previously exchanged Code Word is logic 1 |
| 10:0 | Message/Unformatte | RW     | 0x1     | Transmit Code Word Bits [10:0].                                                                                                                                   |

|  |  |  |  |                                                                                                                               |
|--|--|--|--|-------------------------------------------------------------------------------------------------------------------------------|
|  |  |  |  | These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0. |
|--|--|--|--|-------------------------------------------------------------------------------------------------------------------------------|

### 4.1.9. Auto-Negotiation link partner Received NEXT Page register (0x08)

Table 19. Auto-Negotiation link partner Received NEXT Page register (0x08)

| Bit  | Symbol             | Access | Default | Description                                                                                                                                                       |
|------|--------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | NEXT Page          | RO     | 0x0     | Received Code Word Bit 15<br>1 = This page is not the last page<br>0 = This page is the last page                                                                 |
| 14   | Reserved           | RO     | 0x0     | Received Code Word Bit 14                                                                                                                                         |
| 13   | Message page mode  | RO     | 0x0     | Received Code Word Bit 13<br>1 = Message Page<br>0 = Unformatted Page                                                                                             |
| 12   | Ack2               | RO     | 0x0     | Received Code Word Bit 12<br>1 = Comply with message<br>0 = Cannot comply with message                                                                            |
| 11   | Toggle             | RO     | 0x0     | Received Code Word Bit 11<br>1 = This bit in the previously exchanged Code Word is logic 0<br>0 = The Toggle bit in the previously exchanged Code Word is logic 1 |
| 10:0 | Message/Unformatte | RO     | 0x0     | Received Code Word Bit 10:0<br>These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.      |

### 4.1.10. MASTER-SLAVE control register (0x09)

Table 20. MASTER-SLAVE control register (0x09)

| Bit       | Symbol    | Access | Default | Description                                                                                                                                                                                                                                                                                            |
|-----------|-----------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1<br>3 | Test mode | RW     | 0x0     | The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing register 0x0 bit[15] must be performed to ensure normal operation.<br><br>000 = Normal Mode<br>001 = Test Mode 1 - Transmit Waveform |

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|    |                                          |    |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----|------------------------------------------|----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                                          |    |     | <p>Test</p> <p>010 = Test Mode 2 - Transmit Jitter Test (MASTER mode)</p> <p>011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode)</p> <p>100 = Test Mode 4 - Transmit Distortion Test</p> <p>110, 111 = Reserved</p> <p>normal operation.</p>                                                                                                                                                                                                                                                                                                                                                               |
| 12 | Master/Slave Manual configuration Enable | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>1 = Manual MASTER/SLAVE configuration<br/>0 = Automatic MASTER/SLAVE configuration.</p>                                |
| 11 | Master/Slave configuration               | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>This bit is ignored if bit[12] is 0.<br/>1 = Manual configuration as MASTER<br/>0 = Manual configuration as SLAVE.</p> |
| 10 | Port Type                                | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

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|     |                  |    |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|------------------|----|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                  |    |     | <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>This bit is ignored if bit[12] is 1.<br/>1 = Prefer multi-port device (MASTER)<br/>0 = Prefer single port device (SLAVE)</p>                                                                             |
| 9   | 1000BASE-T Full  | RW | 0x1 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>1 = Advertise<br/>0 = Not advertised</p>           |
| 8   | 1000BASE-T Half- | RW | 0x0 | <p>This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:</p> <ul style="list-style-type: none"> <li>• Software reset is asserted by writing register 0x0 bit[15]</li> <li>• Restart Auto-Negotiation is triggered by writing register 0x0 bit[9]</li> <li>• The port is switched from power down to normal operation by writing register 0x0 bit[11]</li> <li>• Link goes down</li> </ul> <p>1 = Advertise<br/>0 = Not advertised (default)</p> |
| 7:0 | Reserved         | RW | 0x0 | Write as 0, ignore on read.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

## 4.1.11. MASTER-SLAVE status register (0x0A)

Table 21. MASTER-SLAVE status register (0x0A)

| Bit | Symbol                                         | Access          | Default | Description                                                                                                                                                                           |
|-----|------------------------------------------------|-----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | Master/Slave_cfg_error                         | RO RC<br>SWC LH | 0x0     | This register bit will clear on read, rising of MII 0.12 and rising of AN complete.<br>1 = Master/Slave configuration fault detected<br>0 = No fault detected                         |
| 14  | Master/Slave configuration resolution          | RO              | 0x0     | This bit is not valid unless register 0x1 bit5 is 1.<br>1 = Local PHY configuration resolved to Master<br>0 = Local PHY configuration resolved to Slave                               |
| 13  | Local Receiver Status                          | RO              | 0x0     | 1 = Local Receiver OK<br>0 = Local Receiver not OK                                                                                                                                    |
| 12  | Remote Receiver Status                         | RO              | 0x0     | 1 = Remote Receiver OK<br>0 = Remote Receiver not OK                                                                                                                                  |
| 11  | Link Partner 1000Base-T Full Duplex Capability | RO              | 0x0     | This bit is not valid unless register 0x1 bit5 is 1.<br>1 = Link Partner supports 1000BASE-T half duplex<br>0 = Link Partner does not support 1000BASE-T half duplex                  |
| 10  | Link Partner 1000Base-T Half Duplex Capability | RO              | 0x0     | This bit is not valid unless register 0x1 bit5 is 1.<br>1 = Link Partner supports 1000Base-T full duplex<br>0 = Link Partner does not support 1000Base-T full duplex                  |
| 9:8 | Reserved                                       | RO              | 0x0     | Reserved                                                                                                                                                                              |
| 7:0 | Idle Error Count                               | RO RC           | 0x0     | MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over. |

## 4.1.12. MMD access control register (0x0D)

Table 22. MMD access control register (0x0D)

| Bit | Symbol | Access | Default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|

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|       |          |    |     |                                                                                                                                           |
|-------|----------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | Function | RW | 0x0 | 00 = Address<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only |
| 13:5  | Reserved | RO | 0x0 | Reserved                                                                                                                                  |
| 4:0   | DEVAD    | RW | 0x0 | MMD register device address.<br>00001 = MMD1<br>00011 = MMD3<br>00111 = MMD7                                                              |

### • 4.1.13. MMD access data register (0x0E)

Table 23. MMD access data register (0x0E)

| Bit  | Symbol       | Access | Default | Description                                                                                                                                                                                 |
|------|--------------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Address data | RW     | 0x0     | If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register. |

### • 4.1.14. Extended status register (0x0F)

Table 24. Extended status register (0x0F)

| Bit | Symbol                 | Access | Default | Description                                                                                              |
|-----|------------------------|--------|---------|----------------------------------------------------------------------------------------------------------|
| 15  | 1000BASE-X Full Duplex | RO     | 0x0     | 1 = PHY supports 1000BASE-X Full Duplex<br>0 = PHY does not supports 1000BASE-X Full Duplex<br>Always 0. |
| 14  | 1000BASE-X Half Duplex | RO     | 0x0     | 1 = PHY supports 1000BASE-X Half Duplex.<br>0 = PHY does not support 1000BASE-X Half Duplex.<br>Always 0 |
| 13  | 1000BASE-T Full Duplex | RO     | 0x1     | 1 = PHY supports 1000BASE-T Full Duplex<br>0 = PHY does not supports 1000BASE-T Full Duplex<br>Always 1  |
| 12  | 1000BASE-T Half Duplex | RO     | 0x0     | 1 = PHY supports 1000BASE-T Half Duplex<br>0 = PHY does not support 1000BASE-T Half Duplex<br>Always 0.  |

|      |          |    |     |          |
|------|----------|----|-----|----------|
| 11:0 | Reserved | RO | 0x0 | Always 0 |
|------|----------|----|-----|----------|

- 4.1.15. PHY specific function control register (0x10)

Table 25. PHY specific function control register (0x10)

| Bit  | Symbol      | Access | Default | Description                                                                                                                                                                                                                                                                                                     |
|------|-------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | Reserved    | RO     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                        |
| 6:5  | Cross_md    | RW     | 0x3     | Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset.<br>00 = Manual MDI configuration<br>01 = Manual MDIX configuration<br>10 = Reserved<br>11 = Enable automatic crossover for all modes |
| 4    | reserved    | RW     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                        |
| 3    | Crs_on_tx   | RW     | 0x0     | This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.                                                                                                                         |
| 2    | En_sqe_test | RW     | 0x0     | 1 = SQE test enabled, 0 = SQE test disabled<br>Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.                                                                                                                                                                 |
| 1    | En_pol_inv  | RW     | 0x1     | If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te.<br>1 = Polarity Reversal Enabled<br>0 = Polarity Reversal Disabled                                                                                                                                                          |
| 0    | Dis_jab     | RW     | 0x0     | Jabber takes effect only in 10BASE-Te half-duplex mode.<br>1 = Disable jabber function<br>0 = Enable jabber function                                                                                                                                                                                            |

- 4.1.16. PHY specific status register (0x11)

Table 26. PHY specific status register (0x11)

| Bit   | Symbol          | Access | Default | Description                                                                         |
|-------|-----------------|--------|---------|-------------------------------------------------------------------------------------|
| 15:14 | Speed_mode[1:0] | RO     | 0x0     | These status bits speed_mode[2:0] are valid only when bit11 is 1. Bit11 is set when |

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|     |                           |    |     |                                                                                                                                                                                                                                                                                                                                                 |
|-----|---------------------------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                           |    |     | <p>Auto-Negotiation is completed or Auto-Negotiation is disabled.</p> <p>Speed_mode[2:0]:</p> <p>100 = 2P5G</p> <p>011 = 10G</p> <p>010 = 1000 Mbps</p> <p>001 = 100 Mbps</p> <p>000 = 10 Mbps</p>                                                                                                                                              |
| 13  | Duplex                    | RO | 0x0 | <p>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.</p> <p>1 = Full-duplex</p> <p>0 = Half-duplex</p>                                                                                                                                                            |
| 12  | Page Received real-time   | RO | 0x0 | <p>1 = Page received</p> <p>0 = Page not received</p>                                                                                                                                                                                                                                                                                           |
| 11  | Speed and Duplex Resolved | RO | 0x0 | <p>When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode.</p> <p>1 = Resolved</p> <p>0 = Not resolved</p>                                                                                                                                                                                                                |
| 10  | Link status real-time     | RO | 0x0 | <p>1 = Link up</p> <p>0 = Link down</p>                                                                                                                                                                                                                                                                                                         |
| 9   | speed_mode[2]             | RO | 0x0 | Refer to bit15:14.                                                                                                                                                                                                                                                                                                                              |
| 8:7 | Reserved                  | RO | 0x0 | Reserved                                                                                                                                                                                                                                                                                                                                        |
| 6   | MDI Crossover Status      | RO | 0x0 | <p>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset.</p> <p>1 = MDIX</p> <p>0 = MDI</p> |
| 5   | Wirespeed downgrade       | RO | 0x0 | <p>1 = Downgrade</p> <p>0 = No Downgrade</p>                                                                                                                                                                                                                                                                                                    |
| 4   | Reserved                  | RO | 0x0 | Reserved                                                                                                                                                                                                                                                                                                                                        |
| 3   | Transmit Pause            | RO | 0x0 | <p>This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed.</p> <p>This bit indicates MAC pause resolution.</p> <p>This bit is for information purposes only and is not used by the device. When in force</p>                                                                                            |

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|   |                    |    |     |                                                                                                                                                                                                                                                                                                                               |
|---|--------------------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|   |                    |    |     | mode, this bit is set to be 0.<br>1 = Transmit pause enabled<br>0 = Transmit pause disabled                                                                                                                                                                                                                                   |
| 2 | Receive Pause      | RO | 0x0 | This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0.<br>1 = Receive pause enabled<br>0 = Receive pause disabled |
| 1 | Polarity Real Time | RO | 0x0 | 1 = Reverted polarity<br>0 = Normal polarity                                                                                                                                                                                                                                                                                  |
| 0 | Jabber Real Time   | RO | 0x0 | 1 = Jabber<br>0 = No jabber                                                                                                                                                                                                                                                                                                   |

### • 4.1.17. Interrupt Mask Register (0x12)

Table 27. Interrupt Mask Register (0x12)

| Bit | Symbol                          | Access | Default | Description                                   |
|-----|---------------------------------|--------|---------|-----------------------------------------------|
| 15  | Auto-Negotiation Error INT mask | RW     | 0x0     | 1 = Interrupt enable<br>0 = Interrupt disable |
| 14  | Speed Changed INT mask          | RW     | 0x0     | same as bit 15                                |
| 13  | Duplex changed INT mask         | RW     | 0x0     | same as bit 15                                |
| 12  | Page Received INT mask          | RW     | 0x0     | same as bit 15                                |
| 11  | Link Failed INT mask            | RW     | 0x0     | same as bit 15                                |
| 10  | Link Succeed INT mask           | RW     | 0x0     | same as bit 15                                |
| 9   | reserved                        | RW     | 0x0     | No used.                                      |
| 8   | Over temp INT mask              | RW     | 0x0     | same as bit 15                                |
| 7   | Big MSE INT mask                | RW     | 0x0     | Same as bit 15                                |
| 6   | WOL INT mask                    | RW     | 0x0     | same as bit 15                                |
| 5   | Wirespeed downgraded INT mask   | RW     | 0x0     | same as bit 15                                |
| 4   | CRC error INT mask              | RW     | 0x0     | same as bit 15                                |
| 3   | Link fail sds INT mask          | RW     | 0x0     | same as bit 15                                |
| 2   | Link success sds INT mask       | RW     | 0x0     | same as bit 15                                |
| 1   | Polarity changed INT mask       | RW     | 0x0     | same as bit 15                                |

|   |                          |    |     |                |
|---|--------------------------|----|-----|----------------|
| 0 | Jabber Happened INT mask | RW | 0x0 | same as bit 15 |
|---|--------------------------|----|-----|----------------|

## 4.1.18. Interrupt Status Register (0x13)

Table 28. Interrupt Status Register (0x13)

| Bit | Symbol                     | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | Auto-Negotiation Error INT | RO     | 0x0     | <p>Error can take place when any of the following happens:</p> <ul style="list-style-type: none"> <li>● MASTER/SLAVE does not resolve correctly</li> <li>● Parallel detect fault</li> <li>● No common HCD</li> <li>● Link does not come up after negotiation is complete</li> <li>● Selector Field is not equal</li> <li>● flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state</li> </ul> <p>1 = Auto-Negotiation Error takes place<br/>0 = No Auto-Negotiation Error takes place</p> |
| 14  | Speed Changed INT          | RO     | 0x0     | <p>1 = Speed changed<br/>0 = Speed not changed</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 13  | Duplex changed INT         | RO     | 0x0     | <p>1 = duplex changed<br/>0 = duplex not changed</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 12  | Page Received INT          | RO     | 0x0     | <p>1 = Page received<br/>0 = Page not received</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 11  | Link Failed INT            | RO     | 0x0     | <p>1 = Phy link down takes place<br/>0 = No link down takes place</p>                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 10  | Link Succeed INT           | RO     | 0x0     | <p>1 = Phy link up takes place<br/>0 = No link up takes place</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9   | reserved                   | RO     | 0x0     | reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 8   | Over_temp_int              | RO     | 0x0     | <p>1 = over temperature takes place<br/>0 = no over temperature takes place</p>                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7   | Big_mse_int                | RO     | 0x0     | <p>1 = Big MSE takes place<br/>0 = No big MSE takes place</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 6   | int_wol                    | RO     | 0x0     | <p>1 = WOL magic packet is received<br/>0 = No WOL magic packet is received</p>                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5   | Wirespeed downgraded INT   | RO     | 0x0     | <p>1 = speed downgraded.<br/>0 = Speed didn't downgrade.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4   | Crc_err_int                | RO     | 0x0     | <p>1 = CRC error takes place</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

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|   |                      |    |     |                                                                                                                 |
|---|----------------------|----|-----|-----------------------------------------------------------------------------------------------------------------|
|   |                      |    |     | 0 = No CRC error takes place                                                                                    |
| 3 | link_fail_sds_int    | RO | 0x0 | 1 = SDS link down takes place<br>0 = No link down takes place                                                   |
| 2 | Link_success_sds_int | RO | 0x0 | 1 = SDS link up takes place<br>0 = No link up takes place                                                       |
| 1 | Polarity changed INT | RO | 0x0 | 1 = PHY reversed MDI polarity<br>0 = PHY didn't revert MDI polarity                                             |
| 0 | Jabber Happened INT  | RO | 0x0 | 1 = 10BaseT TX jabber happened<br>0 = 10BaseT TX jabber didn't happen<br>Please refer to mii.1.1 Jabber_Detect. |

### • 4.1.19. Speed Auto Downgrade Control Register (0x14)

Table 29. Speed Auto Downgrade Control Register (0x14)

| Bit   | Symbol                            | Access | Default | Description                                                                                                                                                                                                                                                                                |
|-------|-----------------------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | Reserved                          | RO     | 0x0     | Reserved                                                                                                                                                                                                                                                                                   |
| 11    | En_mdio_latch                     | RO     | 0x1     | 1 = To latch MII/MMD register's read out value during MDIO read                                                                                                                                                                                                                            |
| 10:6  | reserved                          | RW     | 0x0     | reserved                                                                                                                                                                                                                                                                                   |
| 5     | En_speed_downgrade                | RW POS | 0x1     | When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update. This bit will be set to 1'b0 in UTP_TO_FIBER_FORCE and UTP_TO_FIBER_AUTO mode; else set to 1'b1, only take effect after software reset                              |
| 4:2   | Autoneg retry limit pre-downgrade | RW     | 0x3     | If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits. only take effect after software reset                                                                                        |
| 1     | Bp_autospd_timer                  | RW     | 0x0     | 1 = the wirespeed downgrade FSM will bypass the timer used for link stability check; only take effect after software reset<br>0 = not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1. |
| 0     | Reserved                          | RO     | 0x0     | Reserved                                                                                                                                                                                                                                                                                   |

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- 4.1.20. Rx Error Counter Register (0x15)

Table 30. Rx Error Counter Register (0x15)

| Bit  | Symbol         | Access | Default | Description                                                                                                                                                                  |
|------|----------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Rx_err_counter | RO     | 0x0     | This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over. Valid only for 1000BASE-T and 100BASE-Tx |

- 4.1.21. Debug Register's Address Offset Register (0x1E)

Table 31. Debug Register's Address Offset Register (0x1E)

| Bit  | Symbol                        | Access | Default | Description                                                              |
|------|-------------------------------|--------|---------|--------------------------------------------------------------------------|
| 15:0 | Debug Register Address Offset | RW     | 0x0     | It's the address offset of the debug register that will be Write or Read |

- 4.1.22. Debug Register's Data Register (0x1F)

Table 32. Debug Register's Data Register (0x1F)

| Bit  | Symbol               | Access | Default | Description                                                                                                                                        |
|------|----------------------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Debug Register Datas | RW     | 0x0     | It's the data to be written to the debug register indicated by the address offset in register 0x1E, or the data read out from that debug register. |

## 4.2. Phy EXT Register

- 4.2.1. Sleep Control1 (0x27)

Table 33. Sleep Control1 (0x27)

| Bit | Symbol       | Access | Default | Description                                                                                               |
|-----|--------------|--------|---------|-----------------------------------------------------------------------------------------------------------|
| 15  | En_sleep_sw  | RW     | 0x0     | 1 = enable sleep mode: PHY will enter sleep mode and close AFE after unplug cable for a timer;            |
| 14  | Pllon_in_slp | RO     | 0x0     | 1 = keep PLL on in sleep mode;<br>0 = close PLL in sleep mode.                                            |
| 13  | Slp_pulse_sw | RW     | 0x1     | when PHY enter sleep,<br>1 = enable PHY to send out one pulse periodic;<br>0 = disable PHY to send pulse. |

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|      |           |    |     |                                            |
|------|-----------|----|-----|--------------------------------------------|
| 12   | Reserved  | RW | 0x0 | Reserved                                   |
| 11:6 | Reserved  | RO | 0x0 | Reserved                                   |
| 5    | Sleeping  | RO | 0x0 | 1 = PHY is slept; 0 = PHY is waked         |
| 4    | Gate_25m  | RO | 0x0 | Not used.                                  |
| 3:0  | Slp_state | RO | 0x0 | FSM state of internal sleep control logic. |

### 4.2.2 pkg\_cfg0 (0xA0)

Table 34. pkg\_cfg0 (0xA0)

| Bit  | Symbol             | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                  |
|------|--------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | Pkg_chk_en         | RW     | 0x0     | 1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.                                                                                                                                                                                                               |
| 14   | Pkg_en_gate        | RW     | 0x1     | 1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;<br>0: not gate the clocks.                                                                                                                                                                                         |
| 13   | Bp_pkg_gen         | RW     | 0x1     | 1: normal mode, to send xMII TX data from PAD;<br>0: test mode, to send out the MII data generated by pkg_gen module.                                                                                                                                                                                                                                        |
| 12   | Pkg_gen_en         | RW     | 0x0     | 1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0;<br>Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared. |
| 11:8 | Pkg_prm_lth        | RW     | 0x8     | The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.                                                                                                                                                                            |
| 7:4  | Pkg_ipg_lth        | RW     | 0xd     | The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.                                                                                                                                                                                        |
| 3    | Xmit_mac_force_gen | RW     | 0x0     | 1: To enable pkg_gen to send out the                                                                                                                                                                                                                                                                                                                         |

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|     |                 |    |     |                                                                                                                                                                                            |
|-----|-----------------|----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                 |    |     | generated data even when the link is not established.                                                                                                                                      |
| 2   | Pkg_corrupt_crc | RW | 0x0 | 1: to make pkg_gen to send out CRC error packages.<br>0: pkg_gen sends out CRC good packages.                                                                                              |
| 1:0 | Pkg_payload     | RW | 0x0 | Control the payload of the generated packages.<br>00: increased Byte payload;<br>01: random payload;<br>10: fix pattern 0x5AA55AA5...<br>11: fixed pattern programed by EXT 0x9F<br>bit7:0 |

---

### 4.2.3. pkg\_cfg1 (0xA1)

Table 35. pkg\_cfg1 (0xA1)

| Bit  | Symbol     | Access | Default | Description                                  |
|------|------------|--------|---------|----------------------------------------------|
| 15:0 | Pkg_length | RW     | 0x40    | To set the length of the generated packages. |

---

### 4.2.4. pkg\_cfg2 (0xA2)

Table 36. pkg\_cfg2 (0xA2)

| Bit  | Symbol         | Access | Default | Description                                                     |
|------|----------------|--------|---------|-----------------------------------------------------------------|
| 15:0 | Pkg_burst_size | RW     | 0x0     | To set the number of packages in a burst of package generation. |

---

### 4.2.5. pkg\_rx\_valid0 (0xA3)

Table 37. pkg\_rx\_valid0 (0xA3)

| Bit  | Symbol            | Access | Default | Description                                                                                                                         |
|------|-------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_valid_high | RO     | 0x0     | Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. |

---

### 4.2.6. pkg\_rx\_valid1 (0xA4)

Table 38. pkg\_rx\_valid1 (0xA4)

| Bit  | Symbol           | Access | Default | Description                                                                   |
|------|------------------|--------|---------|-------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_valid_low | RO     | 0x0     | Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose |

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|  |  |  |  |                                                      |
|--|--|--|--|------------------------------------------------------|
|  |  |  |  | CRC are good and length are >=64Byte and <=1518Byte. |
|--|--|--|--|------------------------------------------------------|

### 4.2.7. pkg\_rx\_os0 (0xA5)

Table 39. pkg\_rx\_os0 (0xA5)

| Bit  | Symbol              | Access | Default | Description                                                                                                               |
|------|---------------------|--------|---------|---------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_os_good_high | RO     | 0x0     | Pkg_ib_os_good[31:16], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

### 4.2.8. pkg\_rx\_os1 (0xA6)

Table 40. pkg\_rx\_os1 (0xA6)

| Bit  | Symbol             | Access | Default | Description                                                                                                              |
|------|--------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_os_good_low | RO     | 0x0     | Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

### 4.2.9. pkg\_rx\_us0 (0xA7)

Table 41. pkg\_rx\_us0 (0xA7)

| Bit  | Symbol              | Access | Default | Description                                                                                                             |
|------|---------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_us_good_high | RO     | 0x0     | Pkg_ib_us_good[31:16], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte. |

### 4.2.10. pkg\_rx\_us1 (0xA8)

Table 42. pkg\_rx\_us1 (0xA8)

| Bit  | Symbol             | Access | Default | Description                                                                                                              |
|------|--------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_us_good_low | RO     | 0x0     | Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

### 4.2.11. pkg\_rx\_err (0xA9)

Table 43. pkg\_rx\_err (0xA9)

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| Bit  | Symbol     | Access | Default | Description                                                                                                |
|------|------------|--------|---------|------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_err | RO     | 0x0     | pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte. |

---

### 4.2.12. pkg\_rx\_os\_bad (0xAA)

Table 44. pkg\_rx\_os\_bad (0xAA)

| Bit  | Symbol        | Access | Default | Description                                                                                        |
|------|---------------|--------|---------|----------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_os_bad | RO     | 0x0     | pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >1518Byte. |

---

### 4.2.13. pkg\_rx\_fragment (0xAB)

Table 45. pkg\_rx\_fragment (0xAB)

| Bit  | Symbol      | Access | Default | Description                                                                  |
|------|-------------|--------|---------|------------------------------------------------------------------------------|
| 15:0 | Pkg_ib_frag | RO     | 0x0     | pkg_ib_frag is the number of RX packages from wire whose length are <64Byte. |

---

### 4.2.14. pkg\_rx\_nosfd (0xAC)

Table 46. pkg\_rx\_nosfd (0xAC)

| Bit  | Symbol       | Access | Default | Description                                                              |
|------|--------------|--------|---------|--------------------------------------------------------------------------|
| 15:0 | Pkg_ib_nosfd | RO     | 0x0     | pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed. |

---

### 4.2.15. pkg\_tx\_valid0 (0xAD)

Table 47. pkg\_tx\_valid0 (0xAD)

| Bit  | Symbol            | Access | Default | Description                                                                                                                        |
|------|-------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_valid_high | RO     | 0x0     | Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte. |

---

### 4.2.16. pkg\_tx\_valid1 (0xAE)

Table 48. pkg\_tx\_valid1 (0xAE)

| Bit  | Symbol           | Access | Default | Description                                                                  |
|------|------------------|--------|---------|------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_valid_low | RO     | 0x0     | Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose |

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|  |  |  |  |                                                      |
|--|--|--|--|------------------------------------------------------|
|  |  |  |  | CRC are good and length are >=64Byte and <=1518Byte. |
|--|--|--|--|------------------------------------------------------|

### 4.2.17. pkg\_tx\_os0 (0xAF)

Table 49. pkg\_tx\_os0 (0xAF)

| Bit  | Symbol              | Access | Default | Description                                                                                                              |
|------|---------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_os_good_high | RO     | 0x0     | Pkg_ob_os_good[31:16], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

### 4.2.18. pkg\_tx\_os1 (0xB0)

Table 50. pkg\_tx\_os1 (0xB0)

| Bit  | Symbol             | Access | Default | Description                                                                                                             |
|------|--------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_os_good_low | RO     | 0x0     | Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

### 4.2.19. pkg\_tx\_us0 (0xB1)

Table 51. pkg\_tx\_us0 (0xB1)

| Bit  | Symbol              | Access | Default | Description                                                                                                            |
|------|---------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_us_good_high | RO     | 0x0     | Pkg_ob_us_good[31:16], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte. |

### 4.2.20. pkg\_tx\_us1 (0xB2)

Table 52. pkg\_tx\_us1 (0xB2)

| Bit  | Symbol             | Access | Default | Description                                                                                                             |
|------|--------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_us_good_low | RO     | 0x0     | Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

### 4.2.21. pkg\_tx\_err (0xB3)

Table 53. pkg\_tx\_err (0xB3)

| Bit  | Symbol     | Access | Default | Description                             |
|------|------------|--------|---------|-----------------------------------------|
| 15:0 | Pkg_ob_err | RW     | 0x0     | pkg_ob_err is the number of TX packages |

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|  |  |  |  |                                                                   |
|--|--|--|--|-------------------------------------------------------------------|
|  |  |  |  | from MII whose CRC are wrong and length are >=64Byte, <=1518Byte. |
|--|--|--|--|-------------------------------------------------------------------|

### 4.2.22. pkg\_tx\_os\_bad (0xB4)

Table 54. pkg\_tx\_os\_bad (0xB4)

| Bit  | Symbol        | Access | Default | Description                                                                                       |
|------|---------------|--------|---------|---------------------------------------------------------------------------------------------------|
| 15:0 | Pkg_ob_os_bad | RO     | 0x0     | pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >1518Byte. |

### 4.2.23. pkg\_tx\_fragment (0xB5)

Table 55. pkg\_tx\_fragment (0xB5)

| Bit  | Symbol      | Access | Default | Description                                                                 |
|------|-------------|--------|---------|-----------------------------------------------------------------------------|
| 15:0 | Pkg_ob_frag | RO     | 0x0     | pkg_ob_frag is the number of TX packages from MII whose length are <64Byte. |

### 4.2.24. pkg\_tx\_nosfd (0xB6)

Table 56. pkg\_tx\_nosfd (0xB6)

| Bit  | Symbol       | Access | Default | Description                                                          |
|------|--------------|--------|---------|----------------------------------------------------------------------|
| 15:0 | Pkg_ob_nosfd | RO     | 0x0     | pkg_ob_nosfd is the number of packages from MII whose SFD is missed. |

### 4.2.25. CH0\_mse (0x51F)

Table 57. CH0\_mse (0x51F)

| Bit  | Symbol        | Access | Default | Description       |
|------|---------------|--------|---------|-------------------|
| 15:0 | channel 0 mse | RO     | 0x0     | utp channel 0 MSE |

### 4.2.26. CH1\_mse (0x520)

Table 58. CH1\_mse (0x520)

| Bit  | Symbol        | Access | Default | Description       |
|------|---------------|--------|---------|-------------------|
| 15:0 | channel 1 mse | RO     | 0x0     | utp channel 1 MSE |

### 4.2.27. CH2\_mse (0x521)

Table 59. CH2\_mse (0x521)

| Bit | Symbol | Access | Default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|

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|      |               |    |     |                   |
|------|---------------|----|-----|-------------------|
| 15:0 | channel 2 mse | RO | 0x0 | utp channel 2 MSE |
|------|---------------|----|-----|-------------------|

### 4.2.28. CH3\_mse (0x522)

Table 60. CH3\_mse (0x522)

| Bit  | Symbol        | Access | Default | Description       |
|------|---------------|--------|---------|-------------------|
| 15:0 | channel 3 mse | RO     | 0x0     | utp channel 3 MSE |

## 4.3. Phy MMD Register

### 4.3.1 PMA/PMD control 1 register(MMD1,0x0)

Table 61.PMA/PMD control 1 register(MMD1,0x0)

| Bit  | Symbol                          | Access | Default | Description                                                                                                                  |
|------|---------------------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------|
| 15   | Pma_rst                         | RW SC  | 0x0     | Setting this bit will set all PMA/PMD registers to their default states. This action also initiate a reset in MMD3 and MMD7. |
| 14   | reserved                        | RO     | 0x0     | Reserved                                                                                                                     |
| 13   | mii_0_speed_sel_1_0[0] :<br>LSB | RW     | 0x0     | 1.0.6 1.0.13<br>1 1 = bits 5:2 select speed<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s                            |
| 12   | reserved                        | RO     | 0x0     | Reserved                                                                                                                     |
| 11   | pma_low_power                   | RW     | 0x0     | 1: low power mode. 0: normal operation                                                                                       |
| 10:7 | reserved                        | RO     | 0x0     | Reserved                                                                                                                     |
| 6    | mii_0_speed_sel_1_0[1] :<br>MSB | RW     | 0x0     | refer to bit13                                                                                                               |
| 5:2  | pma_speed_sel_5_2               | RW     | 0x6     | 0000 : 10Gb/s<br>speed 0110 :<br>2.5Gb/s<br>0111 : 5Gb/s                                                                     |
| 1    | pma_rem_lpbk                    | RO     | 0x0     | 1 = Enable PMA remote loopback mode<br>0 = Disable PMA remote loopback mode                                                  |

### 4.3.2. PMA/PMD status 1 register(MMD1,0x1)

Table 62.PMA/PMD status 1 register(MMD1,0x1)

| Bit  | Symbol   | Access | Default | Description |
|------|----------|--------|---------|-------------|
| 15:3 | reserved | RO     | 0x0     |             |

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|   |                   |    |     |  |
|---|-------------------|----|-----|--|
| 2 | pma_rx_lnk_st_ll  | RW | 0x0 |  |
| 1 | low_power ability | RO | 0x1 |  |
| 0 | reserved          | RO | 0x0 |  |

### 4.3.3 PMA/PMD ability(MMD1,0x4)

Table 63.PMA/PMD ability(MMD1,0x4)

| Bit  | Symbol            | Access | Default | Description          |
|------|-------------------|--------|---------|----------------------|
| 15   | reserved          | RO     | 0x0     | reserved             |
| 14   | 5G ability        | RO     | 0x0     | 5G ability           |
| 13   | 2.5g ability      | RO     | 0x1     | 2.5g ability         |
| 12:7 | reserved          | RO     | 0x0     | reserved             |
| 6    | 10M ability       | RO     | 0x1     | 10M_ability          |
| 5    | 100M ability      | RO     | 0x1     | 100M ability         |
| 4    | 1000M ability     | RO     | 0x1     | 1000M ability        |
| 3    | reserved          | RO     | 0x0     | always 0.            |
| 2    | 10PASS-Ts capable | RO     | 0x0     | no 10PASS-Ts ability |
| 1    | 2BASE-TL capable  | RO     | 0x0     | no 2BASE-TL ability  |
| 0    | 10G capable       | RO     | 0x0     | no 10G ability       |

### 4.3.4. PMA/PMD devices in package(MMD1,0x5)

Table 64.PMA/PMD devices in package(MMD1,0x5)

| Bit  | Symbol          | Access | Default | Description                                |
|------|-----------------|--------|---------|--------------------------------------------|
| 15:8 | Reserved        | RO     | 0x0     | Reserved                                   |
| 7    | Autoneg_present | RO     | 0x1     | 1= Auto-Negotiation present in package;    |
| 6:4  | Reserved        | RO     | 0x0     | Reserved                                   |
| 3    | PCS_present     | RO     | 0x1     | 1= PCS present in package;                 |
| 2    | Reserved        | RO     | 0x0     | Reserved                                   |
| 1    | PMA_present     | RO     | 0x1     | 1= PMA present in package;                 |
| 0    | MII_reg_present | RO     | 0x1     | 1= Clause 22 registers present in package; |

### 4.3.5.PMA/PMD TYPE SEL(MMD1,0x7)

Table 65.PMA/PMD TYPE SEL(MMD1,0x7)

| Bit  | Symbol       | Access | Default | Description                                  |
|------|--------------|--------|---------|----------------------------------------------|
| 15:7 | Reserved     | RO     | 0x0     | Reserved                                     |
| 6:0  | PMA Type Sel | RW     | 0x30    | 0x31 : 5GBase-T PMA<br>0x30 : 2.5GBase-T PMA |

## 4.3.6.PMA/PMD status 2 register(MMD1,0x8)

Table 66.PMA/PMD status 2 register(MMD1,0x8)

| Bit   | Symbol                 | Access | Default | Description                                                                                                            |
|-------|------------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------|
| 15:14 | MMD1_present           | RO     | 0x2     | Always 2'b10.                                                                                                          |
| 13    | TX_fault_ability       | RO     | 0x0     | PMA/PMD does not have the ability to detect a fault condition on the transmit path.                                    |
| 12    | RX_fault_ability       | RO     | 0x0     | PMA/PMD does not have the ability to detect a fault condition on the receive path.                                     |
| 11    | Transmit fault         | RO     | 0x0     | Reserved                                                                                                               |
| 10    | Receive fault          | RO     | 0x0     | Reserved                                                                                                               |
| 9     | PMD extern ability     | RO     | 0x1     | 1 = PMA/PMD has extended abilities listed in register 1.11<br>0 = PMA/PMD does not have extended abilities             |
| 8     | PMD Tx disable capable | RO     | 0x1     | 1 = PMD has the ability to disable the transmit path<br>0 = PMD does not have the ability to disable the transmit path |
| 7:1   | Extra_abilities        | RO     | 0x0     | Reserved                                                                                                               |
| 0     | PMA local lpbk capable | RO     | 0x1     | 1: PMA has the ability to perform a local loopback function.                                                           |

## 4.3.7.PMA/PMD extended ability(MMD1,0xB)

Table 67.PMA/PMD extended ability(MMD1,0xB)

| Bit | Symbol                       | Access | Default | Description                                                                                                                |
|-----|------------------------------|--------|---------|----------------------------------------------------------------------------------------------------------------------------|
| 15  | BASE-H extended abilities    | RO     | 0x0     | BASE-H extended abilities                                                                                                  |
| 14  | 2.5G/5G extended abilities   | RO     | 0x1     | 1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21<br>0 = PMA/PMD does not have 2.5G/5G extended abilities |
| 13  | 200G/400G extended abilities | RO     | 0x0     | 200G/400G extended abilities                                                                                               |
| 12  | 25G extended abilities       | RO     | 0x0     | 25G extended abilities                                                                                                     |
| 11  | BASE-T1 extended abilities   | RO     | 0x0     | BASE-T1 extended abilities                                                                                                 |
| 10  | 40G/100G extended abilities  | RO     | 0x0     | 40G/100G extended abilities                                                                                                |

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|   |                     |    |     |                                                                                            |
|---|---------------------|----|-----|--------------------------------------------------------------------------------------------|
| 9 | P2MP ability        | RO | 0x0 | P2MP ability                                                                               |
| 8 | 10BASE-T ability    | RO | 0x1 | 1 = PMA/PMD is able to perform 10BASE-T<br>0 = PMA/PMD is not able to perform 10BASE-T     |
| 7 | 100BASE-TX ability  | RO | 0x1 | 1 = PMA/PMD is able to perform 100BASE-TX<br>0 = PMA/PMD is not able to perform 100BASE-TX |
| 6 | 1000BASE-KX ability | RO | 0x0 | 1000BASE-KX ability                                                                        |
| 5 | 1000BASE-T ability  | RO | 0x1 | 1 = PMA/PMD is able to perform 1000BASE-T<br>0 = PMA/PMD is not able to perform 1000BASE-T |
| 4 | 10GBASE-KR ability  | RO | 0x0 | 10GBASE-KR ability                                                                         |
| 3 | 10GBASE-KX4 ability | RO | 0x0 | 10GBASE-KX4 ability                                                                        |
| 2 | 10GBASE-T ability   | RO | 0x0 | 10GBASE-T ability                                                                          |
| 1 | 10GBASE-LRM ability | RO | 0x0 | 10GBASE-LRM ability                                                                        |

### 4.3.8. 2.5G PMA/PMD extended ability(MMD1,0x15)

**Table 68.2.5G PMA/PMD extended ability(MMD1,0x15)**

| Bit  | Symbol             | Access | Default | Description                                                                                |
|------|--------------------|--------|---------|--------------------------------------------------------------------------------------------|
| 15:2 | reserved           | RO     | 0x0     | reserved                                                                                   |
| 1    | 5GBASE-T ability   | RO     | 0x0     | 1 = PMA/PMD is able to perform 5GBASE-T<br>0 = PMA/PMD is not able to perform 5GBASE-T     |
| 0    | 2.5GBASE-T ability | RO     | 0x1     | 1 = PMA/PMD is able to perform 2.5GBASE-T<br>0 = PMA/PMD is not able to perform 2.5GBASE-T |

### 4.3.9. Multi-GBASE-T status(MMD1,0x81)

**Table 69. Multi-GBASE-T status(MMD1,0x81)**

| Bit  | Symbol            | Access | Default | Description                           |
|------|-------------------|--------|---------|---------------------------------------|
| 15:1 | reserved          | RO     | 0x0     | reserved                              |
| 0    | lp_info_vld_latch | RO     | 0x0     | 1 = Link partner information is valid |

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|  |  |  |  |                                                                                                                                                |
|--|--|--|--|------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  |  |  | 0 = Link partner information is invalid when MMD1 0x8000 bit0 is 1, this bit is Latch High(LH), else, it's the real time value of lp_info_vld. |
|--|--|--|--|------------------------------------------------------------------------------------------------------------------------------------------------|

### 4.3.10. Multi-GBASE-T pair swap and polarity(MMD1,0x82)

**Table 70.**Multi-GBASE-T pair swap and polarity(MMD1,0x82)

| Bit   | Symbol         | Access | Default | Description |
|-------|----------------|--------|---------|-------------|
| 15:12 | reserved       | RO     | 0x0     |             |
| 11    | mg_pol_flag_3  | RO     | 0x0     |             |
| 10    | mg_pol_flag_2  | RO     | 0x0     |             |
| 9     | mg_pol_flag_1  | RO     | 0x0     |             |
| 8     | mg_pol_flag_0  | RO     | 0x0     |             |
| 7:2   | reserved       | RO     | 0x0     |             |
| 1:0   | mdi_connection | RO     | 0x0     |             |

### 4.3.11. Multi-GBASE-T TX power backoff and PHY short reach setting(MMD1,0x83)

**Table 71.**Multi-GBASE-T TX power backoff and PHY short reach setting(MMD1,0x83)

| Bit   | Symbol      | Access | Default | Description                                                                                                                                                    |
|-------|-------------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | lp_pbo_set  | RO     | 0x0     | Link partner TX power backoff. 1 1 1 = 14dB;<br>1 1 0 = 12dB;<br>1 0 1 = 10dB;<br>1 0 0 = 8dB;<br>0 1 1 = 6dB;<br>0 1 0 = 4dB;<br>0 0 1 = 2dB;<br>0 0 0 = 0dB; |
| 12:10 | loc_pbo_set | RO     | 0x0     | TX power backoff setting. 1 1 1 = 14dB;<br>1 1 0 = 12dB;<br>1 0 1 = 10dB;<br>1 0 0 = 8dB;<br>0 1 1 = 6dB;<br>0 1 0 = 4dB;<br>0 0 1 = 2dB;<br>0 0 0 = 0dB;      |
| 9:0   | reserved    | RO     | 0x0     | reserved                                                                                                                                                       |

## 4.3.12. Multi-GBASE-T test mode(MMD1,0x84)

Table 72.Multi-GBASE-T test mode(MMD1,0x84)

| Bit       | Symbol       | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------|--------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1<br>3 | test_mode_mg | RW     | 0x0     | <p>15 14 13</p> <p>1 1 1 = Test mode 7. Pseudo-random test mode for BER Monitor.</p> <p>1 1 0 = Test mode 6. Transmitter droop test mode.</p> <p>1 0 1 = Test mode 5. Normal operation with no power backoff. This is for the PSD mask and power level test.</p> <p>1 0 0 = Test mode 4. Transmit distortion test.</p> <p>0 1 1 = Test mode 3. Transmit jitter test in SLAVE mode.</p> <p>0 1 0 = Test mode 2. Transmit jitter test in MASTER mode.</p> <p>0 0 1 = Test mode 1. Setting of MASTER transmitter required by SLAVE for transmit jitter test in SLAVE mode.</p> <p>0 0 0 = Normal operation</p>                                                                                                                                                             |
| 12:1<br>0 | tx_test_freq | RW     | 0x0     | <p>Valid when test mode 4 is selected.</p> <p>12 11 10</p> <p>1 1 1 = Reserved</p> <p>1 1 0 = Dual tone 5, <math>S \times (400/1024) \times 397</math>, <math>S \times (400/1024) \times 401</math></p> <p>1 0 1 = Dual tone 4, <math>S \times (400/1024) \times 277</math>, <math>S \times (400/1024) \times 281</math></p> <p>1 0 0 = Dual tone 3, <math>S \times (400/1024) \times 179</math>, <math>S \times (400/1024) \times 181</math></p> <p>0 1 1 = Reserved</p> <p>0 1 0 = Dual tone 2, <math>S \times (400/1024) \times 101</math>, <math>S \times (400/1024) \times 103</math></p> <p>0 0 1 = Dual tone 1, <math>S \times (400/1024) \times 47</math>, <math>S \times (400/1024) \times 53</math></p> <p>0 0 0 = Reserved</p> <p>for 2.5GBASE-T, S=0.5.</p> |
| 9:0       | reserved     | RO     | 0x0     | reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 4.3.13. Multi-GBASE-Tskew delay 1(MMD1,0x91)

**Table 73.**Multi-GBASE-Tskew delay 1(MMD1,0x91)

| Bit  | Symbol       | Access | Default | Description                                    |
|------|--------------|--------|---------|------------------------------------------------|
| 15   | reserved     | RO     | 0x0     | reserved                                       |
| 14:8 | skew_delay_b | RO     | 0x0     | skew delay for pair B, with respect to pair A. |
| 7:0  | reserved     | RO     | 0x0     | reserved                                       |

### 4.3.14. Multi-GBASE-Tskew delay 2(MMD1,0x92)

**Table 74.**Multi-GBASE-Tskew delay 2(MMD1,0x92)

| Bit  | Symbol       | Access | Default | Description                                    |
|------|--------------|--------|---------|------------------------------------------------|
| 15   | reserved     | RO     | 0x0     | Reserved                                       |
| 14:8 | skew_delay_d | RO     | 0x0     | skew delay for pair D, with respect to pair A. |
| 7    | reserved     | RO     | 0x0     | Reserved                                       |
| 6:0  | skew_delay_c | RO     | 0x0     | skew delay for pair C, with respect to pair A. |

### 4.3.15. Multi-GBASE-T fast retrain status and control(MMD1,0x93)

**Table 75.**Multi-GBASE-T fast retrain status and control(MMD1,0x93)

| Bit   | Symbol               | Access | Default | Description                                                                                                                                                                                             |
|-------|----------------------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | fr_rx_counter        | RO     | 0x0     | Counts the number of fast retrain requested by the link partner.                                                                                                                                        |
| 10:6  | fr_tx_counter        | RO     | 0x0     | Counts the number of fast retrain requested by the local device.                                                                                                                                        |
| 5     | reserved             | RO     | 0x0     | always 0.                                                                                                                                                                                               |
| 4     | Fast retrain ability | RO     | 0x1     | Fast retrain ability is supported.                                                                                                                                                                      |
| 3     | fr_negotiated        | RO     | 0x0     | 1 = Fast retrain capability was negotiated<br>0 = Fast retrain capability was not negotiated                                                                                                            |
| 2:1   | fr_sigtype           | RW     | 0x0     | fast retrain signal type. 1 1 = reserved;<br>1 0 = PHY signal Link interruption during fast retrain;<br>0 1 = PHY signal local fault during fast retrain;<br>0 0 = PHY signal IDLE during fast retrain; |
| 0     | fr_enable            | RW     | 0x1     | 1 = Fast retrain capability is enabled<br>0 = Fast retrain capability is disabled                                                                                                                       |

## 4.3.16. PCS control 1 register(MMD3,0x0)

Table 76.PCS control 1 register(MMD3,0x0)

| Bit   | Symbol          | Access    | Default | Description                                                                                                              |
|-------|-----------------|-----------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15    | Pcs_rst         | RW SC     | 0x0     | Setting this bit will set all PCS registers to their default states. This action also initiate a reset in MMD1 and MMD7. |
| 14    | pcs_lpbk        | RW        | 0x0     | 1: enable PCS loopback mode.                                                                                             |
| 13:11 | Reserved        | RO        | 0x4     | Reserved                                                                                                                 |
| 10    | Clock_stoppable | RW<br>SWC | 0x0     | Not used.                                                                                                                |
| 9:6   | Reserved        | RO        | 0x1     | Reserved                                                                                                                 |
| 5:2   | speed_sel       | RO        | 0x7     | Reserved                                                                                                                 |
| 1:0   | Reserved        | RO        | 0x0     | Reserved                                                                                                                 |

## 4.3.17. PCS status 1 register(MMD3,0x1)

Table 77.PCS status 1 register(MMD3,0x1)

| Bit    | Symbol           | Access | Default | Description                                                                                                                                             |
|--------|------------------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12  | Reserved         | RO     | 0x0     | Reserved                                                                                                                                                |
| 1<br>1 | Tx_lpi_rxd       | RO LH  | 0x0     | When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Lach High. |
| 1<br>0 | Rx_lpi_rxd       | RO LH  | 0x0     | When read as 1, it indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. Lach High.  |
| 9      | Tx_lpi_indic     | RO     | 0x0     | When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.                                                       |
| 8      | Rx_lpi_indic     | RO     | 0x0     | When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.                                                        |
| 7:3    | Reserved         | RO     | 0x0     | Reserved                                                                                                                                                |
| 2      | Pcsrx_lnk_status | RO LL  | 0x0     | PCS status, latch low.                                                                                                                                  |
| 1:0    | Reserved         | RO     | 0x0     | Reserved                                                                                                                                                |

## 4.3.18. PCS speed ability(MMD3,0x4)

**Table 78.PCS speed ability(MMD3,0x4)**

| Bit  | Symbol           | Access | Default | Description                                |
|------|------------------|--------|---------|--------------------------------------------|
| 15:8 | Reserved         | RO     | 0x0     | Reserved                                   |
| 7    | pcs_5g_adv_cap   | RO     | 0x0     | PCS is not capable of operating at 5Gb/s.  |
| 6    | pcs_2p5g_adv_cap | RO     | 0x1     | PCS is capable of operating at 2.5Gb/s.    |
| 5:1  | Reserved         | RO     | 0x0     | Reserved                                   |
| 0    | pcs_10g_adv_cap  | RO     | 0x0     | PCS is not capable of operating at 10Gb/s. |

## 4.3.19. EEE control and capability register(MMD3,0x14)

**Table 79.EEE control and capability register(MMD3,0x14)**

| Bit  | Symbol         | Access | Default | Description                               |
|------|----------------|--------|---------|-------------------------------------------|
| 15:3 | Reserved       | RO     | 0x0     | Reserved                                  |
| 2    | 1000BASE-T EEE | RO     | 0x1     | Always 1. EEE is supported for 1000BASE-T |
| 1    | 100BASE-TX EEE | RO     | 0x1     | Always 1. EEE is supported for 100BASE-TX |
| 0    | Reserved       | RO     | 0x0     | Reserved                                  |

## 4.3.20. EEE control and capability 2 register(MMD3,0x15)

**Table 80.EEE control and capability 2 register(MMD3,0x15)**

| Bit  | Symbol       | Access | Default | Description                       |
|------|--------------|--------|---------|-----------------------------------|
| 15:2 | Reserved     | RO     | 0x0     | Reserved                          |
| 1    | pcs_5g_eee   | RO     | 0x0     | 1 = pcs support 2.5g eee ability. |
| 0    | pcs_2p5g_eee | RO     | 0x1     | Reserved                          |

## 4.3.21. EEE wake error counter (MMD3,0x16)

**Table 81.EEE wake error counter(MMD3,0x16)**

| Bit  | Symbol           | Access    | Default | Description                                                                                                                         |
|------|------------------|-----------|---------|-------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Lpi_wake_err_cnt | RO RC SWC | 0x0     | Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. |

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### 4.3.22. AN Control Register(MMD7,0x0)

**Table 82.AN Control Register(MMD7,0x0)**

| Bit   | Symbol       | Access | Default | Description                                                                                                             |
|-------|--------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15    | An_rst       | RW SC  | 0x0     | Setting this bit will set all AN registers to their default states. This action also initiate a reset in MMD1 and MMD3. |
| 14    | Reserved     | RO     | 0x0     | Reserved                                                                                                                |
| 13    | Xnp_ctrl     | RW SWC | 0x1     | If mii register4 bit12 is set to 0, setting of this bit shall have no effect.                                           |
| 12    | mii0_an_en   | RW     | 0x0     | 1 = enable Auto-negotiation process.                                                                                    |
| 11:10 | Reserved     | RO     | 0x0     | Reserved                                                                                                                |
| 9     | mii_re_atneg | RW,SC  | 0x0     | 1 = restart Auto-negotiation process.                                                                                   |
| 8:0   | Reserved     | RO     | 0x0     | Reserved                                                                                                                |

---

### 4.3.23. AN Status Register(MMD7,0x1)

**Table 83.AN Status Register(MMD7,0x1)**

| Bit  | Symbol               | Access   | Default | Description                                 |
|------|----------------------|----------|---------|---------------------------------------------|
| 15:8 | Reserved             | RO       | 0x0     | Reserved                                    |
| 7    | Xnp_status           | RO SWC   | 0x0     | AN result of EXTended nEXT page.            |
| 6    | mii_page_rcved       | RO RC LH | 0x0     | 1 = An page has been reveived.              |
| 5    | an_cmplt             | RO       | 0x0     | 1 = Auto-negotiation process has completed. |
| 4    | Remote fault         | RO       | 0x0     | 1 = remote fault condition detect.          |
| 3    | Auto-nego ability    | RO       | 0x1     | always 1.                                   |
| 2    | link_status          | RO LL    | 0x0     | 1 = link up.                                |
| 1    | Reserved             | RO       | 0x0     |                                             |
| 0    | miireg_lp_atneg_able | RO       | 0x0     | Reserved                                    |

---

### 4.3.24. AN advertisement(MMD7,0x10)

**Table 84.AN advertisement(MMD7,0x10)**

| Bit  | Symbol                    | Access | Default | Description                                                                                                                                                |
|------|---------------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | AN advertisement register | RO     | 0x0     | it's a copy of Phy MII 0x4. writes to the AN advertisement register (7.16) cause a write to occur to the Auto-Negotiation advertisement registe (mii 0x4). |

## 4.3.25. AN LP base page ability register(MMD7,0x13)

**Table 85.**AN LP base page ability register(MMD7,0x13)

| Bit  | Symbol            | Access | Default | Description                                 |
|------|-------------------|--------|---------|---------------------------------------------|
| 15:0 | mr_lp_adv_ability | RO     | 0x0     | lp_adv_ability, it's a copy of Phy MII 0x5. |

## 4.3.26. AN XNP transmit1(MMD7,0x16)

**Table 86.**AN XNP transmit1(MMD7,0x16)

| Bit  | Symbol | Access    | Default | Description                                       |
|------|--------|-----------|---------|---------------------------------------------------|
| 15:0 | Xnp_1  | RW<br>SWC | 0x0     | A write to this register set mr_nEXT_page_loaded. |

## 4.3.27. AN XNP transmit2(MMD7,0x17)

**Table 87.**AN XNP transmit2(MMD7,0x17)

| Bit  | Symbol | Access    | Default | Description                                           |
|------|--------|-----------|---------|-------------------------------------------------------|
| 15:0 | Xnp_2  | RW<br>SWC | 0x0     | Bit 31 to 16 of Edxtended nEXT page want to transmit. |

## 4.3.28. AN XNP transmit3(MMD7,0x18)

**Table 88.**AN XNP transmit3(MMD7,0x18)

| Bit  | Symbol | Access    | Default | Description                                           |
|------|--------|-----------|---------|-------------------------------------------------------|
| 15:0 | Xnp_3  | RW<br>SWC | 0x0     | Bit 47 to 32 of Edxtended nEXT page want to transmit. |

## 4.3.29. Multi-GBASE-T AN control 1(MMD7,0x20)

**Table 89.**Multi-GBASE-T AN control 1(MMD7,0x20)

| Bit | Symbol       | Access | Default | Description                                                                                                                    |
|-----|--------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------|
| 15  | an_ms_cfg_en | RW     | 0x0     | 1=Enable MASTER-SLAVE manual configuration<br>0=Disable MASTER-SLAVE manual configuration<br>it's a copy of Phy MII 0x9 bit12. |

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|      |                          |    |     |                                                                                            |
|------|--------------------------|----|-----|--------------------------------------------------------------------------------------------|
| 14   | an_ms_cfg_val            | RW | 0x0 | 1=Configure PHY as MASTER<br>0=Configure PHY as SLAVE<br>it's a copy of Phy MII 0x9 bit11. |
| 13   | an_port_type             | RW | 0x0 | 1=Multiport device<br>0=single-port device<br>it's a copy of Phy MII 0x9 bit10.            |
| 12   | an_10g_abiity            | RW | 0x0 | 1 = Advertise PHY as 10G BASE-T capable.                                                   |
| 11:9 | Reserved                 | RO | 0x0 | Reserved                                                                                   |
| 8    | an_5g_ability            | RW | 0x0 | 1 = Advertise PHY as 5G BASE-T capable.                                                    |
| 7    | an_2p5g_ability          | RW | 0x1 | 1 = Advertise PHY as 2.5G BASE-T capable.                                                  |
| 6    | an_5g_fast_retrain_adv   | RW | 0x0 | 1 = Advertise PHY as 5G BASE-T fast-retrain capable.                                       |
| 5    | an_2p5g_fast_retrain_adv | RW | 0x0 | 1 = Advertise PHY as 2.5G BASE-T fast-retrain capable.                                     |
| 4:1  | Reserved                 | RO | 0x0 | Reserved                                                                                   |
| 0    | an_10g_lptm_ability      | RW | 0x1 |                                                                                            |

### 4.3.30. Multi-GBASE-T AN status 1(MMD7,0x21)

**Table 90.**Multi-GBASE-T AN status 1(MMD7,0x21)

| Bit | Symbol                       | Access      | Default | Description                                                     |
|-----|------------------------------|-------------|---------|-----------------------------------------------------------------|
| 15  | an_ms_cfg_fault_latch        | RO LH<br>RC | 0x0     | 1 = master slave cfg fault has detetcted.                       |
| 14  | an_ms_cfg_res                | RO          | 0x0     | 1 = Loc phy cfg reserved to MASTER.                             |
| 13  | loc_rcv_status               | RO          | 0x0     | 1 = Loc receiver OK.                                            |
| 12  | rem_rcv_status               | RO          | 0x0     | 1 = Remote receiver OK.                                         |
| 11  | lp_tenge_cap                 | RO          | 0x0     | Reserved                                                        |
| 10  | lp_loop_timing_ability       | RO          | 0x0     | 1 = Link partner is capable of loop-timing.                     |
| 9:7 | Reserved                     | RO          | 0x0     | Reserved                                                        |
| 6   | lp_5g_cap                    | RO          | 0x0     | 1 = link partner is able to operate as 5GBASE-T.                |
| 5   | lp_2p5g_cap                  | RO          | 0x0     | 1 = link partner is able to operate as 2.5GBASE-T.              |
| 4   | lp_5g_fast_retrain_cap       | RO          | 0x0     | 1 = link partner is able to operate as 5GBASE-T fast retrain.   |
| 3   | lp_2p5g_fast_retrain_ca<br>p | RO          | 0x0     | 1 = link partner is able to operate as 2.5GBASE-T fast retrain. |
| 2:0 | Reserved                     | RO          | 0x0     | Reserved                                                        |

## 4.3.31. Local Device EEE Ability 1(MMD7,0x3C)

**Table 91.**Local Device EEE Ability1(MMD7,0x3C)

| Bit  | Symbol      | Access | Default | Description                                             |
|------|-------------|--------|---------|---------------------------------------------------------|
| 15:7 | Reserved    | RO     | 0x0     | Reserved                                                |
| 6    | EEE_10GKR   | RW     | 0x0     | 1 = Advertise that the 10GBASE-KR has EEE capability.   |
| 5    | EEE_1000KX4 | RW     | 0x0     | 1 = Advertise that the 1000BASE-KX4 has EEE capability. |
| 4    | EEE_1000KX  | RW     | 0x0     | 1 = Advertise that the 10GBASE-KX has EEE capability.   |
| 3    | EEE_10GBT   | RW     | 0x0     | 1 = Advertise that the 10GBASE-T has EEE capability.    |
| 2    | EEE_1000BT  | RW     | 0x0     | PHY's 1000BT EEE ability.                               |
| 1    | EEE_100BT   | RW     | 0x0     | PHY's 100BT EEE ability.                                |
| 0    | Reserved    | RO     | 0x0     | Reserved                                                |

## 4.3.32. Link Partner EEE Ability1(MMD7,0x3D)

**Table 92.**Link Partner EEE Ability1(MMD7,0x3D)

| Bit  | Symbol            | Access | Default | Description |
|------|-------------------|--------|---------|-------------|
| 15:4 | Reserved          | RO     | 0x0     |             |
| 3:1  | lp_ge_eee_ability | RO     | 0x0     |             |
| 0    | Reserved          | RO     | 0x0     | Reserved    |

## 4.3.33. Local Device EEE Ability 2(MMD7,0x3E)

**Table 93.**Local Device EEE Ability2(MMD7,0x3E)

| Bit  | Symbol       | Access | Default | Description                                           |
|------|--------------|--------|---------|-------------------------------------------------------|
| 15:2 | Reserved     | RO     | 0x0     | Reserved                                              |
| 1    | EEE_5G_CAP   | RW     | 0x0     | 1 = Advertise that the 5GBASE-T has EEE capability.   |
| 0    | EEE_2P5G_CAP | RW     | 0x0     | 1 = Advertise that the 2.5GBASE-T has EEE capability. |

## 4.3.34. Link Partner EEE Ability2(MMD7,0x3F)

**Table 94.**Link Partner EEE Ability2(MMD7,0x3F)

| Bit  | Symbol             | Access | Default | Description                                                                                                                                          |
|------|--------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | Reserved           | RO     | 0x0     | Reserved                                                                                                                                             |
| 1:0  | lp_eee_adv_ability | RO     | 0x0     | 1 = Link partner is advertising that the 2.5GBASE-T has EEE capability<br>0 = Link partner is not advertising that the 2.5GBASE-T has EEE capability |

## 4.3.35. MultiGBASE-T AN control 2(MMD7,0x40)

**Table 95.**MultiGBASE-T AN control 2(MMD7,0x40)

| Bit  | Symbol                        | Access | Default | Description                                                                     |
|------|-------------------------------|--------|---------|---------------------------------------------------------------------------------|
| 15:4 | Reserved                      | RO     | 0x0     | Reserved                                                                        |
| 3    | 2.5GBASE-T THP Bypass Request | RW     | 0x1     | Link partner requests local devices to initially reset THP during fast retrain. |
| 2    | 5GBASE-T THP Bypass Request   | RW     | 0x1     |                                                                                 |
| 1:0  | Reserved                      | RO     | 0x0     | Reserved                                                                        |

## 4.3.36. Multi-GBASE-T AN status 2(MMD7,0x41)

**Table 96.**Multi-GBASE-T AN status 2(MMD7,0x41)

| Bit  | Symbol                                     | Access | Default | Description                                                                                                                                                               |
|------|--------------------------------------------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | Reserved                                   | RO     | 0x0     | Reserved                                                                                                                                                                  |
| 3    | 2.5GBASE-T Link Partner THP Bypass Request | RO     | 0x0     | 1 = Link partner requests local device to initially reset THP during fast retrain<br>0= Link partner requests local device not to initially reset THP during fast retrain |
| 2:0  | 5GBASE-T Link Partner THP Bypass Request   | RO     | 0x0     | Reserved                                                                                                                                                                  |

## 4.4. Common EXT Register

### 4.4.1. SMI mux (0xA000)

Table 97. SMI mux (0xA000)

| Bit  | Symbol      | Access | Default | Description                                                                               |
|------|-------------|--------|---------|-------------------------------------------------------------------------------------------|
| 15:3 | Reserved    | RO     | 0x0     | Reserved                                                                                  |
| 1    | Smi_sds_phy | RW     | 0x0     | to control access whether phy register or sds register. 1 to access sds; 0 to access phy. |
| 0    | smi_sf      | RO     | 0x0     | always 0.                                                                                 |

### 4.4.2. Mode\_Sel(0xA001)

Table 98. Mode\_Sel(0xA001)

| Bit  | Symbol            | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-------------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | mode_change_rst_n | RW SC  | 0x1     | 0 = to reset whole chip's FSMs and data paths, except the register table. It's self-clear.                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 14   | bridge_sw_reset   | RW     | 0x0     | 1 = to reset the bridge between UTP and SerDes.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 13   | Reserved          | RW     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 12   | reserved          | RW     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11   | Reserved          | RW     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 10:3 | Reserved          | RO     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2:0  | mode_sel          | RW     | 0x0     | chip working mode selection.<br>000 = AUTO_BX2500_SGMII,<br>001 = FORCE_BX2500,<br>101 = UTP_TO_FIBER_FORCE<br>In AUTO_BX2500_SGMII mode, SerDes speed is determined by UTP, if UTP link up at 2.5GBASE-T, SerDes will work as 2500BASE-X, if UTP link up at 1000BASE-T/100BASE-Tx/10BASE-T, SerDes will work as SGMII, if UTP link down, SerDes will be power down or not which is controled by EXT 0xA002 bit13. The internal flow control buffer is disabled in this mode.<br><br>In FORCE_BX2500, SerDes always works as 2500BASE-X, internal flow control buffer |

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|  |  |  |  |                                                                                                                                                                       |
|--|--|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  |  |  | <p>will be activated if UTP doesn't work at 2.5GBASE-T.</p> <p>In UTP_TO_FIBER_FORCE mode, user should manually control the SerDes speed to align with UTP speed.</p> |
|--|--|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### 4.4.3. MDIO\_address\_ctrl (0xA005)

Table 99. MDIO\_address\_ctrl(0xA005)

| Bit   | Symbol               | Access | Default | Description              |
|-------|----------------------|--------|---------|--------------------------|
| 15:11 | Reserved             | RO     | 0x0     | always 0.                |
| 10    | Bypass_mdio_watchdog | RW     | 0x0     | bypass mdio watch dog    |
| 9:8   | Reserved             | RO     | 0x0     | Reserved                 |
| 7     | reserved             | RW     | 0x1     | Reserved                 |
| 6     | En_phyaddr0          | RW     | 0x1     | enable phyaddr0          |
| 5     | En_bdcst_addr        | RW     | 0x0     | enable broadcast address |
| 4:0   | Bdcst_addr           | RW     | 0x0     | broadcast address        |

### 4.4.4. SYNCE0 cfg(0xA006)

Table 100. SYNCE0 cfg (0xA006)

| Bit  | Symbol            | Access | Default | Description                                                                                                                                  |
|------|-------------------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | reserved          | RW     | 0x0     | Reserved                                                                                                                                     |
| 8    | Reserved          | RO     | 0x0     | always 0.                                                                                                                                    |
| 7    | jumbo_enable      | RW     | 0x0     | enable jumbo frame                                                                                                                           |
| 6    | rem_lpbk_sds      | RW     | 0x0     | set remote loopback for sds                                                                                                                  |
| 5    | rem_lpbk_phy      | RW     | 0x0     | set remote loopback for phy                                                                                                                  |
| 4    | uldata_loopback   | RW     | 0x0     | 1=remain upload data when rem lpbk is set for phy or sds                                                                                     |
| 3    | Reserved          | RW     | 0x1     | Reserved                                                                                                                                     |
| 2    | Reserved          | RO     | 0x0     | always 0.                                                                                                                                    |
| 1:0  | fib_speed_sel_reg | RW     | 0x2     | Valid when EXT 0xA001.2:0 is 101 (UTP_TO_FIBER_FORCE). To select the SerDes working speed. 10 = 2500BASE-X, 01 = 1000BASE-X, 00 = 100BASE-FX |

### 4.4.5. MAC\_ADDRESS (0xA007)

Table 101. MAC\_ADDRESS (0xA007)

| Bit | Symbol | Access | Default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|

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|      |                     |    |     |                                              |
|------|---------------------|----|-----|----------------------------------------------|
| 15:0 | mac_addr_loc[47:32] | RW | 0x0 | highest 16 bits for mac address used for wol |
|------|---------------------|----|-----|----------------------------------------------|

### 4.4.6. MAC\_ADDRESS (0xA008)

Table 102. MAC\_ADDRESS (0xA008)

| Bit  | Symbol              | Access | Default | Description                                 |
|------|---------------------|--------|---------|---------------------------------------------|
| 15:0 | mac_addr_loc[31:16] | RW     | 0x0     | middle 16 bits for mac address used for wol |

### 4.4.7. MAC\_ADDRESS (0xA009)

Table 103. MAC\_ADDRESS (0xA009)

| Bit  | Symbol             | Access | Default | Description                                 |
|------|--------------------|--------|---------|---------------------------------------------|
| 15:0 | mac_addr_loc[15:0] | RW     | 0x0     | lowest 16 bits for mac address used for wol |

### 4.4.8. Interrupt control (0xA00A)

Table 104. Interrupt control (0xA00A)

| Bit  | Symbol        | Access | Default | Description                                                                                                                                                                                                                    |
|------|---------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | Reserved      | RO     | 0x0     | always 0.                                                                                                                                                                                                                      |
| 6    | pmeb_intb_sel | RW     | 0x0     | select the source that driven INT_N pin. 1 = INT_N is driven by WOL interrupt;<br>0 = INT_N is driven by legacy interrupt, including PHY/SerDes link up/down interrupt.                                                        |
| 5:4  | Reserved      | RO     | 0x0     | always 0.                                                                                                                                                                                                                      |
| 3    | wol_en        | RW     | 0x0     | enable wol                                                                                                                                                                                                                     |
| 2:0  | wol_lth_sel   | RW     | 0x2     | bit0,1: WOL interrupt is pulse triggered and active low;0: WOL interrupt is level triggered and active_low.<br>Bit2:1,valid when bit0 is 1, to control the pulse width.<br>00: 84ms;<br>01: 168ms;<br>10: 336ms;<br>11: 672ms. |

### 4.4.9. LED common control (0xA00B)

Table 105. LED common control (0xA00B)

| Bit | Symbol      | Access | Default | Description                             |
|-----|-------------|--------|---------|-----------------------------------------|
| 15  | col_blk_sel | RW     | 0x1     | 1 = when collision happens, and related |

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|      |                  |        |     |                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                  |        |     | <p>LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 1, LED blink at Blink Mode2;</p> <p>0 = when collision happens, and related LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 1, LED blink at Blink Mode1.</p> <p>LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.</p> |
| 14   | jabber_led_dis   | RW POS | 0x1 | 1 = when 10Mb/s Jabber happens, LED will not blink;                                                                                                                                                                                                                                                                                                                        |
| 13   | lpbk_led_dis     | RW POS | 0x1 | 1 = In internal loopback mode, LED will not blink;                                                                                                                                                                                                                                                                                                                         |
| 12   | dis_led_an_try   | RW     | 0x0 | 1: LED will be ON when auto-negotiation is at LINK_GOOD_CHECK status, in which status, the link is not up already.                                                                                                                                                                                                                                                         |
| 11:9 | Reserved         | RW     | 0x0 | always 0.                                                                                                                                                                                                                                                                                                                                                                  |
| 8    | Led_2_force_en   | RW     | 0x0 | 1 = enable LED2 force mode.                                                                                                                                                                                                                                                                                                                                                |
| 7:6  | Led_2_force_mode | RW     | 0x0 | <p>Valid when bit8 is set.</p> <p>00: force LED OFF;</p> <p>01: force LED ON;</p> <p>10: force LED Blink at Blink Mode1; 11: force LED Blink at Blink Mode2.</p> <p>LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.</p>                                                                |
| 5    | Led_1_force_en   | RW     | 0x0 | 1 = enable LED1 force mode.                                                                                                                                                                                                                                                                                                                                                |
| 4:3  | Led_1_force_mode | RW     | 0x0 | <p>Valid when bit5 is set.</p> <p>Refer EXT A00B[7:6] for the force mode description.</p>                                                                                                                                                                                                                                                                                  |
| 2    | Led_0_force_en   | RW     | 0x0 | 1 = enable LED0 force mode.                                                                                                                                                                                                                                                                                                                                                |
| 1:0  | Led_0_force_mode | RW     | 0x0 | <p>Valid when bit5 is set.</p> <p>Refer EXT A00B[7:6] for the force mode description.</p>                                                                                                                                                                                                                                                                                  |

### 4.4.10. LED0 control (0xA00C)

Table 106. LED0 control (0xA00C)

| Bit | Symbol | Access | Default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|

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|    |                    |    |     |                                                                                                                                                 |
|----|--------------------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15 | Led_2500_on_en_1   | RW | 0x0 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 2500Base-T, make LED0 ON;                                              |
| 14 | Led_2500_blk_en_1  | RW | 0x0 | 1 = if PHY link up and speed mode is 2500Base-T, make LED0 BLINK;                                                                               |
| 13 | Led_act_blk_ind_1  | RW | 0x0 | When traffic is present, make LED0 BLINK no matter the previous LED0 status is ON or OFF, or make LED0 blink only when the previous LED0 is ON. |
| 12 | Led_fdx_on_en_1    | RW | 0x0 | 1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.                                          |
| 11 | Led_hdx_on_en_1    | RW | 0x0 | If BLINK status is not activated, when PHY link up and duplex mode is half duplex,                                                              |
| 10 | Led_txact_blk_en_1 | RW | 0x1 | 1: If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active,                     |
| 9  | Led_rxact_blk_en_1 | RW | 0x1 | If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active,                        |
| 8  | Led_txact_on_en_1  | RW | 0x0 | 1 = if BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms;                                            |
| 7  | Led_rxact_on_en_1  | RW | 0x0 | 1 = if BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms;                                            |
| 6  | Led_gt_on_en_1     | RW | 0x0 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 1000Base-T, make LED0 ON;                                              |
| 5  | Led_ht_on_en_1     | RW | 0x1 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 100Base_TX, make LED0 ON;                                              |
| 4  | Led_bt_on_en_1     | RW | 0x1 | 1 = if BLINK status is not activated, when PHY link up and speed mode is 10Base-T, make LED0 ON;                                                |
| 3  | Led_col_blk_en_1   | RW | 0x0 | 1 = if PHY link up and collision happen, make LED0 BLINK;                                                                                       |
| 2  | Led_gt_blk_en_1    | RW | 0x0 | 1 = if PHY link up and speed mode is 1000Base-T, make LED0 BLINK;                                                                               |
| 1  | Led_ht_blk_en_1    | RW | 0x0 | 1 = if PHY link up and speed mode is 100Base-T, make LED0 BLINK;                                                                                |
| 0  | Led_bt_blk_en_1    | RW | 0x0 | 1 = if PHY link up and speed mode is                                                                                                            |

|  |  |  |  |                                          |
|--|--|--|--|------------------------------------------|
|  |  |  |  | 10Base-T <sub>e</sub> , make LED0 BLINK; |
|--|--|--|--|------------------------------------------|

#### 4.4.11. LED1 control (0xA00D)

Table 107. LED1 control (0xA00D)

| Bit | Symbol             | Access | Default | Description                                    |
|-----|--------------------|--------|---------|------------------------------------------------|
| 15  | Led_2500_on_en_2   | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 14  | Led_2500_blk_en_2  | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 13  | Led_act_blk_ind_2  | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 12  | Led_fdx_on_en_2    | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 11  | Led_hdx_on_en_2    | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 10  | Led_txact_blk_en_2 | RW     | 0x1     | LED1 control, with same logic as LED0 control. |
| 9   | Led_rxact_blk_en_2 | RW     | 0x1     | LED1 control, with same logic as LED0 control. |
| 8   | Led_txact_on_en_2  | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 7   | Led_rxact_on_en_2  | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 6   | Led_gt_on_en_2     | RW     | 0x1     | LED1 control, with same logic as LED0 control. |
| 5   | Led_ht_on_en_2     | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 4   | Led_bt_on_en_2     | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 3   | Led_col_blk_en_2   | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 2   | Led_gt_blk_en_2    | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 1   | Led_ht_blk_en_2    | RW     | 0x0     | LED1 control, with same logic as LED0 control. |
| 0   | Led_bt_blk_en_2    | RW     | 0x0     | LED1 control, with same logic as LED0 control. |

#### 4.4.12. LED2 control (0xA00E)

Table 108. LED2 control (0xA00E)

| Bit | Symbol             | Access | Default | Description                                    |
|-----|--------------------|--------|---------|------------------------------------------------|
| 15  | Led_2500_on_en_3   | RW     | 0x1     | LED2 control, with same logic as LED0 control. |
| 14  | Led_2500_blk_en_3  | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 13  | Led_act_blk_ind_3  | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 12  | Led_fdx_on_en_3    | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 11  | Led_hdx_on_en_3    | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 10  | Led_txact_blk_en_3 | RW     | 0x1     | LED2 control, with same logic as LED0 control. |
| 9   | Led_rxact_blk_en_3 | RW     | 0x1     | LED2 control, with same logic as LED0 control. |
| 8   | Led_txact_on_en_3  | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 7   | Led_rxact_on_en_3  | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 6   | Led_gt_on_en_3     | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 5   | Led_ht_on_en_3     | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 4   | Led_bt_on_en_3     | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 3   | Led_col_blk_en_3   | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 2   | Led_gt_blk_en_3    | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 1   | Led_ht_blk_en_3    | RW     | 0x0     | LED2 control, with same logic as LED0 control. |
| 0   | Led_bt_blk_en_3    | RW     | 0x0     | LED2 control, with same logic as LED0 control. |

## 4.4.13. LED src sel (0xA00F)

Table 109. LED src sel (0xA00F)

| Bit   | Symbol        | Access | Default | Description                                                                                                                                         |
|-------|---------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | led_3_src_sel | RW     | 0x0     | 00=control LED2 by UTP's status;<br>01=control LED2 by SerDes' status;<br>10=control EEDs by both UTP's and SerDes' status; 11=when UTP is enabled, |

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|       |               |    |     |                                                                                                                                                                                                                                                             |
|-------|---------------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |               |    |     | control LED2 by UTP's status, otherwise by SerDes'.                                                                                                                                                                                                         |
| 13:12 | led_2_src_sel | RW | 0x0 | same logic as led_3_src_sel                                                                                                                                                                                                                                 |
| 11:10 | led_1_src_sel | RW | 0x0 | same logic as led_3_src_sel                                                                                                                                                                                                                                 |
| 9:7   | Reserved      | RO | 0x0 | always 0.                                                                                                                                                                                                                                                   |
| 6:4   | led_duty      | RW | 0x0 | Select duty cycle of Blink: 000:<br>50% ON and 50% OFF;<br>001: 67% ON and 33% OFF;<br>010: 75% ON and 25% OFF;<br>011: 83% ON and 17% OFF;<br>100: 50% ON and 50% OFF;<br>101: 33% ON and 67% OFF;<br>110: 25% ON and 75% OFF;<br>111: 17% ON and 83% OFF. |
| 3:2   | led_freq2     | RW | 0x1 | Select frequency of Blink Mode2: 00:<br>2Hz;<br>01: 4Hz;<br>10: 8Hz;<br>11: 16Hz.                                                                                                                                                                           |
| 1:0   | led_freq1     | RW | 0x2 | Select frequency of Blink Mode1: 00:<br>2Hz;<br>01: 4Hz;<br>10: 8Hz;<br>11: 16Hz.                                                                                                                                                                           |

### 4.4.14. SyncE control (0xA012)

Table 110. SYNCE Control (0xA012)

| Bit  | Symbol                   | Access | Default | Description                                                                                    |
|------|--------------------------|--------|---------|------------------------------------------------------------------------------------------------|
| 15:9 | Reserved                 | RO     | 0x0     | always 0.                                                                                      |
| 8    | en_sync_e_reg            | RW     | 0x0     | SyncE 输出时钟使能。<br>0 : 关闭 , PAD 高阻 ;<br>1 : 有效 , 可以选择时钟输出。                                       |
| 7    | en_sync_e_during_lnkdown | RW     | 0x0     | 1 = always output SyncE clock even when link is down; 0 = close SyncE clock when link is down. |
| 6:4  | Reserved                 | RW     | 0x0     |                                                                                                |
| 3    | clk_sel                  | RW     | 0x0     | Clock frequency select<br>0: 25MHz<br>1 : 125MHz                                               |
| 2:1  | clk_src_sel              | RW     | 0x3     | SyncE circuit input clock selection                                                            |

|   |          |    |     |                                                                                                                  |
|---|----------|----|-----|------------------------------------------------------------------------------------------------------------------|
|   |          |    |     | 2'b00 : 选择 PHY 恢复的 RX 时钟<br>2'b01 : 选择 PHY 的 VCO 时钟<br>2'b10 : 选择 xtal 的 25M 参考时钟<br>2'b11 : 选择 Serdes 恢复的 RX 时钟 |
| 0 | Reserved | RW | 0x0 | Reserved                                                                                                         |

#### 4.4.15. SPI flash load control and status (0xA030)

Table 111. SPI flash load control and status (0xA030)

| Bit  | Symbol           | Access | Default | Description                                                                                                                                                                                           |
|------|------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | spif_flag_bytes  | RO     | 0x0     | the flag Byte read out from the SPI flash.                                                                                                                                                            |
| 7:5  | spif_load_status | RO     | 0x0     | valid when bit4 is 1.<br>000 = LOAD_SUCCESS,<br>001 = CHIP_ID_ERR,<br>010 = CHIP_VER_ERR,<br>011 = LOAD_CFG_ERR,<br>100 = CHKSUM_ERR,<br>101 = PARITY_ERR,<br>110 = TIMEOUT_ERR,<br>111 = PHYADD_ERR. |
| 4    | spif_done_status | RO     | 0x0     | 1 = SPI flash data load is done                                                                                                                                                                       |
| 3:1  | Reserved         | RO     | 0x0     | always 0.                                                                                                                                                                                             |
| 0    | spif_restart     | RW SC  | 0x0     | 1 = to load SPI flash data manually. It's self-cleared                                                                                                                                                |

#### 4.4.16. SPI flash load status2 (0xA031)

Table 112. SPI flash load status2(0xA031)

| Bit  | Symbol         | Access | Default | Description                                   |
|------|----------------|--------|---------|-----------------------------------------------|
| 15:0 | spif_ld_ok_cnt | RO     | 0x0     | the counter of successfully loaded registers. |

#### 4.4.17. SPI flash load status3 (0xA032)

Table 113. SPI flash load status3(0xA032)

| Bit  | Symbol       | Access | Default | Description                             |
|------|--------------|--------|---------|-----------------------------------------|
| 15:0 | spif_chip_id | RO     | 0x0     | the chip ID read out from the SPI flash |

#### 4.4.18. SPI flash load status4 (0xA033)

Table 114. SPI flash load status4(0xA033)

| Bit | Symbol | Access | Default | Description |
|-----|--------|--------|---------|-------------|
|-----|--------|--------|---------|-------------|

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|      |               |    |     |                                                  |
|------|---------------|----|-----|--------------------------------------------------|
| 15:8 | spif_chip_ver | RO | 0x0 | the chip version read out from the SPI flash     |
| 7:0  | spif_fw_ver   | RO | 0x0 | the firmware version read out from the SPI flash |

### 4.4.19. Manu\_hw\_rst (0xA0C0)

Table 115. Manu\_hw\_rst (0xA0C0)

| Bit  | Symbol      | Access | Default | Description                                                          |
|------|-------------|--------|---------|----------------------------------------------------------------------|
| 15   | manu_hw_rst | RW SC  | 0x0     | 1 = reset whole chip's FSM and data path, except the register space. |
| 14:0 | reserved    | RO     | 0x0     | Reserved                                                             |

### 4.4.20. Hw\_reserved (0xA0FF)

Table 116. Hw\_reserved (0xA0FF)

| Bit  | Symbol      | Access | Default | Description |
|------|-------------|--------|---------|-------------|
| 15:0 | hw_reserved | RW     | 0x5555  | reserved    |

## 4.5. Sds MII Register

### 4.5.1. Basic control register (0x00)

Table 117. Basic control register (0x00)

| Bit | Symbol               | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                                |
|-----|----------------------|--------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | Reset                | RW SC  | 0x0     | PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.                                                                                                                                                                                                                                       |
| 14  | Loopback             | RW     | 0x0     | Internal loopback control                                                                                                                                                                                                                                                                                                                                                  |
| 13  | Speed_Selection(LSB) | RW     | 0x0     | LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero and serdes is working at SGMII_MAC mode.<br>Refer to SDS MII 0x12 bit2:0 for serdes working mode, and SDS MII 0x11 bit15:14. |
| 12  | Autoneg_En           | RW     | 0x1     | 1: to enable auto-negotiation;                                                                                                                                                                                                                                                                                                                                             |
| 11  | Power_down           | RW     | 0x0     | 1 = Power down                                                                                                                                                                                                                                                                                                                                                             |

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|     |                      |       |     |                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------|-------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | Isolate              | RW    | 0x0 | Isolate phy from RGMII/SGMII/FIBER.                                                                                                                                                                                                                                                                                                                                                        |
| 9   | Re_Autoneg           | RW SC | 0x0 | Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART.                                                                                                                                                                                                                                                                                     |
| 8   | Duplex_Mode          | RW    | 0x1 | The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.                                                                                                                                                                         |
| 7   | Collision_Test       | RW    | 0x0 | Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.                                                                                                                                                                                                                                                                                                 |
| 6   | Speed_Selection(MSB) | RW    | 0x1 | See bit13.                                                                                                                                                                                                                                                                                                                                                                                 |
| 5   | mr_unidirectional    | RW    | 0x0 | When bit 0.12 is one or bit 0.8 is zero, this bit is ignored.<br><br>When bit 0.12 is zero and bit 0.8 is one:<br>1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established<br>0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established |
| 4:0 | Reserved             | RO    | 0x0 | Reserved. Write as 0, ignore on read                                                                                                                                                                                                                                                                                                                                                       |

### 4.5.2. Basic status register (0x01)

Table 118. Basic status register (0x01)

| Bit | Symbol            | Access | Default | Description                                                                       |
|-----|-------------------|--------|---------|-----------------------------------------------------------------------------------|
| 15  | 100Base-T4        | RO     | 0x0     | PHY doesn't support 100BASE-T4                                                    |
| 14  | 100Base-X_Fd      | RO     | 0x1     | PHY supports 100BASE-X_FD                                                         |
| 13  | 100Base-X_Hd      | RO     | 0x0     | PHY supports 100BASE-X_HD                                                         |
| 12  | 10Mbps_Fd         | RO     | 0x0     | PHY supports 10Mbps_Fd                                                            |
| 11  | 10Mbps_Hd         | RO     | 0x0     | PHY supports 10Mbps_Hd                                                            |
| 10  | 100Base-T2_Fd     | RO     | 0x0     | PHY doesn't support 100Base-T2_Fd                                                 |
| 9   | 100Base-T2_Hd     | RO     | 0x0     | PHY doesn't support 100Base-T2_Hd                                                 |
| 8   | Extended_Status   | RO     | 0x1     | Whether support EXTended status register in 0Fh                                   |
| 7   | Unidirect_Ability | RO     | 0x1     | 1'b0: PHY able to transmit from MII only when the PHY has determined that a valid |

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|   |                         |              |     |                                                                                                           |
|---|-------------------------|--------------|-----|-----------------------------------------------------------------------------------------------------------|
|   |                         |              |     | link has been established                                                                                 |
| 6 | Mf_Preamble_Suppression | RO           | 0x1 | 1'b0: PHY will not accept management frames with preamble suppressed                                      |
| 5 | Autoneg_Complete        | RO           | 0x0 | 1'b0: Auto-negotiation process not completed                                                              |
| 4 | Remote_Fault            | RO RC SWC LH | 0x0 | 1'b0: no remote fault condition detected                                                                  |
| 3 | Autoneg_Ability         | RO           | 0x1 | 1'b0: PHY not able to perform Auto-negotiation                                                            |
| 2 | Link_Status             | RO SWC LL    | 0x0 | Link status                                                                                               |
| 1 | Jabber_Detect           | RO           | 0x0 | always 0                                                                                                  |
| 0 | Extended_Capability     | RO           | 0x1 | To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh |

### 4.5.3. Sds identification register1 (0x02)

Table 119. Sds identification register1 (0x02)

| Bit  | Symbol | Access | Default | Description                                            |
|------|--------|--------|---------|--------------------------------------------------------|
| 15:0 | Phy_Id | RO     | 0x4f51  | Bits 3 to 18 of the Organizationally Unique Identifier |

### 4.5.4. Sds identification register2 (0x03)

Table 120. Sds identification register2 (0x03)

| Bit   | Symbol      | Access | Default | Description                                             |
|-------|-------------|--------|---------|---------------------------------------------------------|
| 15:10 | Phy_Id      | RO     | 0x3a    | Bits 19 to 24 of the Organizationally Unique Identifier |
| 9:4   | Type_No     | RO     | 0x9     | 6 bits manufacturer's type number                       |
| 3:0   | Revision_No | RO     | 0x9     | 4 bits manufacturer's revision number                   |

### 4.5.5. Auto-Negotiation advertisement (0x04)

Table 121. Auto-Negotiation advertisement (0x04)

| Bit | Symbol    | Access | Default | Description                                                                                                                                    |
|-----|-----------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | NEXT_Page | RW     | 0x0     | This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: |
| 14  | Ack       | RO     | 0x0     | Always 0                                                                                                                                       |

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|       |                  |    |     |                                                                                                                                                |
|-------|------------------|----|-----|------------------------------------------------------------------------------------------------------------------------------------------------|
| 13:12 | Remote_Fault     | RO | 0x0 | Always 0                                                                                                                                       |
| 11:9  | Reserved         | RO | 0x0 | Reserved                                                                                                                                       |
| 8     | Asymmetric_Pause | RW | 0x1 | This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: |
| 7     | Pause            | RW | 0x1 | This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: |
| 6     | Half_duplex      | RW | 0x0 | Half duplex ability                                                                                                                            |
| 5     | Full_duplex      | RW | 0x1 | Full duplex ability                                                                                                                            |
| 4:0   | Reserved         | RO | 0x0 | Reserved                                                                                                                                       |

### 4.5.6. Auto-Negotiation link partner ability (0x05)

Table 122. Auto-Negotiation link partner ability when link partner is 1000BASE-X or 2500BASE-X(0x05)

| Bit   | Symbol       | Access | Default | Description                                |
|-------|--------------|--------|---------|--------------------------------------------|
| 15    | NEXT Page    | RO SWC | 0x0     | NEXT page. Received Code Word Bit 15       |
| 14    | ACK          | RO SWC | 0x0     | Acknowledge. Received Code Word Bit 14     |
| 13:12 | REMOTE_FAULT | RO SWC | 0x0     | Remote Fault. Received Code Word Bit 13:12 |
| 11:9  | RESERVED     | RO     | 0x0     | Reserved. Received Code Word Bit 11:9      |
| 8:7   | PAUSE        | RO SWC | 0x0     | Pause. Received Code Word Bit 8:7          |
| 6     | HALF_DUPLEX  | RO SWC | 0x0     | Half duplex. Received Code Word Bit 6      |
| 5     | FULL_DUPLEX  | RO SWC | 0x0     | Full duplex. Received Code Word Bit 5      |
| 4:0   | RESERVED     | RO     | 0x0     | Reserved. Received Code Word Bit 4:0       |

Table Auto-Negotiation link partner ability when link partner is SGMII\_MAC (0x05)

| Bit  | Symbol   | Access | Default | Description                            |
|------|----------|--------|---------|----------------------------------------|
| 15   | Reserved | RO SWC | 0x0     | Reserved. Received Code Word Bit 15    |
| 14   | ACK      | RO SWC | 0x0     | Acknowledge. Received Code Word Bit 14 |
| 13:1 | Reserved | RO SWC | 0x0     | Reserved. Received Code Word Bit 13:1  |
| 0    | RESERVED | RO     | 0x1     | Reserved. Received Code Word Bit 0     |

Table Auto-Negotiation link partner ability when link partner is SGMII\_PHY (0x05)

| Bit | Symbol   | Access | Default | Description                                         |
|-----|----------|--------|---------|-----------------------------------------------------|
| 15  | PHY link | RO SWC | 0x0     | Link partner link status. Received Code Word Bit 15 |
| 14  | ACK      | RO SWC | 0x0     | Acknowledge. Received Code Word Bit 14              |
| 13  | Reserved | RO SWC | 0x0     | Reserved. Received Code Word Bit 13                 |

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|       |             |        |     |                                                       |
|-------|-------------|--------|-----|-------------------------------------------------------|
| 12    | Duplex mode | RO SWC | 0x0 | Link Partner duplex mode. Received Code Word Bit 12   |
| 11:10 | Speed       | RO     | 0x0 | Link partner speed mode, Received Code Word Bit 11:10 |
| 9:1   | Reserved    | RO SWC | 0x0 | Reserved. Received Code Word Bit 9:1                  |
| 0     | RESERVED    | RO     | 0x1 | Reserved. Received Code Word Bit 0                    |

### 4.5.7. Auto-Negotiation expansion register (0x06)

Table 123. Auto-Negotiation expansion register (0x06)

| Bit  | Symbol               | Access      | Default | Description                         |
|------|----------------------|-------------|---------|-------------------------------------|
| 15:3 | Reserved             | RO          | 0x0     | Reserved                            |
| 2    | Local NEXT Page able | RO          | 0x0     | 1 = Local Device supports NEXT Page |
| 1    | Page received        | RO RC<br>LH | 0x0     | 1 = A new page is received          |
| 0    | Reserved             | RO          | 0x0     | Reserved                            |

### 4.5.8. Auto-Negotiation NEXT Page register (0x07)

Table 124. Auto-Negotiation NEXT Page register (0x07)

| Bit  | Symbol    | Access | Default | Description |
|------|-----------|--------|---------|-------------|
| 15:0 | NEXT Page | RO     | 0x0     | always be 0 |

### 4.5.9. Auto-Negotiation link partner Received NEXT Page register (0x08)

Table 125. Auto-Negotiation link partner Received NEXT Page register (0x08)

| Bit  | Symbol                 | Access | Default | Description |
|------|------------------------|--------|---------|-------------|
| 15:0 | Link Partner NEXT Page | RO     | 0x0     | always be 0 |

### 4.5.10. Extended status register (0x0F)

Table 126. Extended status register (0x0F)

| Bit  | Symbol                 | Access | Default | Description                              |
|------|------------------------|--------|---------|------------------------------------------|
| 15   | 1000BASE-X Full Duplex | RO     | 0x1     | 1 = PHY supports 1000BASE-X Full Duplex  |
| 14   | 1000BASE-X Half Duplex | RO     | 0x0     | 1 = PHY supports 1000BASE-X Half Duplex. |
| 13   | 1000BASE-T Full Duplex | RO     | 0x0     | 1 = PHY supports 1000BASE-T Full Duplex  |
| 12   | 1000BASE-T Half Duplex | RO     | 0x0     | 1 = PHY supports 1000BASE-T Half Duplex  |
| 11:0 | Reserved               | RO     | 0x0     | Always 0                                 |

## 4.5.11. Sds specific status register (0x11)

Table 127. Sds specific status register (0x11)

| Bit   | Symbol                | Access | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-----------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | Speed_mode[1:0]       | RO     | 0x0     | Lowest 2bits of speed_mode[2:0]<br>When SerDes works as SGMII MAC, if Auto-Negotiation is enabled, the speed_mode is sourced from Auto-Negotiation process with SGMII PHY, otherwise, it's {1'b0, SDS MII 0x0 Speed_Selection[1:0]};<br>When SerDes works as SGMII PHY, it equals to the UTP speed mode;<br>When SerDes works as 100BASE-FX, it equals to 001;<br>When SerDes works as 1000BASE-X, it equals to 010;<br>When SerDes works as 2500BASE-X, it equals to 100;<br>Refer to SDS MII 0x12 bit2:0 for SerDes' working mode. |
| 13    | Duplex                | RO     | 0x0     | This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 12:11 | Pause                 | RO     | 0x0     | Pause to mac                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 10    | Link status real-time | RO     | 0x0     | 1 = Link up                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | Speed_mode[2]         | RO     | 0x0     | MSB of speed_mode[2:0].<br>Refer to bit15:14.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 8     | Duplex_error          | RO     | 0x0     | realtime duplex error                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7     | En_flowctrl_rx        | RO     | 0x0     | realtime en_flowctrl_rx                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 6     | En_flowctrl_tx        | RO     | 0x0     | realtime en_flowctrl_tx                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 5:4   | Reserved              | RO     | 0x0     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3:1   | Xmit                  | RO     | 0x0     | realtime transmit statemachine. 001: Xmit Idle; 010: Xmit Config; 100: Xmit Data.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0     | Sync_status           | RO     | 0x0     | realtime sync_status                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## 4.5.12. Sds specific status register (0x12)

Table 128. Sds specific status register (0x12)

| Bit  | Symbol   | Access | Default | Description |
|------|----------|--------|---------|-------------|
| 15:2 | Reserved | RO     | 0x0     | reserved    |

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|     |               |    |     |                                                                                                                                                    |
|-----|---------------|----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | rx_lpi_active | RO | 0x0 | 1 = SerDes is RX LPI pattern.                                                                                                                      |
| 2:0 | ser_mode_cfg  | RO | 0x4 | SerDes working status:<br>000=SGMII_MAC,                      001=SGMII_PHY,<br>010=FIB_1000,                      011=FIB_100,<br>100=2500BASE-X. |

### 4.5.13. Isolate\_rx and 2500BX AN control (0x14)

Table 129. (0x14)

| Bit   | Symbol               | Access | Default | Description                                                                                                                                                                                                           |
|-------|----------------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | Reserved             | RW     | 0xF     | reserved                                                                                                                                                                                                              |
| 11    | Reserved             | RW     | 0x1     | reserved                                                                                                                                                                                                              |
| 10    | isolate_rx           | RW     | 0x0     | 1 = isolate SerDes RX                                                                                                                                                                                                 |
| 9     | reserved             | RO     | 0x0     | reserved                                                                                                                                                                                                              |
| 8     | Uni_rx_iso           | RW     | 0x0     | 1 = in unidirection mode, isolate RX data;                                                                                                                                                                            |
| 7:4   | Reserved             | RW     | 0x2     | Reserved                                                                                                                                                                                                              |
| 3     | En_ctrl_2500bx_an_en | RW     | 0x1     | 1 = 2500BASE-X's AN_EN is controled by a shadow register of SDS MII 0x0 bit12, which could only be accessed when SerDes works in 2500BASE-X mode;<br>0 = the shadow register of SDS MII 0x0 bit12 is always disabled. |
| 2:0   | Reserved             | RO     | 0x0     | Reserved                                                                                                                                                                                                              |

### 4.5.14. Link fail counter mon (0x16)

Table 130. Link fail counter mon (0x16)

| Bit  | Symbol        | Access | Default | Description       |
|------|---------------|--------|---------|-------------------|
| 15:8 | Reserved      | RO     | 0x0     | Reserved          |
| 7:0  | Link_fail_cnt | RO SC  | 0x0     | link fail counter |

## 4.6. Sds EXT Register

### 4.6.1. Sds prbs cfg1 (0x05)

Table 131. Sds prbs cfg1 (0x05)

| Bit | Symbol  | Access | Default | Description                                                                                 |
|-----|---------|--------|---------|---------------------------------------------------------------------------------------------|
| 15  | En_prbs | RW     | 0x0     | enable TX PRBS or self-defined pattern, the pattern type is determined by bit7:5 test_mode. |

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|      |                  |    |     |                                                                                                                                                                                                                                                                         |
|------|------------------|----|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14   | En_bert          | RW | 0x0 | enable Bit Error Rate Test;                                                                                                                                                                                                                                             |
| 13:9 | Reserved         | RW | 0x0 | Reserved                                                                                                                                                                                                                                                                |
| 8    | Test_mode_prbs31 | RW | 0x0 | 1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0] take effect then.                                                                                                                                                                   |
| 7:5  | Test_mode        | RW | 0x0 | Control the TX pattern in test mode: 0x0, PRBS7; 0x1, PRBS10; 0x2, Fix pattern, the fix pattern is controlled by Ext.6;0x3, 010101...; 0x4, 00110011...; 0x5, 00000_11111_00000_11111...; 0x6, 0000_0000_00_1111_1111_11...; 0x7, Increase pattern, 0->1023->0->1023... |
| 4    | Reserved         | RW | 0x0 | Reserved                                                                                                                                                                                                                                                                |
| 3:0  | Reserved         | RO | 0x0 | Reserved                                                                                                                                                                                                                                                                |

### 4.6.2. Sds prbs cfg2 (0x06)

Table 132. Sds prbs cfg2 (0x06)

| Bit       | Symbol          | Access | Default | Description                           |
|-----------|-----------------|--------|---------|---------------------------------------|
| 15:1<br>0 | Reserved        | RO     | 0x0     | Reserved                              |
| 9:0       | Fix_pattern_9_0 | RW     | 0x0     | fix pattern transmited in test_mode 2 |

### 4.6.3. Sds prbs mon1 (0x08)

Table 133. Sds prbs mon1 (0x08)

| Bit  | Symbol        | Access | Default | Description                                                                                                 |
|------|---------------|--------|---------|-------------------------------------------------------------------------------------------------------------|
| 15:9 | Reserved      | RO     | 0x0     | Reserved                                                                                                    |
| 8    | Err           | RO     | 0x0     | Err flag after PRBS has synchronized                                                                        |
| 7:2  | Reserved      | RO     | 0x0     | Reserved                                                                                                    |
| 1    | Bitsync_latch | RO LL  | 0x0     | PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out. |
| 0    | Bitsync       | RO     | 0x0     | real time synchronization status                                                                            |

### 4.6.4. Sds prbs mon2 (0x09)

Table 134. Sds prbs mon2 (0x09)

| Bit  | Symbol       | Access | Default | Description                                         |
|------|--------------|--------|---------|-----------------------------------------------------|
| 15:0 | Err_cnt_15_0 | RO     | 0x0     | real time lowest 16 bits received error bit counter |

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### 4.6.5. Sds prbs mon3 (0x0A)

Table 135. Sds prbs mon3 (0x0A)

| Bit  | Symbol        | Access | Default | Description                                          |
|------|---------------|--------|---------|------------------------------------------------------|
| 15:0 | Err_cnt_31_16 | RO     | 0x0     | real time highest 16 bits received error bit counter |

### 4.6.6. Sds status mon1 (0xC0)

Table 136. Sds status mon1 (0xC0)

| Bit  | Symbol   | Access | Default | Description                                                               |
|------|----------|--------|---------|---------------------------------------------------------------------------|
| 15:4 | Reserved | RO     | 0x0     | Reserved                                                                  |
| 3    | Linkup   | RO     | 0x0     | real time linkup status                                                   |
| 2:0  | Speed    | RO     | 0x0     | real time sds speed. 11: 2500Mbps; 10: 1000Mbps; 01: 100Mbps; 00: 10Mbps. |

### 4.6.7. Sds status mon2 (0xC1)

Table 137. Sds status mon2 (0xC1)

| Bit  | Symbol      | Access | Default | Description                                                                                                                                                                                                                                 |
|------|-------------|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | Reserved    | RO     | 0x0     | Reserved                                                                                                                                                                                                                                    |
| 8    | Sync_status | RO     | 0x0     | real time sgmi ,1000BX or 2500BX sync status                                                                                                                                                                                                |
| 7:4  | Reserved    | RO     | 0x0     | Reserved                                                                                                                                                                                                                                    |
| 3:0  | An_cst      | RO     | 0x0     | real time autonegotiation state machine.<br>0000: AN_ENABLE; 0001: AN_RESTART;<br>0010: ABILITY_DETECT; 0011:<br>ACK_DETECT; 0100: COMPLET_ACK;<br>0101: IDLE_DETECT; 0110: LINK_OK;<br>0111: AN_DIS_LINKOK; 1000:<br>AN_PARALLEL_DETECTED. |

### 4.6.8. Sds status mon3 (0xC2)

Table 138. Sds status mon3 (0xC2)

| Bit   | Symbol                | Access | Default | Description                                                      |
|-------|-----------------------|--------|---------|------------------------------------------------------------------|
| 15:10 | Reserved              | RO     | 0x0     | Reserved                                                         |
| 9     | align_unmatch_err_ind | RO     | 0x0     | Alignment index mismatch error happened since the last read out. |
| 8     | align_unmatch_err     | RO     | 0x0     | Real time alignment index mismatch.                              |
| 7     | Reserved              | RO     | 0x0     | Reserved                                                         |

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|     |               |    |     |                                                  |
|-----|---------------|----|-----|--------------------------------------------------|
| 6:5 | Align_cst     | RO | 0x0 | real time sgmi or 1000BX alignment state machine |
| 4:0 | Aligned_index | RO | 0x0 | real time alignment index                        |

### 4.6.9. Sds rx\_cg\_invalid\_cnt(0xC3)

Table 139. Sds rx\_cg\_invalid\_cnt (0xC3)

| Bit  | Symbol            | Access | Default | Description                   |
|------|-------------------|--------|---------|-------------------------------|
| 15:8 | Reserved          | RO     | 0x0     | Reserved                      |
| 7:0  | rx_cg_invalid_cnt | RO     | 0x0     | the counter for rx_cg_invalid |

### 4.6.10. Sds Pkg Cfg0 (0x1a0)

Table 140.Sds Pkg Cfg0 (0x1a0)

| Bit  | Symbol                | Access | Default | Description                                                                                                                                                                                                                                                     |
|------|-----------------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | u0_pkg_chk_en         | RW     | 0x0     | 1: to enable RX/TX package checker. For RX checker, if ext.A0B7.15=0, RX checker checks the Fiber's GMII RX data; For TX checker, if ext.A0B7.10=1, TX checker checks the pkg_gen's TX data; else if ext.A0B7.14=0, TX checker checks the Fiber's GMII TX data; |
| 14   | u0_pkg_en_gate        | RW     | 0x1     | 1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;                                                                                                                       |
| 13   | u0_bp_pkg_gen         | RW     | 0x1     | 1: normal function; 0: test function, the TX data is sourced from pkg_gen;                                                                                                                                                                                      |
| 12   | u0_pkg_gen_en         | RW SC  | 0x0     | 1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0.                                                                                                                                     |
| 11:8 | u0_pkg_prm_lth        | RW     | 0x8     | The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.                                                                               |
| 7:4  | u0_pkg_ipg_lth        | RW     | 0xc     | The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.                                                                                           |
| 3    | u0_Xmit_mac_force_gen | RW     | 0x0     | 1: To enable pkg_gen to send out the generated data even when the link is not                                                                                                                                                                                   |

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|     |                    |    |     |                                                                                                                                                                                            |
|-----|--------------------|----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                    |    |     | established.                                                                                                                                                                               |
| 2   | u0_pkg_corrupt_crc | RW | 0x0 | 1: to make pkg_gen to send out CRC error packages.                                                                                                                                         |
| 1:0 | u0_pkg_payload     | RW | 0x0 | Control the payload of the generated packages.<br>00: increased Byte payload;<br>01: random payload;<br>10: fix pattern 0x5AA55AA5...<br>11: fixed pattern programed by EXT 0x3B<br>bit7:0 |

### 4.6.11. Sds Pkg Cfg1 (0x1a1)

Table 141. Sds Pkg Cfg1(0x1a1)

| Bit  | Symbol        | Access | Default | Description                                  |
|------|---------------|--------|---------|----------------------------------------------|
| 15:0 | u0_pkg_length | RW     | 0x40    | To set the length of the generated packages. |

### 4.6.12. Sds Pkg Cfg2 (0x1a2)

Table 142. Sds Pkg Cfg2(0x1a2)

| Bit  | Symbol            | Access | Default | Description                                                     |
|------|-------------------|--------|---------|-----------------------------------------------------------------|
| 15:0 | u0_pkg_burst_size | RW     | 0x0     | To set the number of packages in a burst of package generation. |

### 4.6.13. Sds Pkg Rx Valid0 (0x1a3)

Table 143. Sds Pkg Rx Valid0(0x1a3)

| Bit  | Symbol               | Access | Default | Description                                                                                                                         |
|------|----------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_valid_high | RO RC  | 0x0     | Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. |

### 4.6.14. Sds Pkg Rx Valid1 (0x1a4)

Table 144. Sds Pkg Rx Valid1(0x1a4)

| Bit  | Symbol              | Access | Default | Description                                                                                                                        |
|------|---------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_valid_low | RO RC  | 0x0     | Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte. |

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### 4.6.15. Sds Pkg Rx Os0 (0x1a5)

Table 145. Sds Pkg Rx Os0(0x1a5)

| Bit  | Symbol                 | Access | Default | Description                                                                                                              |
|------|------------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_os_good_high | RO RC  | 0x0     | Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

### 4.6.16. Sds Pkg Rx Os1 (0x1a6)

Table 146.Sds Pkg Rx Os1 (0x1a6)

| Bit  | Symbol                | Access | Default | Description                                                                                                              |
|------|-----------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_os_good_low | RO RC  | 0x0     | Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

### 4.6.17. Sds Pkg Rx Us0 (0x1a7)

Table 147.Sds Pkg Rx Us0 (0x1a7)

| Bit  | Symbol                 | Access | Default | Description                                                                                                            |
|------|------------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_us_good_high | RO RC  | 0x0     | Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte. |

### 4.6.18. Sds Pkg Rx Us1 (0x1a8)

Table 148.Sds Pkg Rx Us1 (0x1a8)

| Bit  | Symbol                | Access | Default | Description                                                                                                              |
|------|-----------------------|--------|---------|--------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_us_good_low | RO RC  | 0x0     | Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte. |

### 4.6.19. Sds Pkg Rx Err (0x1a9)

Table 149. Sds Pkg Rx Err (0x1a9)

| Bit  | Symbol        | Access | Default | Description                                                                      |
|------|---------------|--------|---------|----------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_err | RO RC  | 0x0     | pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length |

|  |  |  |  |                           |
|--|--|--|--|---------------------------|
|  |  |  |  | are >=64Byte, <=1518Byte. |
|--|--|--|--|---------------------------|

#### 4.6.20. Sds Pkg Rx Os Bad (0x1aa)

Table 150. Sds Pkg Rx Os Bad(0x1aa)

| Bit  | Symbol           | Access | Default | Description                                                                                        |
|------|------------------|--------|---------|----------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_os_bad | RO RC  | 0x0     | pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >1518Byte. |

#### 4.6.21. Sds Pkg Rx Fragment (0x1ab)

Table 151. Sds Pkg Rx Fragment(0x1ab)

| Bit  | Symbol         | Access | Default | Description                                                                  |
|------|----------------|--------|---------|------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_frag | RO RC  | 0x0     | pkg_ib_frag is the number of RX packages from wire whose length are <64Byte. |

#### 4.6.22. Sds Pkg Rx Nosfd (0x1ac)

Table 152. Sds Pkg Rx Nosfd(0x1ac)

| Bit  | Symbol          | Access | Default | Description                                                              |
|------|-----------------|--------|---------|--------------------------------------------------------------------------|
| 15:0 | u0_pkg_ib_nosfd | RO RC  | 0x0     | pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed. |

#### 4.6.23. Sds Pkg Tx Valid0 (0x1ad)

Table 153. Sds Pkg Tx Valid0 (0x1ad)

| Bit  | Symbol               | Access | Default | Description                                                                                                                        |
|------|----------------------|--------|---------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_valid_high | RO RC  | 0x0     | Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte. |

#### 4.6.24. Sds Pkg Tx Valid1 (0x1ae)

Table 154. Sds Pkg Tx Valid1(0x1ae)

| Bit  | Symbol              | Access | Default | Description                                                                                                                       |
|------|---------------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_valid_low | RO RC  | 0x0     | Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte. |

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### 4.6.25. Sds Pkg Tx Os0 (0x1af)

Table 155. Sds Pkg Tx Os0 (0x1af)

| Bit  | Symbol                 | Access | Default | Description                                                                                                             |
|------|------------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_os_good_high | RO RC  | 0x0     | Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

### 4.6.26. Sds Pkg Tx Os1 (0x1b0)

Table 156. Sds Pkg Tx Os1 (0x1b0)

| Bit  | Symbol                | Access | Default | Description                                                                                                             |
|------|-----------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_os_good_low | RO RC  | 0x0     | Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

### 4.6.27. Sds Pkg Tx Us0 (0x1b1)

Table 157. Sds Pkg Tx Us0(0x1b1)

| Bit  | Symbol                 | Access | Default | Description                                                                                                           |
|------|------------------------|--------|---------|-----------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_us_good_high | RO RC  | 0x0     | Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte. |

### 4.6.28. Sds Pkg Tx Us1 (0x1b2)

Table 158. Sds Pkg Tx Us1(0x1b2)

| Bit  | Symbol                | Access | Default | Description                                                                                                             |
|------|-----------------------|--------|---------|-------------------------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_us_good_low | RO RC  | 0x0     | Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte. |

### 4.6.29. Sds Pkg Tx Err (0x1b3)

Table 159. Sds Pkg Tx Err(0x1b3)

| Bit  | Symbol        | Access | Default | Description                                                                                               |
|------|---------------|--------|---------|-----------------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_err | RO RC  | 0x0     | pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte. |

### 4.6.30. Sds Pkg Tx Os Bad (0x1b4)

Table 160. Sds Pkg Tx Os Bad(0x1b4)

| Bit  | Symbol           | Access | Default | Description                                                                                       |
|------|------------------|--------|---------|---------------------------------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_os_bad | RO RC  | 0x0     | pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >1518Byte. |

### 4.6.31. Sds Pkg Tx Fragment (0x1b5)

Table 161. Sds Pkg Tx Fragment(0x1b5)

| Bit  | Symbol         | Access | Default | Description                                                                 |
|------|----------------|--------|---------|-----------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_frag | RO RC  | 0x0     | pkg_ob_frag is the number of TX packages from MII whose length are <64Byte. |

### 4.6.32. Sds Pkg Tx Nosfd (0x1b6)

Table 162. Sds Pkg Tx Nosfd(0x1b6)

| Bit  | Symbol          | Access | Default | Description                                                             |
|------|-----------------|--------|---------|-------------------------------------------------------------------------|
| 15:0 | u0_pkg_ob_nosfd | RO RC  | 0x0     | pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed. |

## 5. DC Characteristics

### 5.1. Absolute Maximum Ratings

Table 163. Absolute Maximum Ratings

| Description          | Symbol             | Mini | Max  | Unit |
|----------------------|--------------------|------|------|------|
| High power supply    | DVDDH, AVDDH       | -0.3 | 3.63 | V    |
| Low power supply     | DVDDL, AVDDL,SVDDL | -0.2 | 1.05 | V    |
| Input IO Voltage     | DVDD3318 = 1.8V    | -0.3 | 1.98 | V    |
|                      | DVDD3318 = 3.3V    | -0.3 | 3.63 | V    |
| Junction Temperature |                    | –    | 125  | °C   |
| Storage Temperature  |                    | -45  | 125  | °C   |

Note : These absolute maximum ratings indicate levels where permanent damage to the device can occur. The function of chip is not guaranteed under these conditions. The chip at these conditions may affect long-term reliability of the device.

### 5.2. Recommended Operating Conditions

Table 164. Recommended Operating Conditions

| Description                                  | Pins                | Min   | Typ  | Max   | Unit |
|----------------------------------------------|---------------------|-------|------|-------|------|
| High power supply                            | DVDDH, AVDDH        | 3.135 | 3.30 | 3.465 | V    |
| Low power supply                             | DVDDL, AVDDL, SVDDL | 0.92  | 0.95 | 0.98  | V    |
| Input IO Voltage                             | DVDD3318 = 1.8V     | 1.71  | 1.8  | 1.89  | V    |
|                                              | DVDD3318 = 3.3V     | 3.135 | 3.3  | 3.465 | V    |
| Ambient Operation Temperature for Commercial |                     | 0     | –    | 70    | °C   |
| Ambient Operation Temperature for Industry   |                     | -40   | –    | 85    | °C   |

### 5.3. DC Characteristics

Table 165. DC Characteristics

| Symbol              | Parameter            | Min   | Typ  | Max   | Units |
|---------------------|----------------------|-------|------|-------|-------|
| DVDDH,AVDDH         | 3.3V Supply Voltage  | 3.135 | 3.30 | 3.465 | V     |
| DVDDL, AVDDL, SVDDL | 0.95V Supply Voltage | 0.92  | 0.95 | 0.98  | V     |
| DVDD3318            | DVDD3318 = 1.8V      | 1.71  | 1.8  | 1.89  | V     |
|                     | DVDD3318 = 3.3V      | 3.135 | 3.3  | 3.465 | V     |
| Voh                 | 3.3V IO power domain | 2.4   | –    | –     | V     |

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|     |                      |           |   |           |   |
|-----|----------------------|-----------|---|-----------|---|
|     | 1.8V IO power domain | VDDH-0.45 | – | –         | V |
| Vol | 3.3V IO power domain | –         | – | 0.4       | V |
|     | 1.8V IO power domain | –         | – | 0.45      | V |
| Vih | 3.3V IO power domain | 2.0       | – | VDDH+0.3  | V |
|     | 1.8V IO power domain | 0.65*VDDH | – | VDDH+0.3  | V |
| Vil | 3.3V IO power domain | -0.3      | – | 0.8       | V |
|     | 1.8V IO power domain | -0.3      | – | 0.35*VDDH | V |

## 5.4. Power Consumption

Table 166. AUTO\_BX2500\_SGMII mode Power Consumption

| Condition                | 3.3V(A) | 0.95V(A) | Power Consumption(W) |
|--------------------------|---------|----------|----------------------|
| Hardware Reset           | 0.009   | 0.031    | 0.058                |
| Power down(MII reg0.11)  | 0.025   | 0.093    | 0.171                |
| Sleep                    | 0.024   | 0.068    | 0.144                |
| EEE @2500Mbps(1%Traffic) | 0.039   | 0.517    | 0.619                |
| Traffic @2500Mbps        | 0.132   | 0.750    | 1.15                 |
| Traffic @1000Mbps        | 0.107   | 0.343    | 0.679                |

Note: Test by TT IC with 3.3V and 0.95V at room temperature.

AUTO\_BX2500\_SGMII mode Power Consumption

| Condition         | 3.3V(A) | 0.95V(A) | Power Consumption(W) |
|-------------------|---------|----------|----------------------|
| Traffic @2500Mbps | 0.135   | 1.000    | 1.40                 |

Note: Test by FF IC with 3.3V and 0.95V at high temperature 85°C.

## 6. AC and Timing Characteristics

### 6.1. Power On Sequence

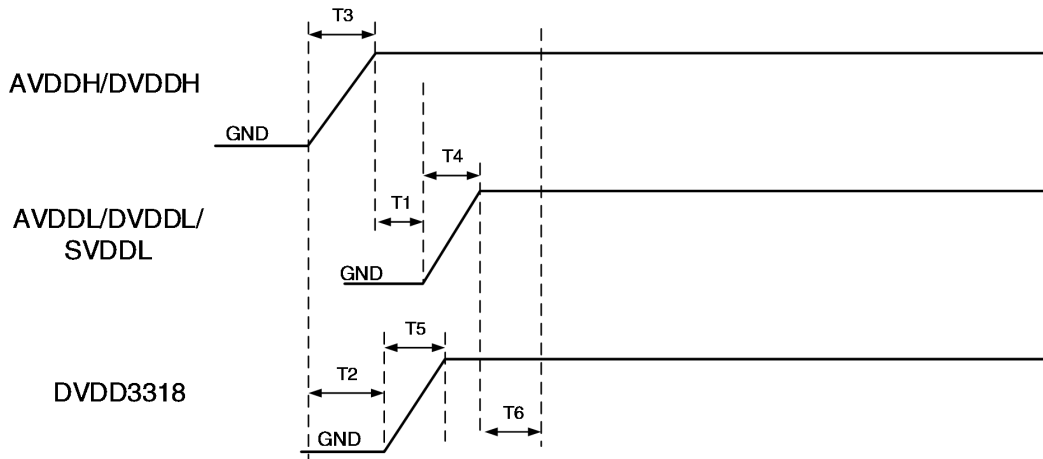


Table 167. Power On Sequence

| Symbol | Description                                                     | Min    | Typ | Max | Units |
|--------|-----------------------------------------------------------------|--------|-----|-----|-------|
| T1     | The delay time from 3.3V to 0.95V                               | (Note) | –   | –   | ms    |
| T2     | The delay time from 3.3V to DVDD3318                            | 0      | –   | –   | ms    |
| T3     | AVDDH/DVDDH power rising time.                                  | 0.5    | –   | 10  | ms    |
| T4     | AVDDL/DVDDL/SVDDL power rising time.                            | 0.5    | –   | 5   | ms    |
| T5     | DVDD3318 power rising time.                                     | 0.5    | –   | –   | ms    |
| T6     | Core logic ready time from all powers steady(without SPI flash) | –      | –   | 50  | ms    |

Note: AVDDL/DVDDL/SVDDL should start to ramp up after AVDDH/DVDDH reaches 3.3V

### 6.2. Crystal Requirement

Table 168. Crystal Requirement

| Symbol          | Description                                             | Min | Typ | Max | Unit |
|-----------------|---------------------------------------------------------|-----|-----|-----|------|
| Fref            | Parallel Resonant Crystal Reference Frequency           | –   | 25  | –   | MHz  |
| Fref Tolerance  | Parallel Resonant Crystal Reference Frequency Tolerance | -50 | –   | 50  | ppm  |
| Fref Duty Cycle | Reference Clock Input Duty Cycle                        | 40  | –   | 60  | %    |
| ESR             | Equivalent Series Resistance                            | –   | –   | 50  | ohm  |
| Vih             | Crystal output high level                               | 1.4 | –   | –   | V    |
| Vil             | Crystal output low level                                | –   | –   | 0.4 | V    |

### 6.3. Oscillator/External Clock Requirement

Table 169. Oscillator/External Clock Requirement

| Parameter                | Min | Typ | Max | Unit |
|--------------------------|-----|-----|-----|------|
| Frequency                | –   | 25  | –   | MHz  |
| Frequency tolerance      | -50 | –   | 50  | PPM  |
| Duty Cycle               | 40  | –   | 60  | %    |
| V <sub>ih</sub>          | 1.5 | –   | –   | V    |
| V <sub>il</sub>          | –   | –   | 0.4 | V    |
| Rise Time (10%~90%)      | –   | –   | 10  | ns   |
| Fall Time (10%~90%)      | –   | –   | 10  | ns   |
| RMS Jitter (12kHz~20MHz) | –   | –   | 1   | ps   |

### 6.4. 2500BASE-X Differential Transmitter Characteristics

Table 170. 2500BX Differential Transmitter Characteristics

| Symbol                 | Parameter                   | Min | Typ | Max  | Units | Notes         |
|------------------------|-----------------------------|-----|-----|------|-------|---------------|
| UI                     | Unit Interval               | –   | 320 | –    | ps    | 320ps ± 75ppm |
| T <sub>X1</sub>        | Eye Mask                    | –   | –   | 0.15 | UI    |               |
| T <sub>X2</sub>        | Eye Mask                    | –   | –   | 0.4  | UI    |               |
| T <sub>Y1</sub>        | Eye Mask                    | 150 | –   | –    | mV    |               |
| T <sub>Y2</sub>        | Eye Mask                    | –   | –   | 400  | mV    |               |
| V <sub>TX-DIFFpp</sub> | Output differential voltage | 350 | 500 | 700  | mV    |               |
| T <sub>TX-EYE</sub>    | Minimum TX eye width        | 0.7 | –   | –    | UI    |               |
| T <sub>TX-JITTER</sub> | Output Jitter               | –   | –   | 0.3  | UI    |               |
| R <sub>TX</sub>        | Differential Resistance     | 80  | 100 | 120  | ohm   |               |
| C <sub>TX</sub>        | AC Coupling Capacitor       | 80  | 100 | 120  | nF    |               |
| L <sub>TX</sub>        | Transmit Length in PCB(FR4) | –   | –   | 10   | inch  |               |

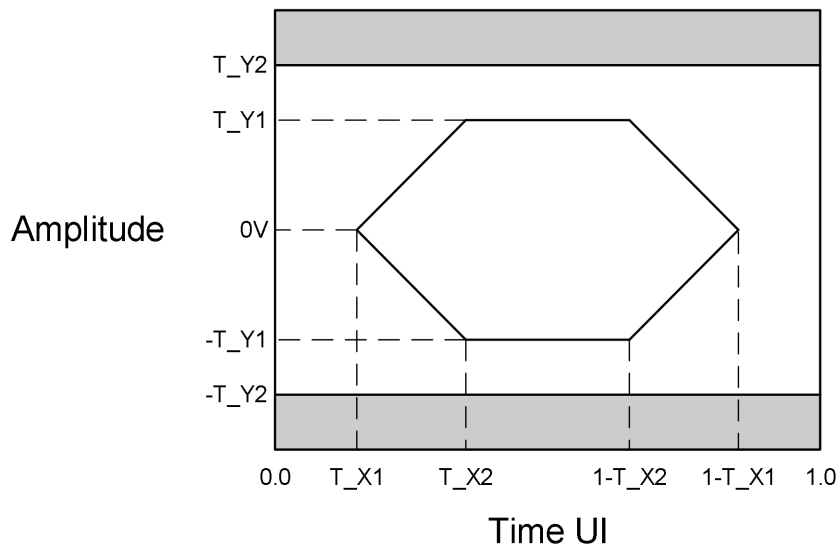


Figure 4. QSGMII Differential Transmitter Eye Diagram

## 6.5. 2500BASE-X Differential Receiver Characteristics

Table 171. 2500BX Differential Receiver Characteristics

| Symbol          | Parameter                  | Min | Typ | Max      | Units | Notes |
|-----------------|----------------------------|-----|-----|----------|-------|-------|
| UI              | Unit Interval              | –   | 320 | –        | ps    |       |
| R_X1            | Eye Mask                   | –   | –   | 0.3      | UI    |       |
| R_Y1            | Eye Mask                   | 100 | –   | –        | mV    |       |
| R_Y2            | Eye Mask                   | –   | –   | 600      | mV    |       |
| $V_{RX-DIFFpp}$ | Input differential voltage | 200 | –   | 120<br>0 | mV    |       |
| $T_{RX-EYE}$    | Minimum RX eye width       | 0.4 | –   | –        | UI    |       |
| $T_{RX-JITTER}$ | Input Jitter Tolerance     | –   | –   | 0.6      | UI    |       |
| $R_{RX}$        | Differential Resistance    | 80  | 100 | 120      | ohm   |       |

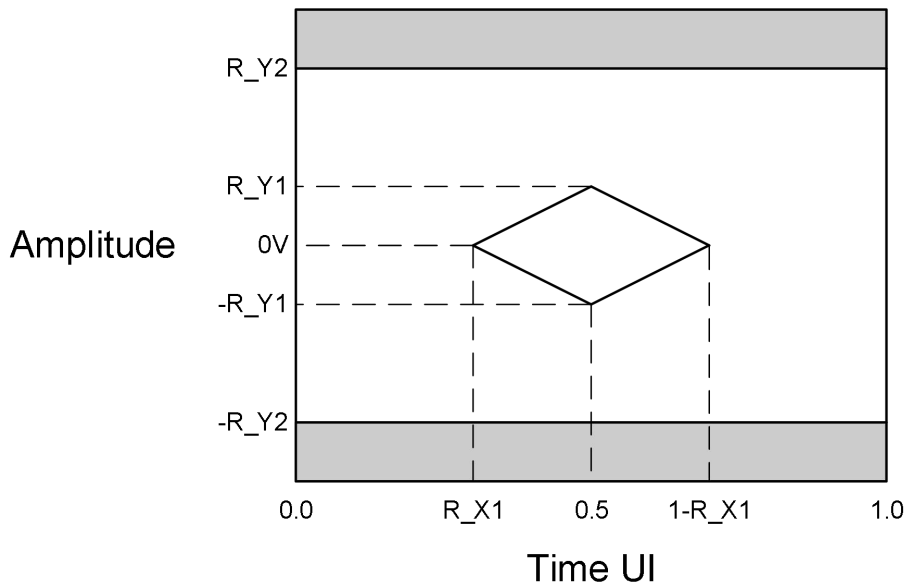


Figure 5. QSGMII Differential Receiver Eye Diagram

## 6.6. SGMII Differential Transmitter Characteristics

Table 172. SGMII Differential Transmitter Characteristics

| Symbol                  | Parameter                   | Min | Typ | Max  | Units | Notes             |
|-------------------------|-----------------------------|-----|-----|------|-------|-------------------|
| UI                      | Unit Interval               | –   | 800 | –    | ps    | 800ps $\pm$ 75ppm |
| T_X1                    | Eye Mask                    | –   | –   | 0.15 | UI    |                   |
| T_X2                    | Eye Mask                    | –   | –   | 0.4  | UI    |                   |
| T_Y1                    | Eye Mask                    | 150 | –   | –    | mV    |                   |
| T_Y2                    | Eye Mask                    | –   | –   | 400  | mV    |                   |
| V <sub>TX-DIFFp-p</sub> | Output Differential Voltage | 350 | 500 | 700  | mV    |                   |
| T <sub>TX-EYE</sub>     | Minimum TX Eye Width        | 0.7 | –   | –    | UI    |                   |
| T <sub>TX-JITTER</sub>  | Output Jitter               | –   | –   | 0.3  | UI    |                   |
| R <sub>TX</sub>         | Differential Resistance     | 80  | 100 | 120  | ohm   |                   |
| C <sub>TX</sub>         | AC Coupling Capacitor       | 80  | 100 | 120  | nF    |                   |
| L <sub>TX</sub>         | Transmit Length in PCB(FR4) | –   | –   | 10   | inch  |                   |

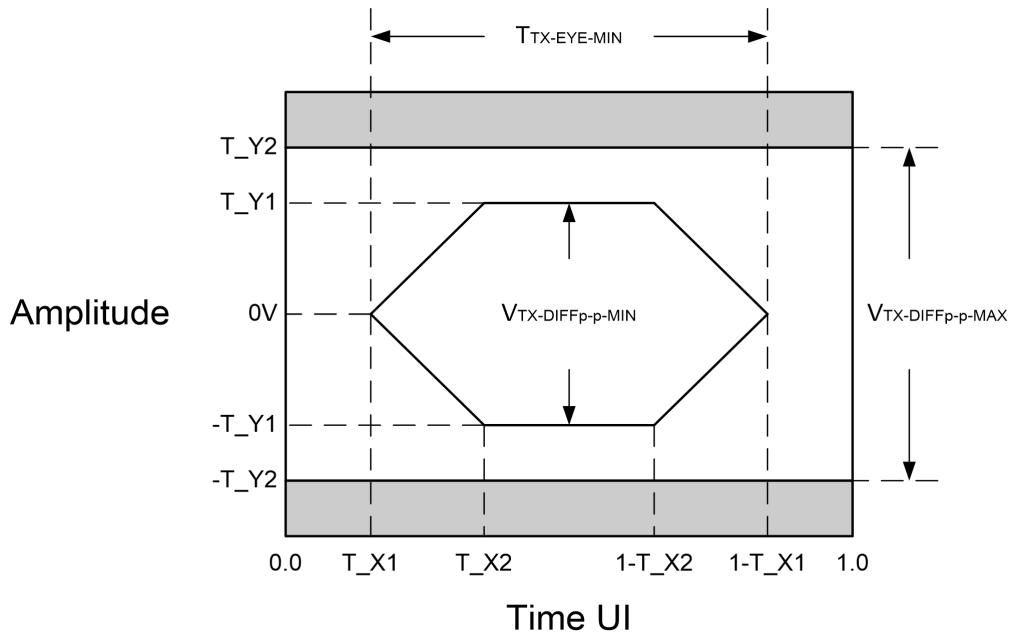


Figure 6. 1.25G Serdes Differential Transmitter Eye Diagram

## 6.7. SGMII Differential Receiver Characteristics

Table 173. SGMII Differential Receiver Characteristics

| Symbol           | Parameter                  | Min | Typ | Max      | Units | Notes             |
|------------------|----------------------------|-----|-----|----------|-------|-------------------|
| UI               | Unit Interval              | –   | 800 | –        | ps    | 800ps $\pm$ 75ppm |
| R_X1             | Eye Mask                   | –   | –   | 0.3      | UI    |                   |
| R_Y1             | Eye Mask                   | 100 | –   | –        | mV    |                   |
| R_Y2             | Eye Mask                   | –   | –   | 600      | mV    |                   |
| $V_{RX-DIFFp-p}$ | Input Differential Voltage | 200 | –   | 120<br>0 | mV    |                   |
| $T_{RX-EYE}$     | Minimum RX Eye Width       | 0.4 | –   | –        | UI    |                   |
| $T_{RX-JITTER}$  | Input Jitter Tolerance     | –   | –   | 0.6      | UI    |                   |
| $R_{RX}$         | Differential Resistance    | 80  | 100 | 120      | ohm   | –                 |

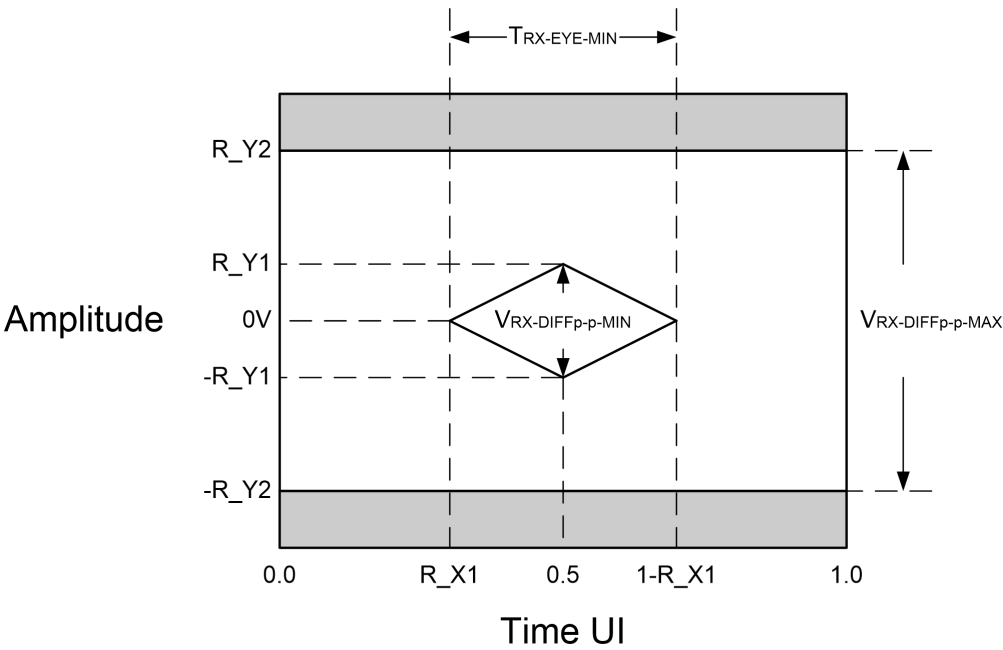


Figure 7. 1.25G Serdes Differential Receiver Eye Diagram

6.8. SMI (MDC/MDIO) Interface Timing

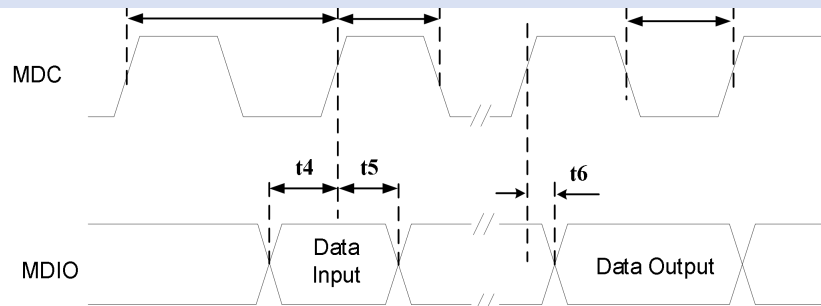


Figure 8. SMI (MDC/MDIO) Timing

Table 174. SMI (MDC/MDIO) Interface Characteristics

| Symbol | Description                                   | Min | Typ | Max | Units |
|--------|-----------------------------------------------|-----|-----|-----|-------|
| t1     | MDC Clock Period                              | 80  | –   | –   | ns    |
| t2     | MDC High Time                                 | 32  | –   | –   | ns    |
| t3     | MDC Low Time                                  | 32  | –   | –   | ns    |
| t4     | MDIO to MDC Rising Setup Time (Data Input)    | 10  | –   | –   | ns    |
| t5     | MDIO to MDC Rising Hold Time (Data Input)     | 10  | –   | –   | ns    |
| t6     | MDIO Valid from MDC rising edge (Data Output) | 0   | –   | 20  | ns    |

## 6.9. SPI Flash Interface Timing

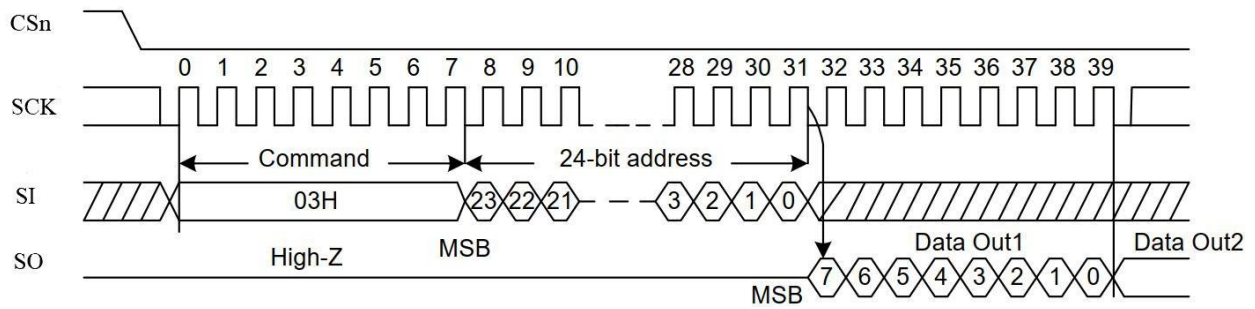


Figure 9. Read Command Sequence

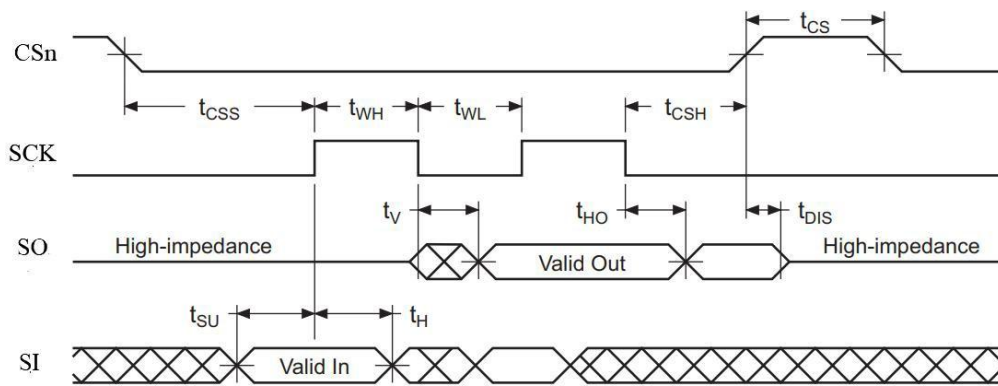


Figure 10. SPI flash interface timing

| Symbol    | Description                                          | Min | Typ  | Max | Units |
|-----------|------------------------------------------------------|-----|------|-----|-------|
| $f_{sck}$ | SCK Frequency                                        | –   | 12.5 | –   | MHz   |
| $t_{WH}$  | SCK High Time                                        | –   | 40   | –   | ns    |
| $t_{WL}$  | SCK Low Time                                         | –   | 40   | –   | ns    |
| $t_{CSS}$ | CSn setup time                                       | 5   | –    | –   | ns    |
| $t_{CSH}$ | CSn hold time                                        | 5   | –    | –   | ns    |
| $t_{SU}$  | Output to SPI Flash serial data input pin setup time | 2   | –    | –   | ns    |
| $t_H$     | Output to SPI Flash serial data input pin hold time  | 2   | –    | –   | ns    |

Table 175. SPI Flash Interface Characteristics

# 7. Mechanical and Thermal

## 7.1. Mechanical Information

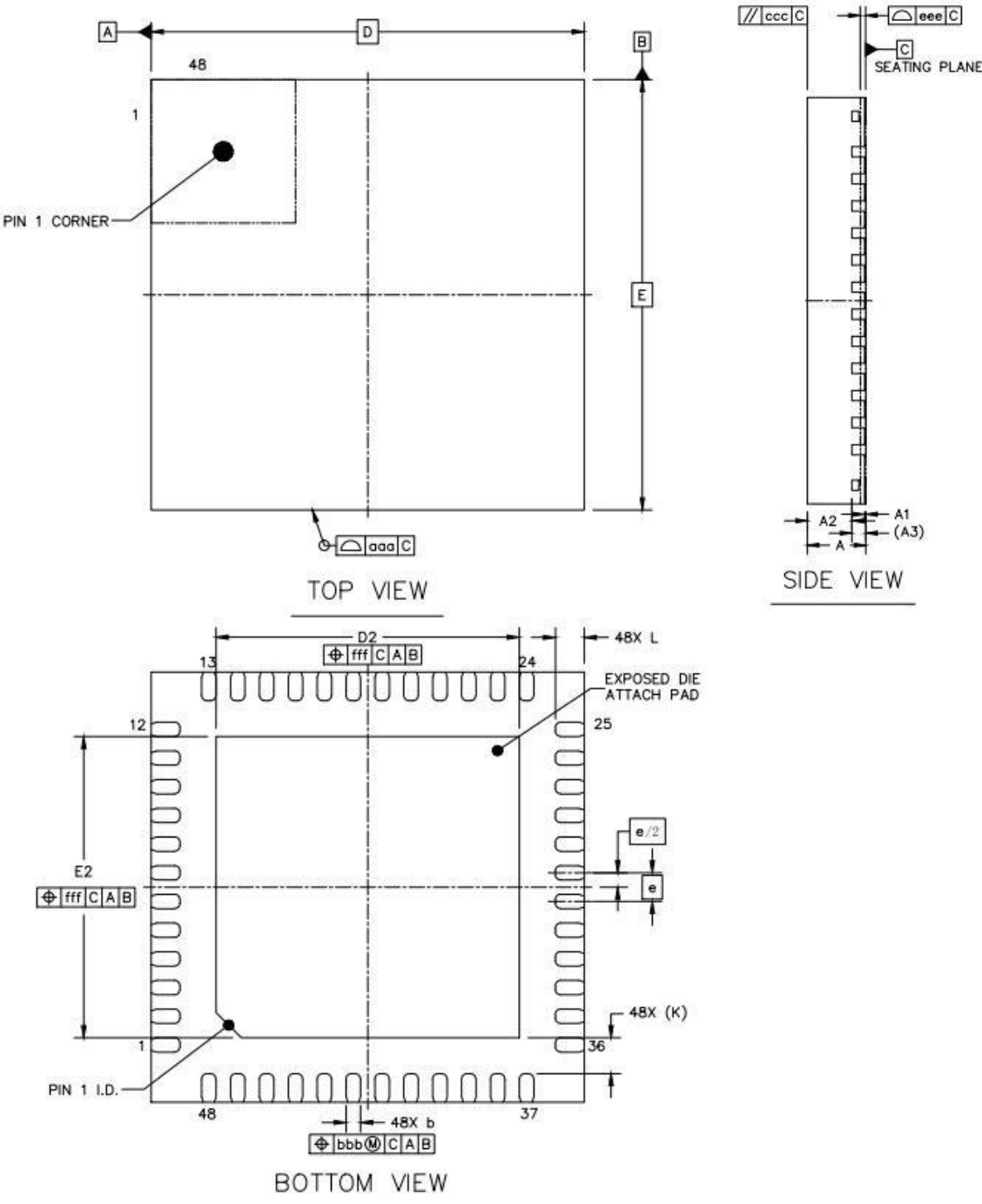


Table 176. Mechanical Dimensions

|                 |   | SYMBOL | MIN       | NOM  | MAX  |
|-----------------|---|--------|-----------|------|------|
| TOTAL THICKNESS |   | A      | 0.80      | 0.85 | 0.90 |
| STAND OFF       |   | A1     | 0         | 0.02 | 0.05 |
| MOLD THICKNESS  |   | A2     | ---       | 0.65 | ---  |
| L/F THICKNESS   |   | A3     | 0.203 REF |      |      |
| LEAD WIDTH      |   | b      | 0.15      | 0.20 | 0.25 |
| BODY SIZE       | X | D      | 6.00 BSC  |      |      |
|                 | Y | E      | 6.00 BSC  |      |      |
| LEAD PITCH      |   | e      | 0.40 BSC  |      |      |
| EP SIZE         | X | D2     | 4.10      | 4.30 | 4.50 |
|                 | Y | E2     | 4.10      | 4.30 | 4.50 |
| LEAD LENGTH     |   | L      | 0.30      | 0.40 | 0.50 |

## 7.2. Thermal

Table 177. Thermal Resistance

| Symbol            | Parameter                                                                                                                                                                            | Condition                                                                   | Typ  | Units                |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|------|----------------------|
| $\Theta_{JA}$     | Thermal resistance - junction to ambient<br>$\Theta_{JA} = (T_J - T_A) / P$<br>P = Total power dissipation                                                                           | JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow $T_A=25^{\circ}\text{C}$ | 27.8 | $^{\circ}\text{C/W}$ |
|                   |                                                                                                                                                                                      | JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow $T_A=85^{\circ}\text{C}$ | 26.2 | $^{\circ}\text{C/W}$ |
| $\Theta_{JB}$     | Thermal resistance - junction to board $\Theta_{JB} = (T_J - T_B) / P_{\text{bottom}}$<br>$P_{\text{bottom}}$ = Power dissipation from the bottom of the package to the PCB surface. | JEDEC with no air flow                                                      | 9.6  | $^{\circ}\text{C/W}$ |
| $\Theta_{JC-Top}$ | Thermal resistance - junction to case $\Theta_{JC} = (T_J - T_C) / P_{\text{top}}$<br>$P_{\text{top}}$ = Power dissipation from the top of the package                               | JEDEC with no air flow                                                      | 15.5 | $^{\circ}\text{C/W}$ |

# 8. Ordering Information

ZIMC offers an RoHS package that is compliant with RoHS.

| Part Number | Grade    | Package      | Pack             | Status | Operation Temp |
|-------------|----------|--------------|------------------|--------|----------------|
| XZP821      | Consumer | QFN-48 E-PAD | Tape Reel 3000ea |        | 0 ~70°C        |