CD4029 CMOS Presettable Up/Down Counter

1. General Description

1.1 Description

CD4029 consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes.The inputs consist of a single CLOCK, $\overline{\text{CARRY-IN}}$ ($\overline{\text{CLOCK ENABLE}}$,BINARY/DECADE,UP/DOWN,PRESET ENABLE,and four individual JAM signals.Q1,Q2,Q3,Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock.A low on each JAM line,when the PRESET ENABLE signal is high,resets the counter to its zero count.The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY-IN}}$ and PRESET ENABLE signals are low.Advancement is inhibited when the $\overline{\text{CARRY-IN}}$ or PRESET ENABLE signals are high.The $\overline{\text{CARRY OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY-IN}}$ signal is low.The $\overline{\text{CARRY-IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK ENABLE}}$.The $\overline{\text{CARRY-IN}}$ terminal must be connected to VSS when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high;the counter counts in the decade mode when the BINARY/DECADE input is low.The counter counts up when the UP/DOWN input is high,and down when the UP/DOWN input is low.Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement.

Parallel clocking provides synchronous control and hence faster response from all counting outputs.Ripple-clocking allows for longer clock input rise and fall times.

1.2 Features

- Multi-Package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- “Preset Enable” and individual “Jam” inputs provided
- Binary or decade Up/Down counting
- BCD outputs in decade mode
- 100% tested for quiescent current at 18V
- Standardized symmetrical output characteristics
- Maximum input current of 1μA at 18V and 25℃
- 5V,10V, and 15V parametric ratings

1.3 Device Information

PART NUMBER	PACKAGE
CD4029	DIP
	SOP
	TSSOP

2. Pin Description and Functional Diagram

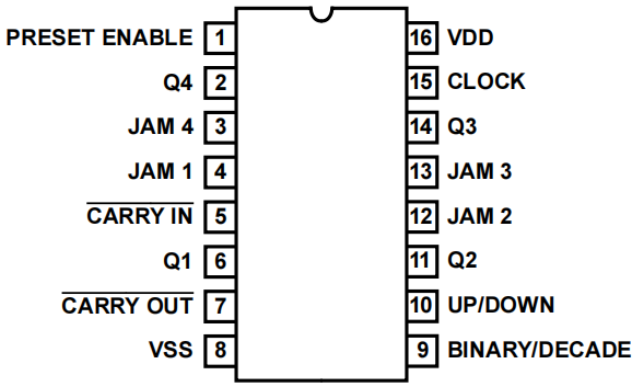


Figure 2.1 Top View

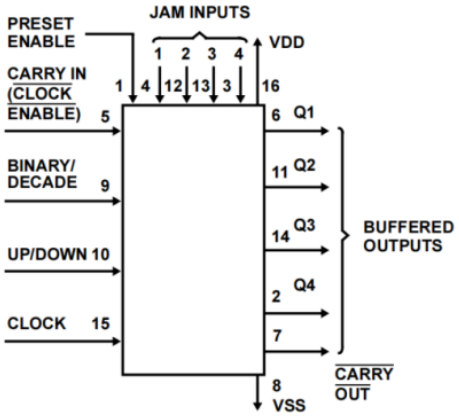


Figure 2.2 Functional Diagram

PIN No.	NAME	I/O	FUNCTION
1	PRESET ENABLE	I	Preset Control Input
2	Q4	O	Count Data Output
3	JAM 4	I	Parallel Data Input
4	JAM 1	I	Parallel Data Input
5	$\overline{\text{CARRY IN}}$	I	Carry Input
6	Q1	O	Count Data Output
7	$\overline{\text{CARRY OUT}}$	O	Carry Output
8	VSS		Ground
9	BINARY/DECADE	I	Binary/Decimal Control Input
10	UP/DOWN	I	Count Up/Down Control Input
11	Q2	O	Count Data Output
12	JAM 2	I	Parallel Data Input
13	JAM 3	I	Parallel Data Input
14	Q3	O	Count Data Output
15	CLOCK	I	Clock Input
16	VDD		Supply Voltage

3. System Diagram

3.1 Logic Diagram

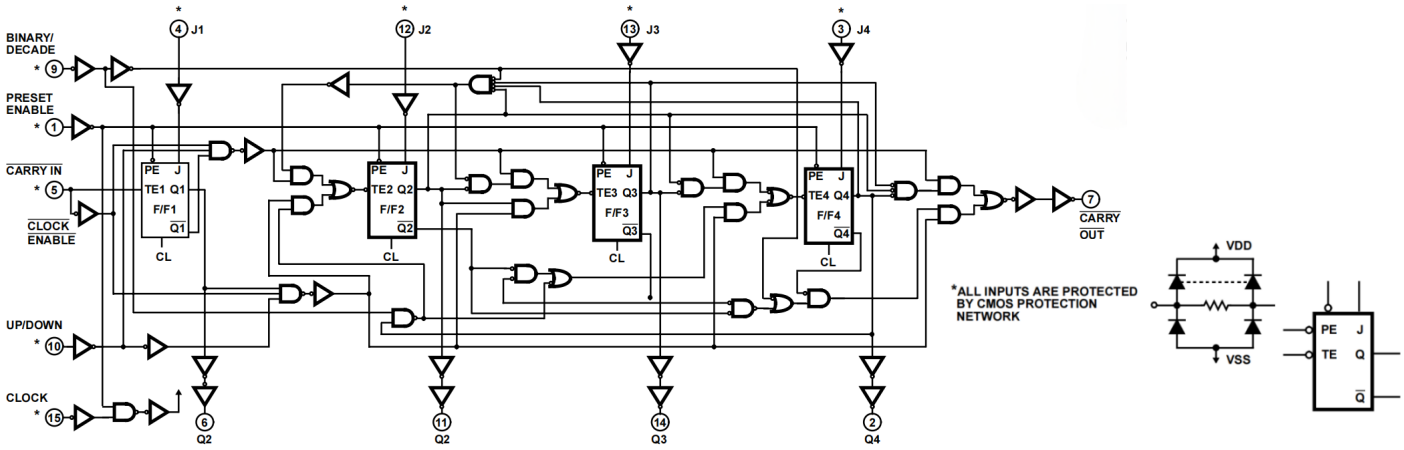


Figure 3.1：CD4029 Logic Diagram

3.2 Truth Table

Input				Output	
Clock	TE	PE	J	Q	$\overline{Q}$
X	X	0	0	0	1
↓	0	1	X	$\overline{Q}$	Q
X	X	0	1	1	0
↓	1	1	X	Q	$\overline{Q}$
↑	X	1	X	Q	$\overline{Q}$

X = Don't Care, 1 ≡ High State, 0 ≡ Low State,↑=positive-going transition,↓=negative-going transition

3.3 Function Table

Control Input	Logic Level	Action
BIN/DEC	1 0	Binary Count Decade Count
UP/DOWN(U/D)	1 0	Up Count Down Count
Preset Enable(PE)	1 0	Jam In No Jam
$\overline{\text{CARRY IN}}$ ($\overline{\text{CI}}$) ($\overline{\text{CLOCK ENABLE}}$)	1 0	No Counter Advance at POS Clock Transition Advance Counter at POS Clock Transition

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V_{DD}	DC Supply Voltage Range (Voltage Referenced to VSS Terminals)	-0.5	20	V
V_I	Input Voltage Range, All Inputs	0.5	VDD+0.5	V
P_D	Power Dissipation		500	mW
T_J	Junction Temperature		125	℃
T_{OP}	Operating Temperature	0	70	℃

Absolute maximum ratings are those values beyond which the device could be permanently damaged,These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

4.2 Electrical Characteristics

4.2.1 DC Specifications

(T_a=25℃, voltages are referenced to VSS (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition			MIN	TYP	MAX	Unit
		VO	VIN	VDD				
I_{DD}	Supply Current	--	0,5	5	--	0	1	uA
		--	0,10	10	--	0	1	uA
		--	0,18	18	--	0	1	uA
I_{OL}	Low Level Output Current	0.4	0,5	5	1.5	3.5	--	mA
		0.5	0,10	10	4	8	--	mA
		1.5	0,15	15	15	30	--	mA
I_{OH}	High Level Output Current	4.6	0,5	5	-1	-2	--	mA
		2.5	0,5	5	-4	-8	--	mA
		9.5	0,10	10	-2	-4	--	mA
		13.5	0,15	15	-7	-14	--	mA
V_{OL}	Low Level Output Voltage	--	0,5	5	--	0	0.05	V
		--	0,10	10	--	0	0.05	V
		--	0,15	15	--	0	0.05	V
V_{OH}	High Level Output Voltage	--	0,5	5	4.95	5	--	V
		--	0,10	10	9.95	10	--	V
		--	0,15	15	14.95	15	--	V
V_{IL}	Low Level Input Voltage	0.5,4.5	--	5	--	--	1.5	V
		1,9	--	10	--	--	3	V
		1.5,13.5	--	15	--	--	4	V
V_{IH}	High Level Input Voltage	0.5,4.5	--	5	3.5	--	--	V
		1,9	--	10	7	--	--	V
		1.5,13.5	--	15	11	--	--	V
I_{IN}	Input Leakage Current	--	0,18	18	--	0	±1	uA

5. Timing Diagrams

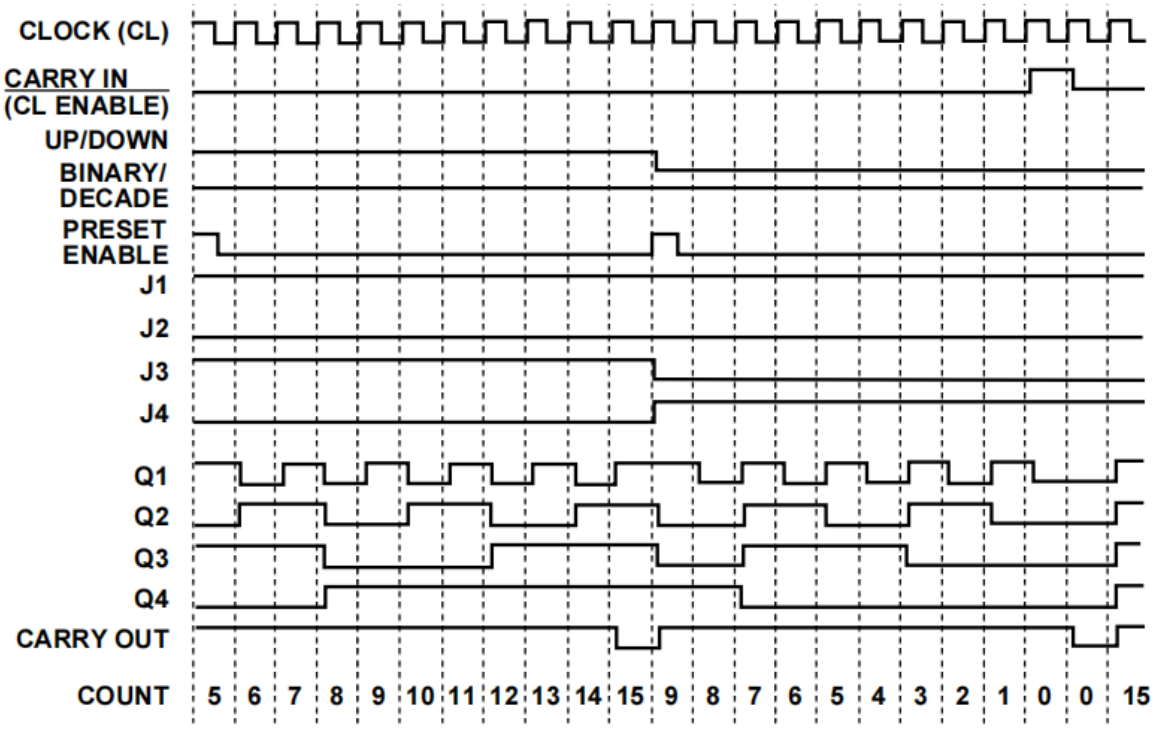


Figure 5.1：Timing diagrams-binary mode

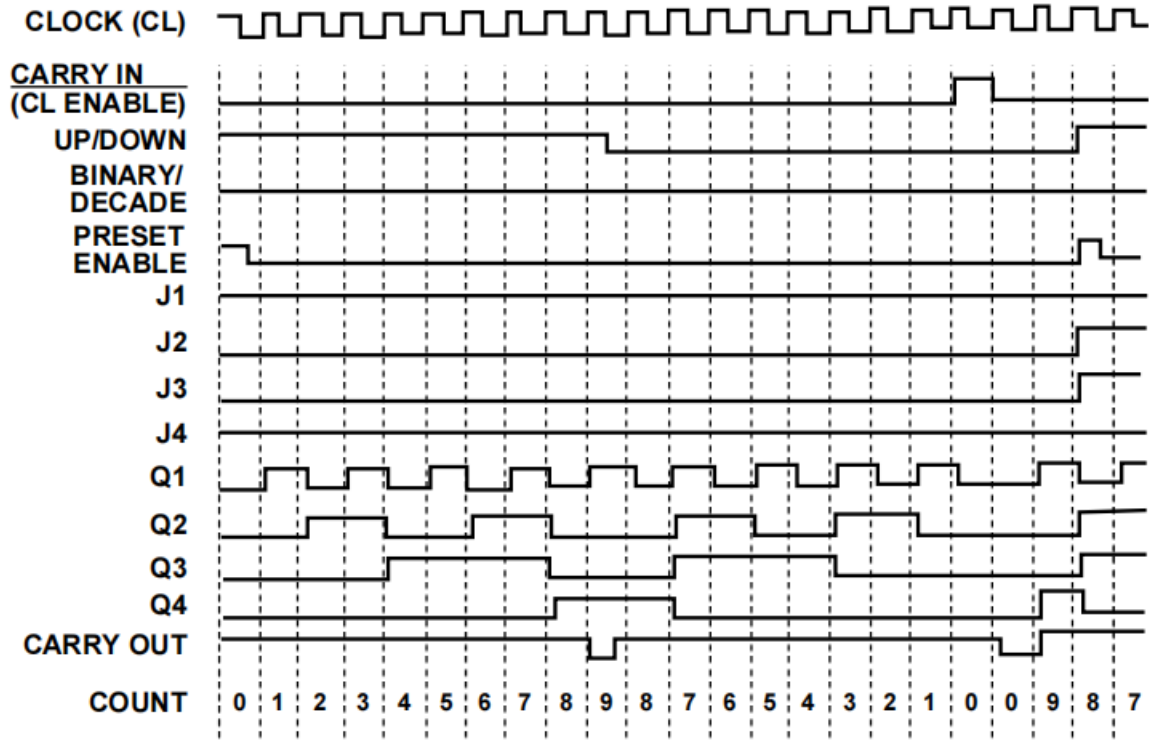
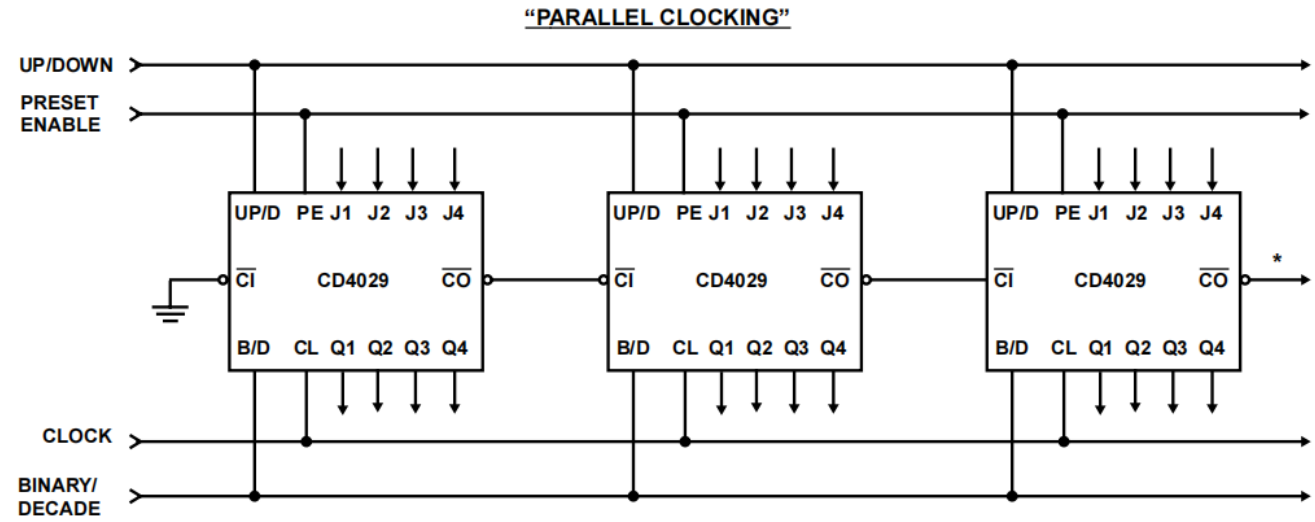
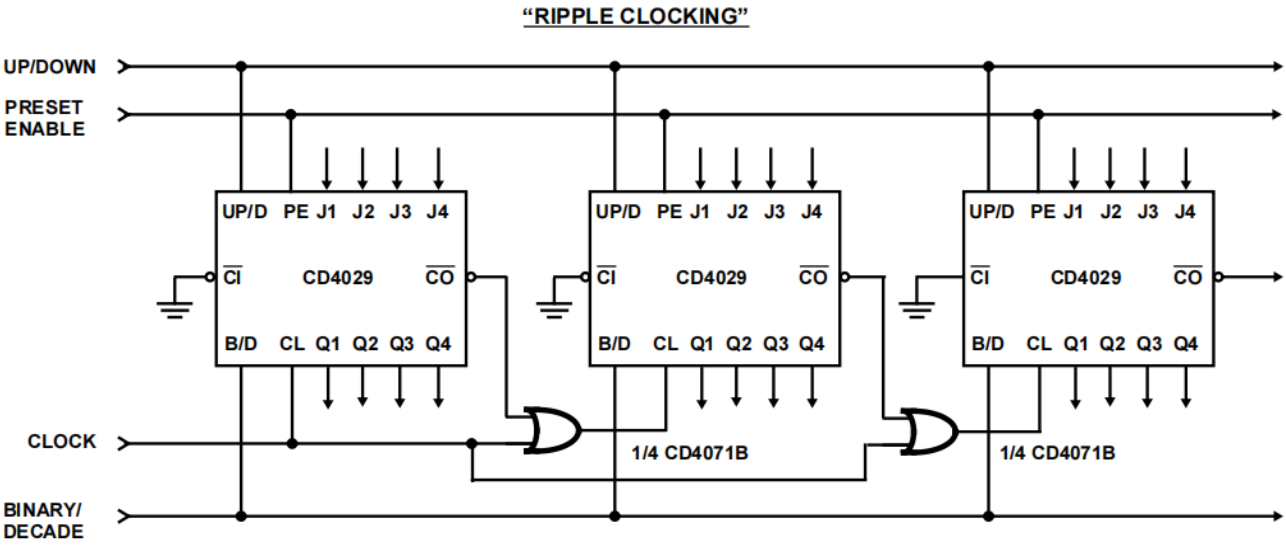


Figure 5.2：Timing diagrams-decade mode

6. Applications information



* $\overline{\text{CARRY OUT}}$ lines at the 2nd,3rd,etc.stages may have a negative-going glitch pulse resulting from differential delays of different CD4029 IC's.These negative-going glitches do not affect proper CD4029 operation.However,if the $\overline{\text{CARRY OUT}}$ signals are used to trigger other edge-sensitive logic devices,such as FF's or counters,the $\overline{\text{CARRY OUT}}$ signals should be gated with the clock signal using a 2 input OR gate such as CD4071B.



Ripple Clocking Mode:
The Up/Down control can be changed at any count.The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high.For cascading counters operating in a fixed up-count or down-count mode,the $\overline{\text{OR}}$ gates are not required between stages,and CO is connected directly to the CL input of the next stage with $\overline{\text{CI}}$ grounded.

Figure 6.1/6.2：Cascading counter packages

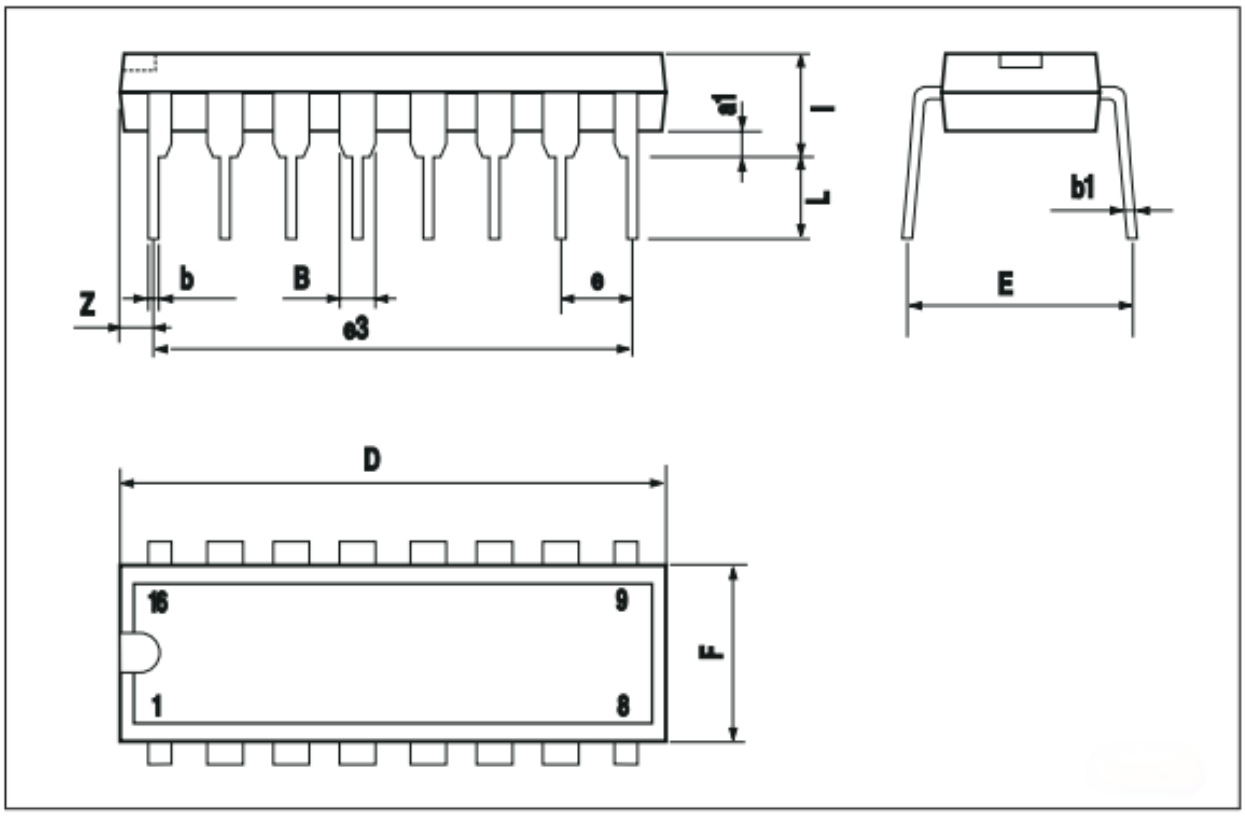
7. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
CD4029ND16ATBE	DIP	16	Tube	25
CD4029NS16ARDQ	SOP	16	Tape & Reel	4000
CD4029TS16ARDQ	TSSOP	16	Tape & Reel	4000

8. Package Information

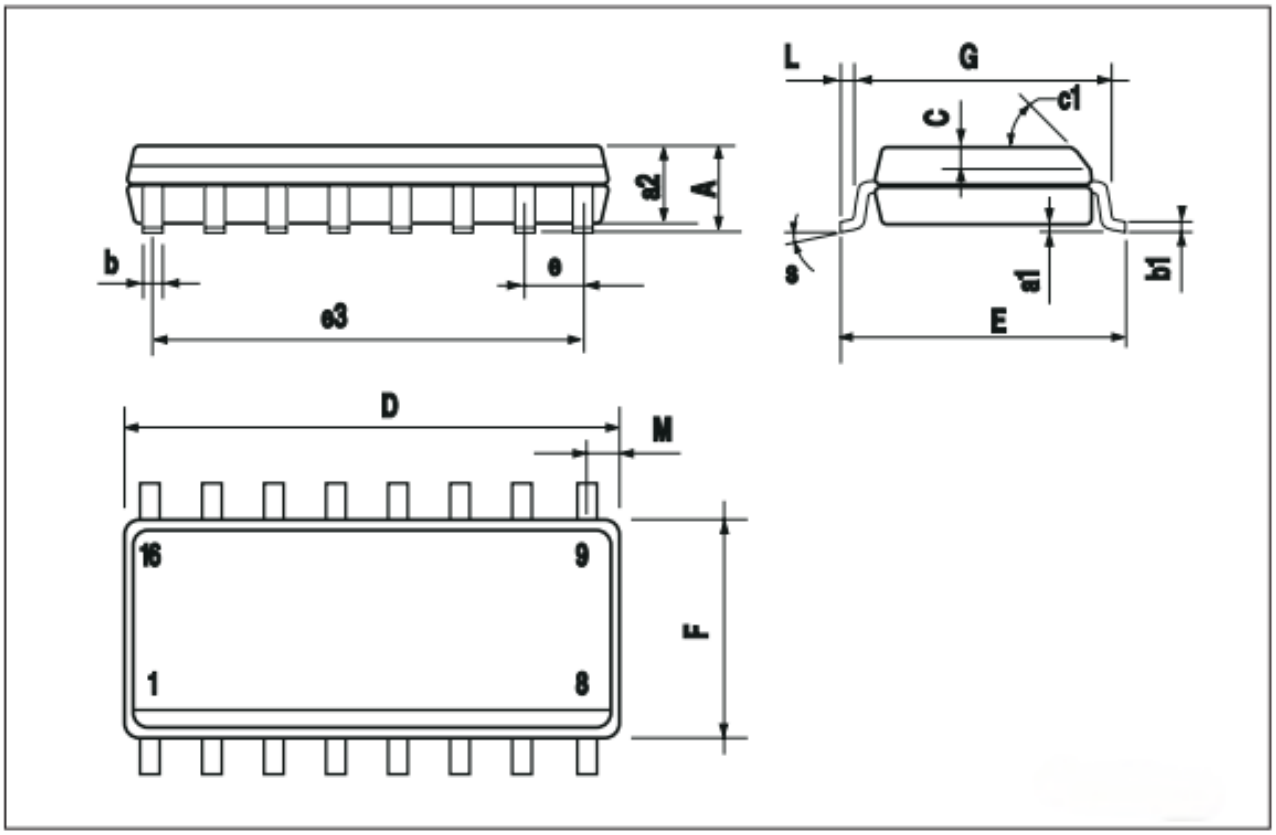
8.1 DIP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



8.2 SOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



8.3 TSSOP16

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030