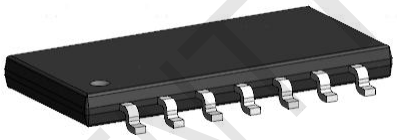
WSTD723GW

Smart High-Side Power Switch Dual Channel，70mΩ，SOP-14L，*AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12 V and 24 V trucks + trailer and transportation systems

Package	SOP-14L
Marking	WSTD723GW



Basic Features

- Dual channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Optimized electromagnetic compatibility
- Fast switching device
- Wide operating voltage range

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage	V_S	60V
Operating voltage range	V_{NOM}	7-58V
On-state resistance (per channel，T_j = 25℃)	R_{ON}	70mΩ
On-state resistance (two channels parallel，T_j = 25℃)		35mΩ
Nominal load current (one channel active，T_j = 25℃)	$I_{L(NOM)1}$	4A
Nominal load current (All channels active，T_j = 25℃)	$I_{L(NOM)2}$	6A
Current limitation (per channel)	I_{LIMH}	12A
Supply current in sleep	I_{SLEEP}	6uA

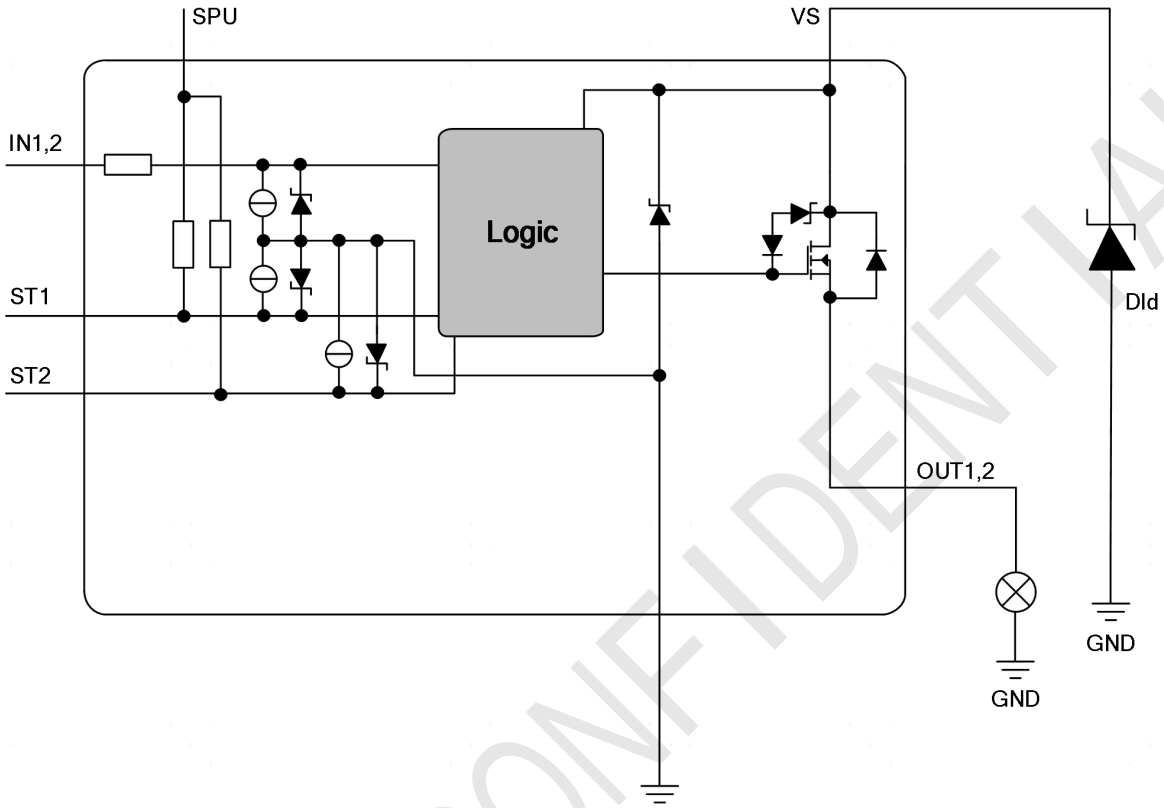
Diagnostic Functions

- Diagnostic feedback with open drain output and integrated pull up resistors
- Off-state open load detection
- OUT short to VS detection
- Feedback of Thermal shutdown in ON-state
- Diagnostic feedback of both channels works properly in case of inverse current

Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Thermal shutdown
- Protection against loss of ground and loss of Vbb
- Reverse battery protection with external resistor
- Electrostatic discharge protection

Typical Application Circuit

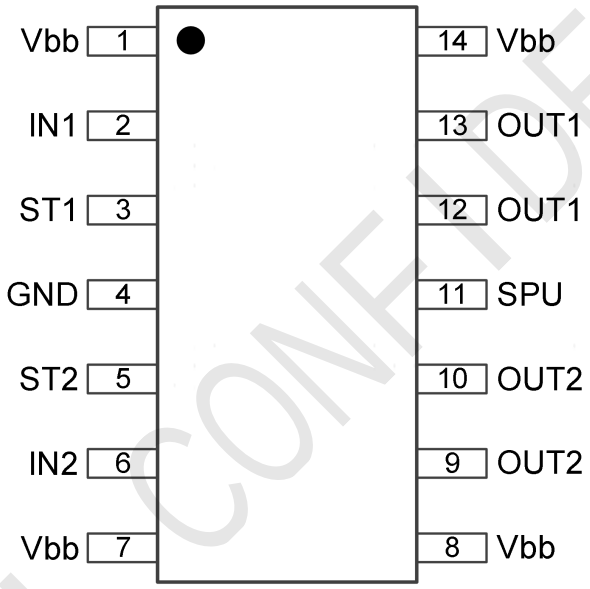


Ordering Information

Package	Top Mark	Part No.
SOP-14L, Pb-free	WSTD723GW XXYMXX	WSTD723GW

Pin Configuration

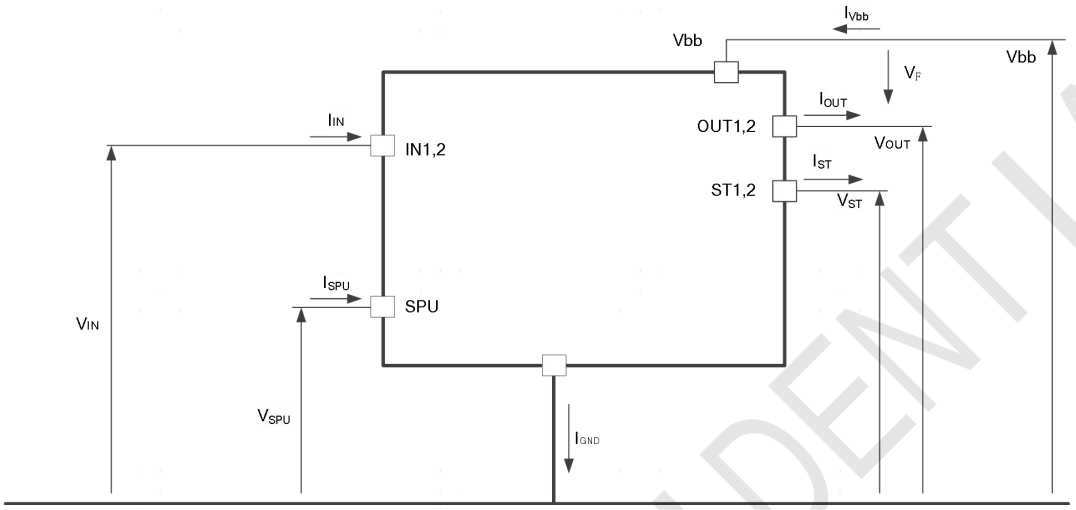
Top view



Pin Description

Pin Name	Pin NO.	Pin Description
Vbb	1/7/8/14	**Positive power supply voltage.** Design the wiring for the simultaneous max. short circuit currents
IN1	2	**Input 1,2** activates channel 1,2 in case of logic high signal
IN2	6	
OUT1	12/13	**Output 1,2** protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current; both output pins have to be connected in parallel for operation according this spec.
OUT2	9/10	
ST1	3	**Diagnostic feedback 1,2** of channel 1,2 open drain
ST2	5	
GND	4	**Logic Ground**
SPU	11	Connection for **external pull up voltage** source for the open drain status output.

Current and Voltage Conventions



Note2: $V_F = V_{OUT}$ - Vbb during reverse battery condition.

Absolute Maximum Ratings (Note3)

Symbol	Parameter	Value	Unit
V_{bb}	DC supply voltage	60	V
$-V_{bb}$	Reverse DC supply voltage	0.3	V
V_{bb}	Supply voltage for full short circuit protection ($T_{j,start}$=-40℃-150°C)	50	V
I_{OUT}	OUT0,1 DC output current	Internally limited	A
P_{tot}	Power dissipation (DC, T_a=25℃)	3.0	W
	All channels active (T_a=85℃)	1.6	
V_{IN}	IN1,2 DC input voltage	-6.0 to 6.0	V
V_{SPU}	Status pull up voltage	-0.3 to 6.0	V
V_{ST}	ST1,2 DC output voltage	-0.3 to 6.0	V
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note4)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance (all channels active)	35	℃/W

Note4：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note5)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$ 3)	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_{bb} connected (HBM)	±4	kV
$V_{ESD(CDM)}$ 4)	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	±750	V

Note5：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

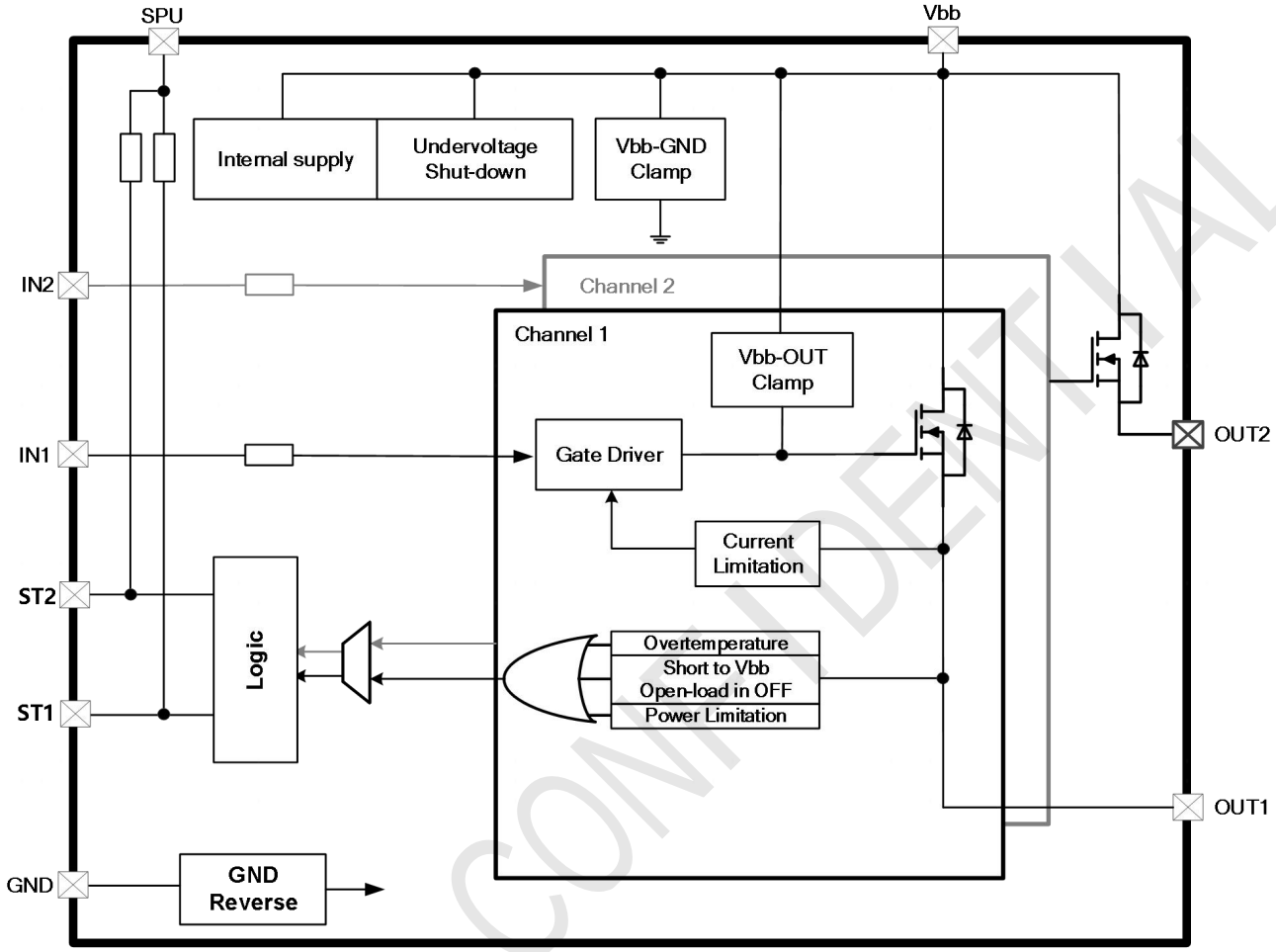
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

EAS Susceptibility (Note6)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse (one channel)			90	mJ	I_{OUT} = 4A $T_{J(0)}$ = 150 °C V_{bb} = 28 V

Note6:：Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note7) , 7V<V_S < 58 V; -40°C < Tj < 150°C, unless otherwise specified

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		7	24	58	V
Under voltage shutdown	V_{USD}			3.5	5.0	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=2A, T_j = 25℃		70		mΩ
		I_{OUT}=2A,T_j =150℃			140	
		I_{OUT}=2A,V_S =5V, T_j = 25℃			110	
Nominal load current (One Channel Active)	$I_{L(NOM)1}$	T_A=25℃		4		A
Nominal load current at T_A=85℃ (One Channel Active)	$I_{L(NOM)1\_85}$	T_A=85℃, T_j < 150℃		3		A
Nominal load current (All Channels Active)	$I_{L(NOM)2}$	T_A=25℃		6		A
Nominal load current at T_A=85℃ (All Channels Active)	$I_{L(NOM)2\_85}$	T_A=85℃, T_j < 150℃		4		A
Inverse Current Capability	$I_{L(INV)}$	V_{bb}<V_{OUT}, V_{IN}=5V, T_A=25℃		4		A
V_{bb} clamp voltage	V_{CLAMP}	I_S=20 mA	60	64	71	V
Supply current in sleep	I_{SLEEP}	V_{bb} =36V, V_{IN}=V_{OUT}=0V,T_j =25℃		6.0	12	μA
		V_{bb} =36V, V_{IN}=V_{OUT}=0V,T_j= 125℃			20	μA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_{bb} =36V, V_{INx}=5V, one channel ON		3.0	6.0	mA
		V_{bb} =36V, $V_{IN1,2}$=5V, all channels ON		6.0	12	
Off-state output current	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_{bb}=36V, T_j =25℃	0	2	6	μA
		V_{IN} =V_{OUT}=0V, V_{bb}=36V, T_j =125℃	0		12	μA
OUT - V_{bb} diode voltage	V_F	I_{OUT} =-2A, T_j =150℃			0.9	V

Switching

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	V_{bb}=28V,R_L=14Ω		10	40	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$			20	80	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	V_{bb}=28V,R_L=14Ω	1.0	1.8	3.6	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		1.0	2.0	4.0	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	V_{bb}=28V,R_L=14Ω	-50		50	us

Logic input (IN1,2)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	V_{LOW}=0.9V	2	11	35	uA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V

High level logic input current	I_{HIGH}	V_{HIGH}=2.0V	1	10	30	uA
Logic input hysteresis voltage	$V_{(hyst)}$			0.2		V

Protections

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DC short circuit current	I_{LIMH}	5V < V_{bb}< 36V ,V_{DS}=6V	8	12	18	A
		V_{DS}=32V		8		
Short circuit current during thermal cycling	I_{LIML}	V_{bb}=24V, T_R<T_j<$T_{TSD,}$		4		
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Current limit reset temperature	T_R			135		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃		60		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=2A, L= 6mH, T_j =-40℃ to 150℃	V_{bb}-60	V_{bb}-64	V_{bb}-71	V

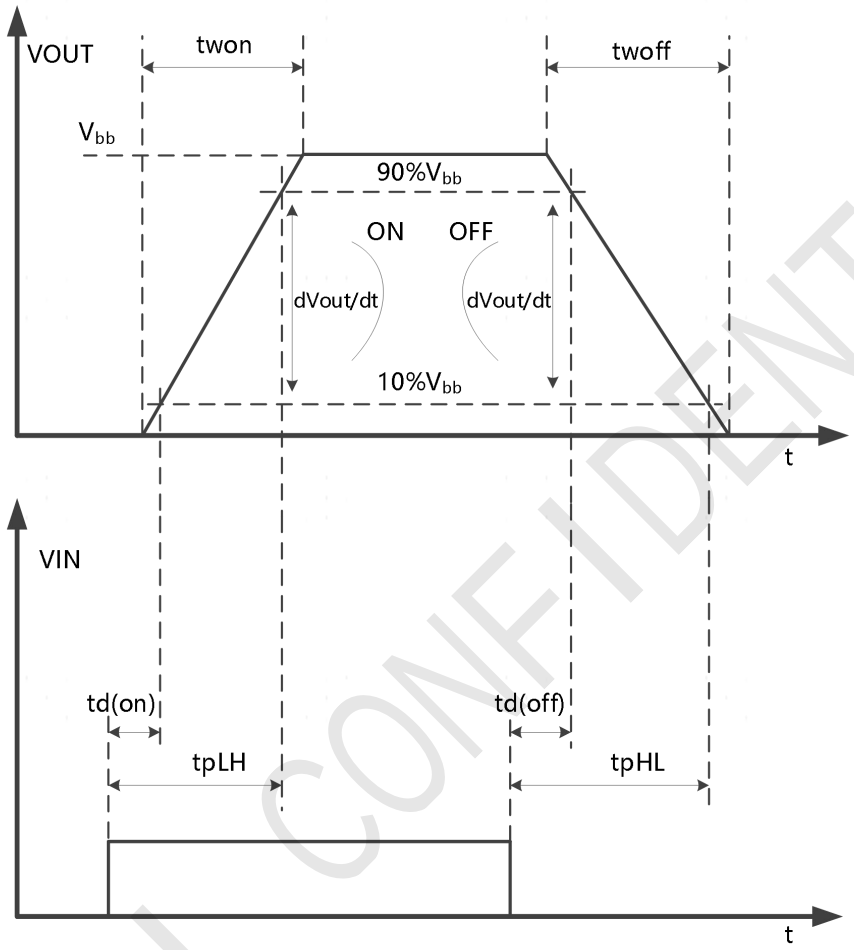
OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load detection voltage	V_{OL}	V_{INx} = 0V	2	3	4	V
OFF-state open load detection current	$I_{L(off2)}$	V_{INx} = 0V, V_{OUT}=V_{OL},T_j = -40℃ to 150℃		2		uA

Note7: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew

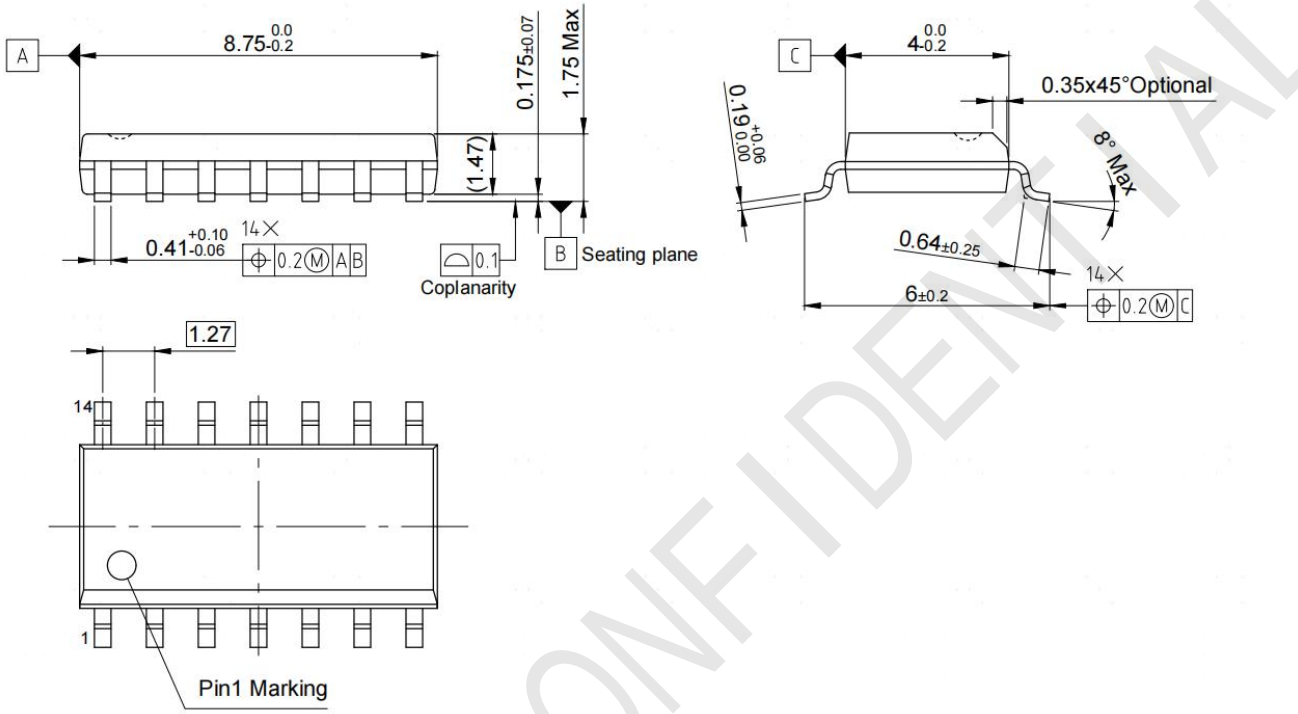


Truth table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	WSTD723GW
Normal Operation	L H	L H	L H
Open Load	L H	V_{OUT}＞3V H	H H
Short circuit to GND	L H	L L	L L
Short circuit to Vbb	L H	H H	H H
Overtemperature	L H	L L	L L

Package Outline

SOP-14L

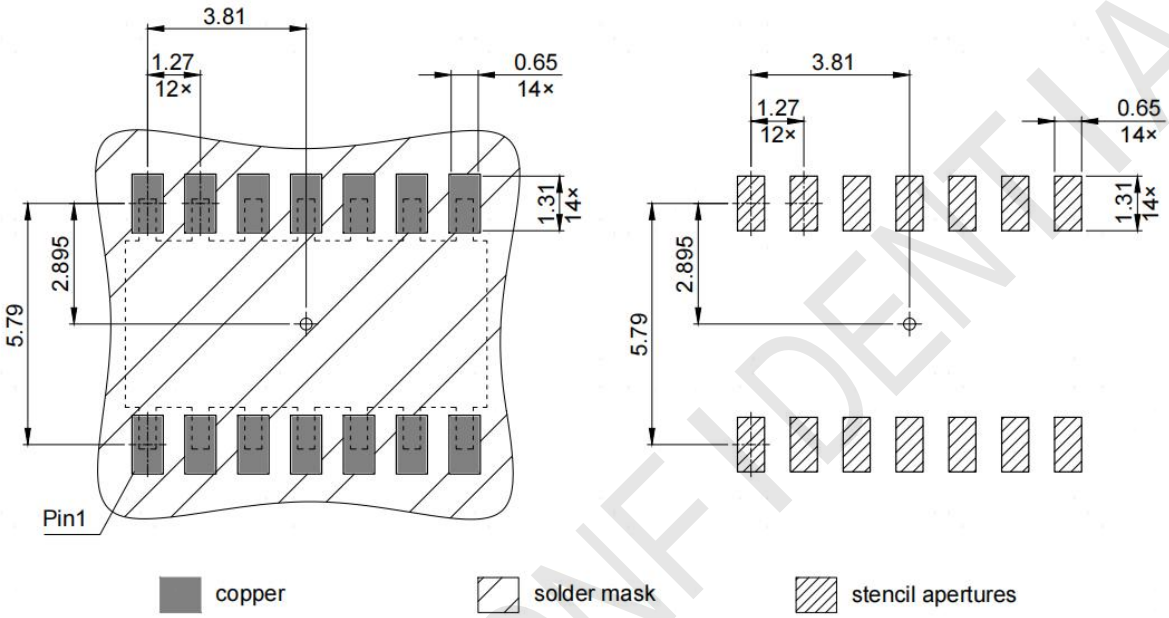


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.75
A1	0.10	_	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	_	0.47
b1	0.38	0.41	0.44
c	0.20	_	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	_	0.50
L	0.50	_	0.80
L1	1.05REF		
θ	0	_	8°

Soldering Footprint

SOP-14L

Unit：mm



Recommended Solder PAD Pitch AND Dimensions

CONTACT

Winsemi Microelectronics Co., Ltd.
ADD: Room 3101-3102, 31F, Building 8A, Shenzhen International Innovation Valley, Nanshan District, Shenzhen, P.R. China.
Post Code : 518040
Tel : 86-0755-82506288
Fax: 86-0755-82506299
Website : www.winsemi.com